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April 2001

FDC645N N-Channel PowerTrench[®] MOSFET

General Description

SEMICONDUCTOR IM

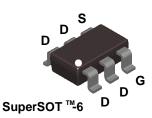
This N-Channel MOSFET has been designed specifically to improve the overall efficiency of DC/DC converters using either synchronous or conventional switching PWM controllers. It has been optimized for low gate charge, low $R_{DS(ON)}$ and fast switching speed.

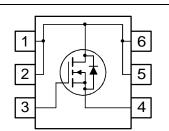
Applications

• DC/DC converter

Features

- 5.5 A, 30 V. $R_{DS(ON)} = 30 \text{ m}\Omega @ V_{GS} = 4.5 \text{ V}$ $R_{DS(ON)} = 26 \text{ m}\Omega @ V_{GS} = 10 \text{ V}$
- High performance trench technology for extremely low $R_{\text{DS}(\text{ON})}$
- Low gate charge (13 nC typical)
- High power and current handling capability





Absolute Maximum Ratings TA=25°C unless otherwise noted

Symbol		Parameter	Ratings	Units		
V _{DSS}	Drain-Source Voltage			30	V	
V _{GSS}	Gate-Source Voltage			±12	V	
ID	Drain Curre	nt – Continuous	(Note 1a)	5.5	A	
		 Pulsed 		20		
P _D	Maximum Power Dissipation (Note 1a)		(Note 1a)	1.6	W	
			(Note 1b)	0.8		
T _J , T _{STG}	Operating and Storage Junction Temperature Range			-55 to +150		
Therma	I Charac	teristics				
R _{0JA}	Thermal Resistance, Junction-to-Ambient (Note 1a)			78	°C/W	
R _{0JC}	Thermal Resistance, Junction-to-Case (Note 1)			30		
		g and Orderin	g Information Reel Size	Tape width	Quantity	
.645		FDC645N	7"		3000 units	

FDC645N

Symbol	Parameter	Test Conditions	Min	Тур	Max	Units
Off Char	acteristics			I		I
BV _{DSS}	Drain–Source Breakdown Voltage	$V_{GS} = 0 V, I_D = 250 \mu A$	30			V
<u>ΔBV_{DSS}</u> ΔT _J	Breakdown Voltage Temperature Coefficient	$I_D = 250 \ \mu\text{A}$, Referenced to 25°C		22		mV/°C
I _{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = 24 V, V_{GS} = 0 V$			1	μA
I _{GSSF}	Gate-Body Leakage, Forward	$V_{GS} = 12 \text{ V}, V_{DS} = 0 \text{ V}$			100	nA
I _{GSSR}	Gate-Body Leakage, Reverse	$V_{GS} = -12 V, V_{DS} = 0 V$			-100	nA
On Char	acteristics (Note 2)					
V _{GS(th)}	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_{D} = 250 \ \mu A$	0.8	1.4	2	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate Threshold Voltage Temperature Coefficient	$I_D = 250 \ \mu A$, Referenced to $25^{\circ}C$		- 4		mV/°C
R _{DS(on)}	Static Drain–Source On–Resistance	$ \begin{array}{l} V_{GS} = 4.5 \ V, \ I_D = 5.5 \ A \\ V_{GS} = 10 \ V, \ I_D = 6.2 \ A \\ V_{GS} = 4.5 \ V, \ I_D = 5.5 \ A, \ T_J = 125^\circ C \end{array} $		25 23 34	30 26 48	mΩ
I _{D(on)}	On-State Drain Current	$V_{GS} = 4.5 V, V_{DS} = 5 V$	20			Α
g fs	Forward Transconductance	$V_{DS} = 10 \text{ V}, \qquad I_D = 5.5 \text{ A}$		33		S
Dynamic	Characteristics					
Ciss	Input Capacitance			1460		pF
Coss	Output Capacitance	f = 1.0 MHz		227		pF
Crss	Reverse Transfer Capacitance			96		pF
Switchin	g Characteristics (Note 2)		•	•	•	•
t _{d(on)}	Turn–On Delay Time	$V_{DS} = 15 \text{ V}, I_D = 1 \text{ A},$		8	16	ns
tr	Turn–On Rise Time	$V_{GS} = 4.5 \text{ V}, \text{ R}_{GEN} = 6 \Omega$		9	18	ns
t _{d(off)}	Turn–Off Delay Time			35	56	ns
t _f	Turn–Off Fall Time	1		7	14	ns
Qg	Total Gate Charge	$V_{DS} = 15 V, I_D = 6.2 A,$	1	13	21	nC
Q _{gs}	Gate-Source Charge	V _{GS} = 4.5 V		3.6		nC
Q _{gd}	Gate-Drain Charge	7		3.6		nC
Drain-So	ource Diode Characteristics	and Maximum Ratings	•	•		•
Is	Maximum Continuous Drain–Source				1.3	Α
V _{SD}	Drain–Source Diode Forward Voltage	$V_{GS} = 0 V$, $I_S = 1.3 A$ (Note 2)		0.7	1.2	V

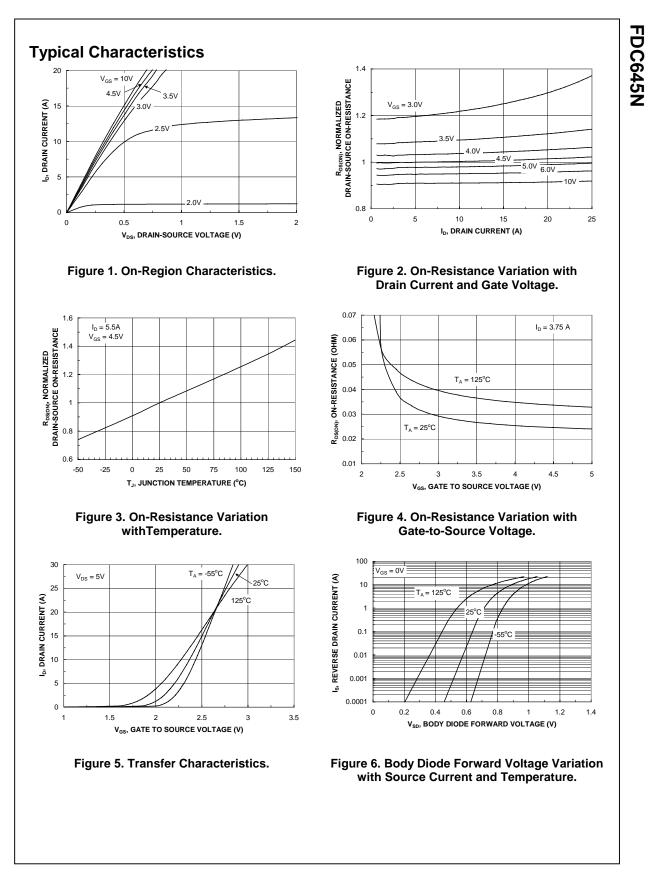
Notes:

1. R_{0JA} is the sum of the junction-to-case and case-to-ambient resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. R_{0JC} is guaranteed by design while R_{0CA} is determined by the user's board design.

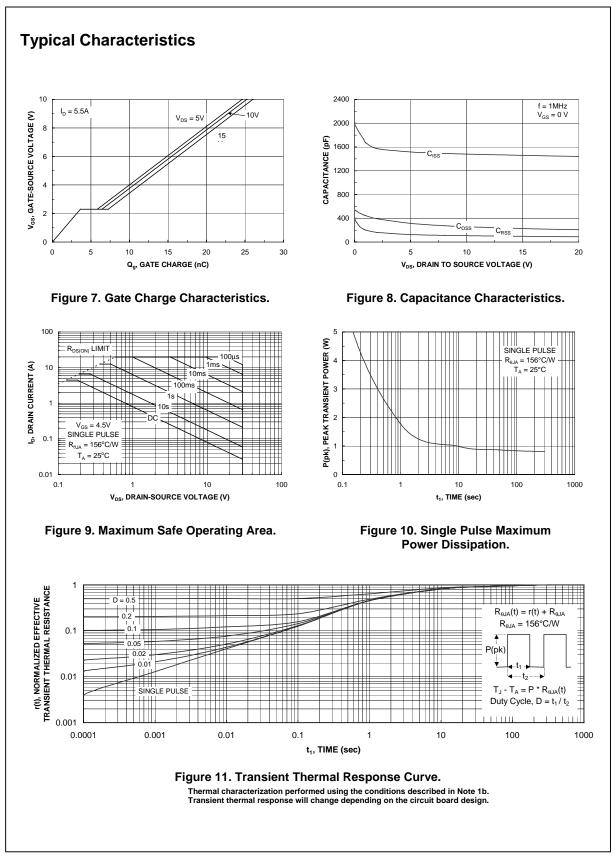
a. 78°C/W when mounted on a 1in^2 pad of 2oz copper on FR-4 board.

b. 156°C/W when mounted on a minimum pad.

2. Pulse Test: Pulse Width $\leq 300~\mu s,$ Duty Cycle $\leq 2.0\%$



FDC645N Rev C(W)



FDC645N

FDC645N Rev C(W)

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