ON Semiconductor

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ON Semiconductor®

FDD3860

N-Channel PowerTrench® MOSFET

100 V, 29 A, 36 mΩ

Features

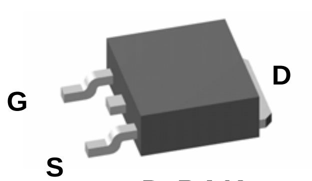
- Max $r_{DS(on)}$ = 36 mΩ at V_{GS} = 10 V, I_D = 5.9 A
- High Performance Trench Technology for Extremely Low $r_{DS(on)}$
- 100% UIL Tested
- RoHS Compliant

General Description

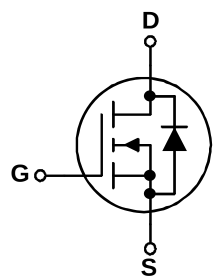
This N-Channel MOSFET is rugged gate version of ON Semiconductor's advanced Power Trench® process. This part is tailored for low $r_{DS(on)}$ and low Qg figure of merit, with avalanche ruggedness for a wide range of switching applications.

Applications

- DC-AC Conversion
- Synchronous Rectifier



D-PAK
(TO-252)



MOSFET Maximum Ratings T_C = 25°C unless otherwise noted.

Symbol	Parameter			Ratings	Units
V_{DS}	Drain to Source Voltage			100	V
V_{GS}	Gate to Source Voltage			±20	V
I_D	Drain Current -Continuous	T_C = 25°C		29	A
	-Continuous	T_A = 25°C	(Note 1a)	6.2	
	-Pulsed			60	
E_{AS}	Single Pulse Avalanche Energy		(Note 3)	121	mJ
P_D	Power Dissipation	T_C = 25°C		83	W
	Power Dissipation	T_A = 25°C	(Note 1a)	3.75	
T_J, T_{STG}	Operating and Storage Junction Temperature Range			-55 to +175	°C

Thermal Characteristics

$R_{\theta JC}$	Thermal Resistance, Junction to Case		1.8	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	(Note 1a)	40	

Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
FDD3860	FDD3860	D-PAK (TO-252)	13''	16 mm	2500 units

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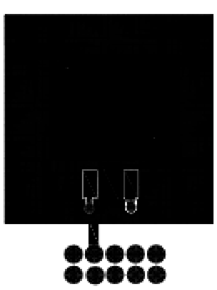
Electrical Characteristics $T_J = 25°C$ unless otherwise noted.

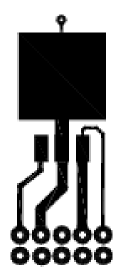
Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
Off Characteristics						
BV_{DSS}	Drain to Source Breakdown Voltage	$I_D = 250\mu A$, $V_{GS} = 0V$	100			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	$I_D = 250\mu A$, referenced to 25°C		98		mV/°C
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = 80V$, $V_{GS} = 0V$			1	μA
I_{GSS}	Gate to Source Leakage Current	$V_{GS} = \pm 20V$, $V_{DS} = 0V$			±100	nA
On Characteristics						
$V_{GS(th)}$	Gate to Source Threshold Voltage	$V_{GS} = V_{DS}$, $I_D = 250\mu A$	2.5	3.8	4.5	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate to Source Threshold Voltage Temperature Coefficient	$I_D = 250\mu A$, referenced to 25°C		-11.4		mV/°C
$r_{DS(on)}$	Static Drain to Source On Resistance	$V_{GS} = 10V$, $I_D = 5.9A$		29	36	mΩ
		$V_{GS} = 10V$, $I_D = 5.9A$, $T_J = 125°C$		51	64	
g_{FS}	Forward Transconductance	$V_{DS} = 10V$, $I_D = 5.9A$		20		S
Dynamic Characteristics						
C_{iss}	Input Capacitance	$V_{DS} = 50V$, $V_{GS} = 0V$, f = 1MHz		1310	1740	pF
C_{oss}	Output Capacitance			100	130	pF
C_{rss}	Reverse Transfer Capacitance			45	70	pF
R_g	Gate Resistance	f = 1MHz		1.6		Ω
Switching Characteristics						
$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = 50V$, $I_D = 5.9A$, $V_{GS} = 10V$, $R_{GEN} = 6\Omega$		16	29	ns
t_r	Rise Time			10	21	ns
$t_{d(off)}$	Turn-Off Delay Time			24	39	ns
t_f	Fall Time			7	15	ns
Q_g	Total Gate Charge at 10V	$V_{DD} = 50V$, $I_D = 5.9A$		22	31	nC
Q_{gs}	Gate to Source Charge			7.1		nC
Q_{gd}	Gate to Drain "Miller" Charge			6.3		nC
Drain-Source Diode Characteristics						
V_{SD}	Source to Drain Diode Forward Voltage	$V_{GS} = 0V$, $I_S = 2.0A$ (Note 2)		0.7	1.2	V
		$V_{GS} = 0V$, $I_S = 5.9A$ (Note 2)		0.8	1.3	
t_{rr}	Reverse Recovery Time	$I_F = 5.9A$, di/dt = 100A/μs		34	55	ns
Q_{rr}	Reverse Recovery Charge			40	64	nC

Notes:

1: $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design while $R_{\theta JA}$ is determined by the user's board design.



a) 40°C/W when mounted on a 1 in² pad of 2 oz copper



b) 96°C/W when mounted on a minimum pad.

2: Pulse Test: Pulse Width < 300μs, Duty cycle < 2.0%.

3: Starting $T_J = 25°C$, L = 3mH, $I_{AS} = 9A$, $V_{DD} = 100V$, $V_{GS} = 10V$.

Typical Characteristics T_J = 25°C unless otherwise noted.

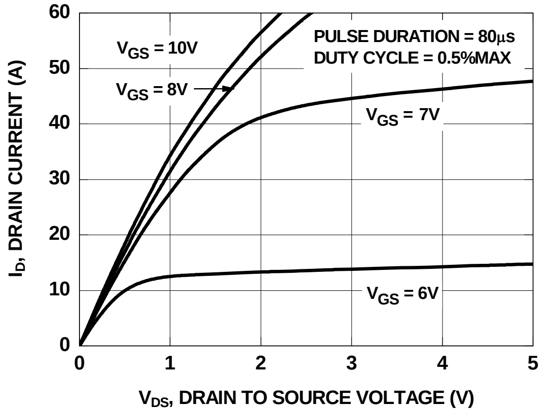


Figure 1. On-Region Characteristics

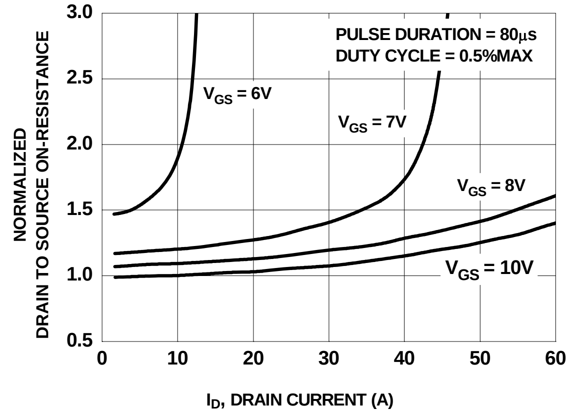


Figure 2. Normalized On-Resistance vs. Drain Current and Gate Voltage

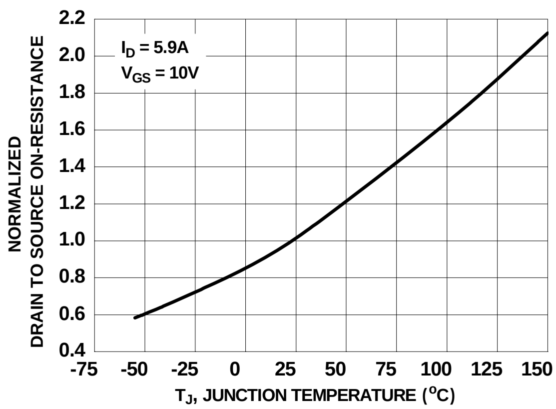


Figure 3. Normalized On-Resistance vs. Junction Temperature

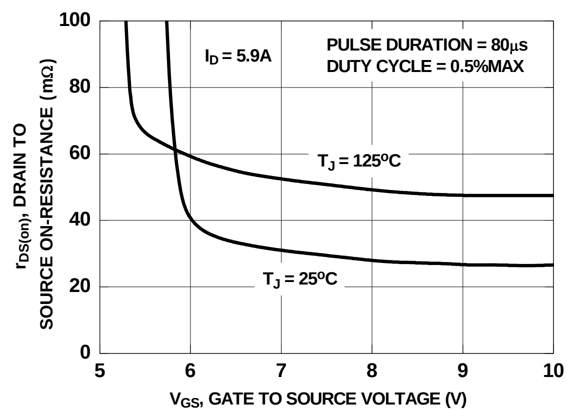


Figure 4. On-Resistance vs. Gate to Source Voltage

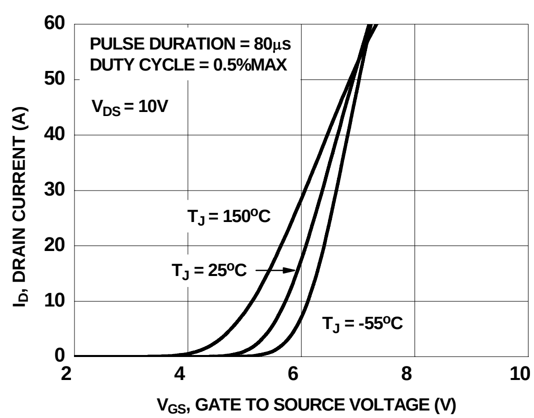


Figure 5. Transfer Characteristics

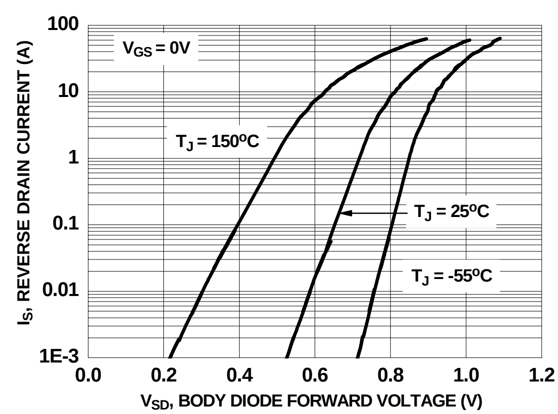


Figure 6. Source to Drain Diode Forward Voltage vs. Source Current

Typical Characteristics T_J = 25°C unless otherwise noted.

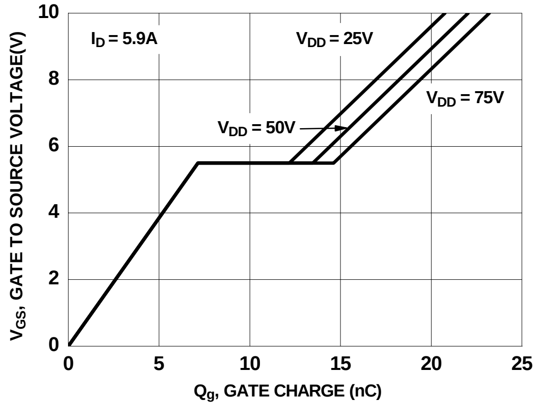


Figure 7. Gate Charge Characteristics

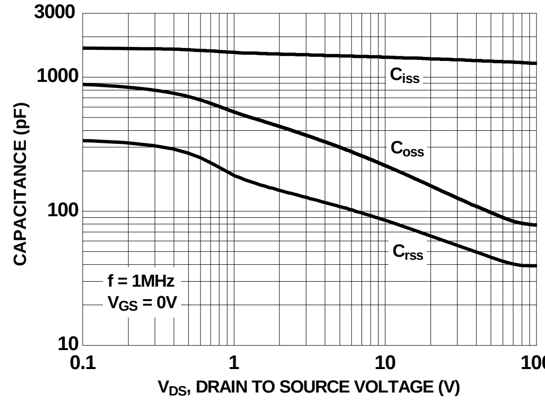


Figure 8. Capacitance vs. Drain to Source Voltage

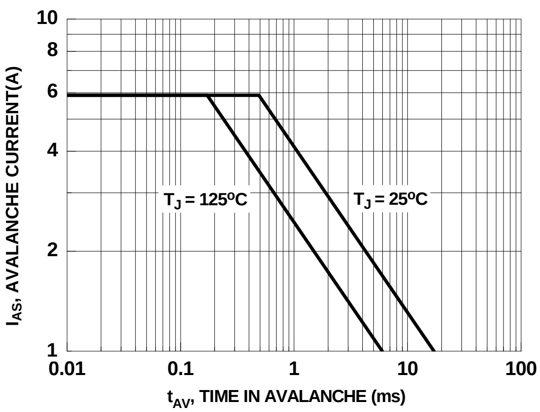


Figure 9. Unclamped Inductive Switching Capability

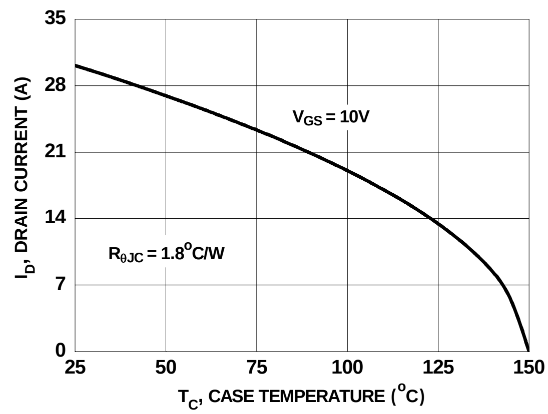


Figure 10. Maximum Continuous Drain Current vs. Case Temperature

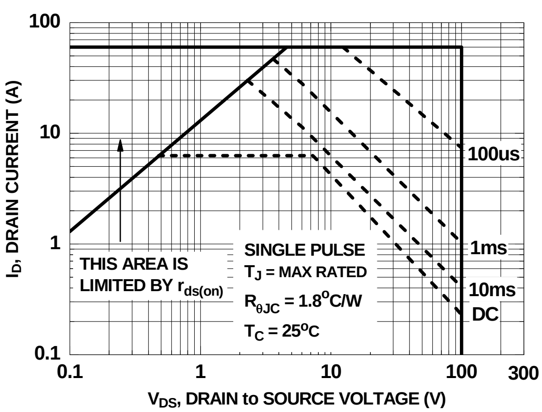


Figure 11. Forward Bias Safe Operating Area

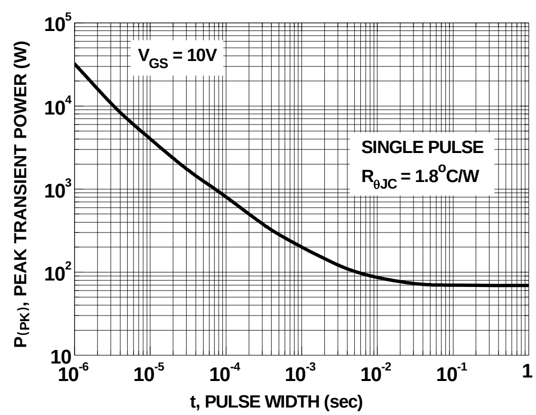


Figure 12. Single Pulse Maximum Power Dissipation

Typical Characteristics T_J = 25°C unless otherwise noted.

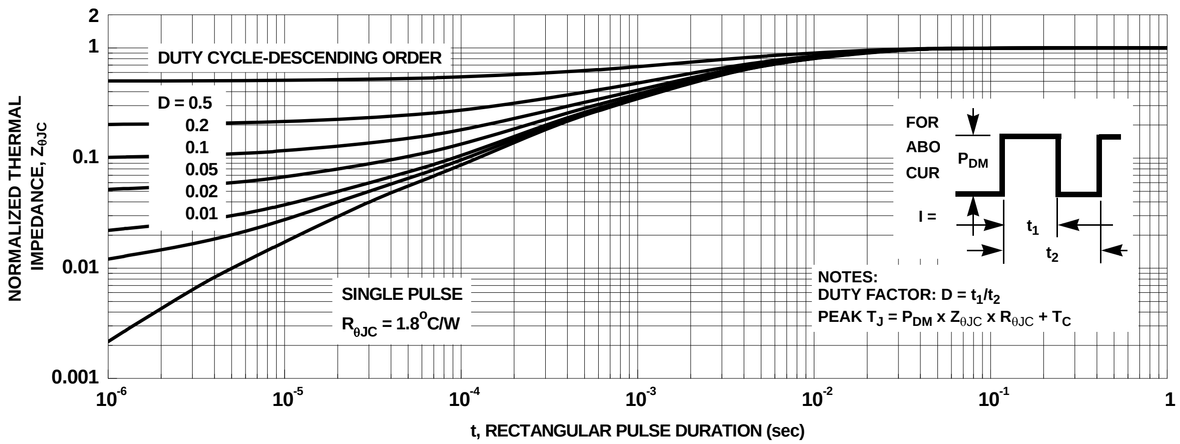


Figure 13. Transient Thermal Response Curve

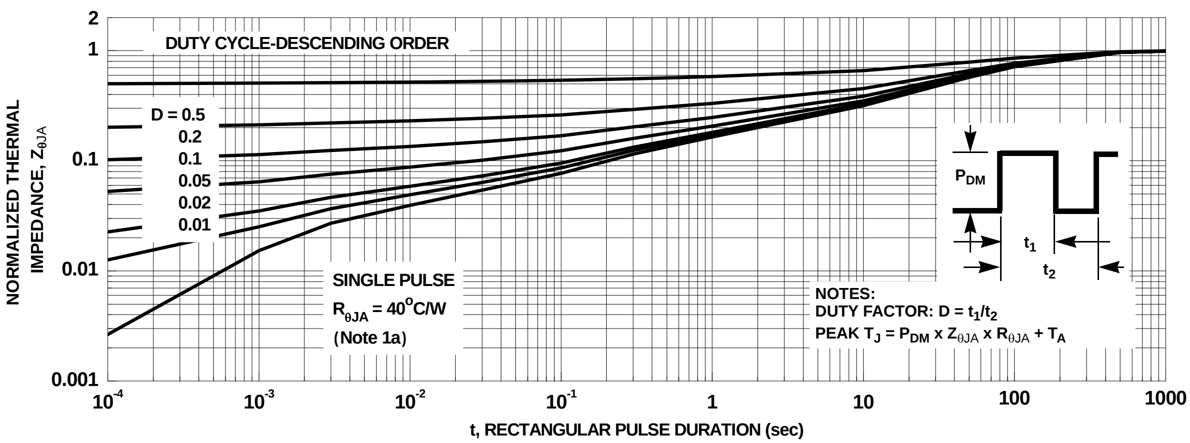


Figure 14. Transient Thermal Response Curve

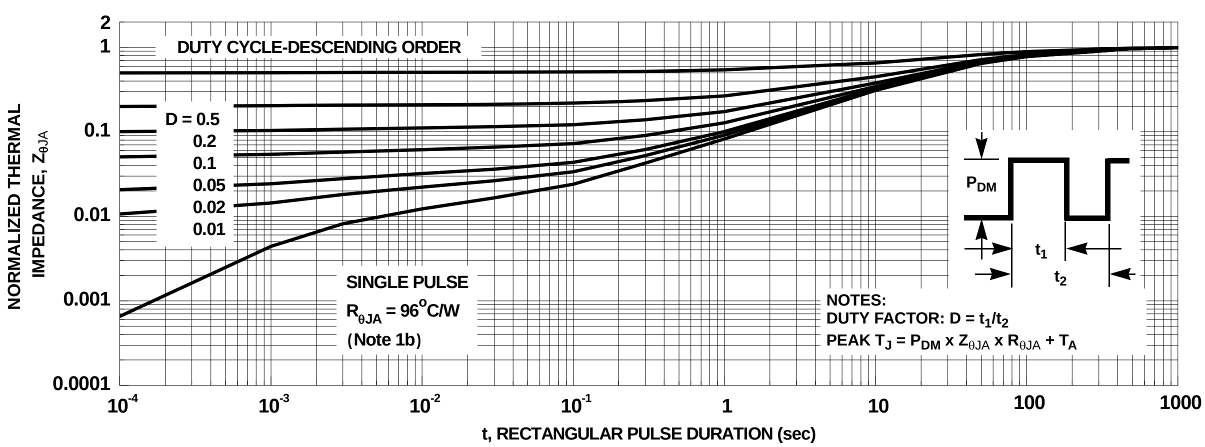


Figure 15. Transient Thermal Response Curve

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