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November 2013

FDD6N50F

N-Channel UniFETTM FRFET[®] MOSFET 500 V, 5.5 A, 1.15 Ω

Features

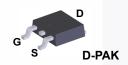
- $R_{DS(on)}$ = 950 m Ω (Typ.) @ V_{GS} = 10 V, I_D = 2.75 A
- Low Gate Charge (Typ. 15nC)
- Low C_{rss} (Typ. 6.3pF)
- · 100% Avalanche Tested
- · Improved dv/dt Capability
- · RoHS Compliant

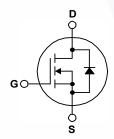
Applications

- LCD/LED/PDP TV
- Lighting
- · Uninterruptible Power Supply
- · AC-DC Power Supply

Description

UniFETTM MOSFET is Fairchild Semiconductor's high voltage MOSFET family based on planar stripe and DMOS technology. This MOSFET is tailored to reduce on-state resistance, and to provide better switching performance and higher avalanche energy strength. The body diode's reverse recovery performance of UniFET FRFET® MOSFET has been enhanced by lifetime control. Its trr is less than 100nsec and the reverse dv/dt immunity is 15V/ns while normal planar MOSFETs have over 200nsec and 4.5V/nsec respectively. Therefore, it can remove additional component and improve system reliability in certain applications in which the performance of MOSFET's body diode is significant. This device family is suitable for switching power converter applications such as power factor correction (PFC), flat panel display (FPD) TV power, ATX and electronic lamp ballasts.





MOSFET Maximum Ratings T_C = 25°C unless otherwise noted.

Symbol		Parameter		FDD6N50F	Unit
V_{DSS}	Drain to Source Voltage			500	V
V_{GSS}	Gate to Source Voltage	te to Source Voltage		±30	V
	Drain Current	- Continuous (T _C = 25°C)		5.5	А
ID	Diamounent	- Continuous (T _C = 100°C)		2.4	A
I _{DM}	Drain Current	Drain Current - Pulsed (Note		22	Α
E _{AS}	Single Pulsed Avalanche	Energy	(Note 2)	270	mJ
I _{AR}	Avalanche Current	valanche Current (No		5.5	Α
E _{AR}	Repetitive Avalanche En	etitive Avalanche Energy (Not		8.9	mJ
dv/dt	Peak Diode Recovery dv	/dt	(Note 3)	20	V/ns
Б	Dawar Diagination	(T _C = 25°C)		89	W
P_{D}	Power Dissipation	- Derate Above 25°C		0.71	W/°C
T _J , T _{STG}	Operating and Storage To	ting and Storage Temperature Range		-55 to +150	°C
T_L	Maximum Lead Tempera	ture for Soldering, 1/8" from Case fo	or 5 Seconds	300	°C

Thermal Characteristics

Symbol	Parameter	FDD6N50F	Unit
$R_{ heta JC}$	Thermal Resistance, Junction to Case, Max.		°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient, Max.	83	*C/VV

Package Marking and Ordering Information

Part Number	Top Mark	Package	Packing Method	Reel Size	Tape Width	Quantity
FDD6N50FTM	FDD6N50F	DPAK	Tape and Reel	330 mm	16 mm	2500 units

Electrical Characteristics $T_C = 25^{\circ}C$ unless otherwise noted.

Symbol	Parameter	Test Conditions	Min.	Тур.	Max.	Unit
Off Charac	cteristics					
BV _{DSS}	Drain to Source Breakdown Voltage	$I_D = 250 \mu A, V_{GS} = 0 V, T_J = 25^{\circ} C$	500	-	-	V
ΔBV _{DSS} / ΔΤ _J	Breakdown Voltage Temperature Coefficient	I _D = 250 μA, Referenced to 25°C	-	0.15	-	V/°C
1	Zero Gate Voltage Drain Current	V _{DS} = 500 V, V _{GS} = 0 V	-	-	10	^
I _{DSS} Zero Gate Voltage Drain Current	$V_{DS} = 400 \text{ V}, T_{C} = 125^{\circ}\text{C}$	-	-	100	μA	
I _{GSS}	Gate to Body Leakage Current	V _{GS} = ±30 V, V _{DS} = 0 V	-	-	±100	nA

On Characteristics

$V_{GS(th)}$	Gate Threshold Voltage	$V_{GS} = V_{DS}, I_{D} = 250 \mu\text{A}$	3.0	-	5.0	V
R _{DS(on)}	Static Drain to Source On Resistance	V_{GS} = 10 V, I_{D} = 2.75 A	-	0.95	1.15	Ω
9 _{FS}	Forward Transconductance	V _{DS} = 40 V, I _D = 2.75 A	-	4.3	-	S

Dynamic Characteristics

C _{iss}	Input Capacitance	V - 25 V V - 0 V		-	720	960	pF
C _{oss}	Output Capacitance	$V_{DS} = 25 \text{ V}, V_{GS} = 0 \text{ V},$ f = 1 MHz		-	85	115	pF
C _{rss}	Reverse Transfer Capacitance	1 - 1 101112		-\	6.3	9.5	pF
Q _{g(tot)}	Total Gate Charge at 10V	V _{DS} = 400 V, I _D = 6 A,		-	15	19.8	nC
Q_{gs}	Gate to Source Gate Charge	V _{GS} = 10 V		-	4.4	-	nC
Q_{gd}	Gate to Drain "Miller" Charge	(1)	Note 4)	-	6.1	-	nC

Switching Characteristics

t _{d(on)}	Turn-On Delay Time		-	17	44	ns
t _r		$V_{DD} = 250 \text{ V}, I_D = 6 \text{ A},$	-	28.3	66.6	ns
t _{d(off)}	Turn-Off Delay Time	V_{GS} = 10 V, R_G = 25 Ω	-	33.4	76.7	ns
t _f	Turn-Off Fall Time	(Note 4)	-	20.5	51	ns

Drain-Source Diode Characteristics

I _S	Maximum Continuous Drain to Source Diode Forward Current		-	-	5.5	Α
I _{SM}	Maximum Pulsed Drain to Source Diode Forward Current		-	-	22	Α
V_{SD}	Drain to Source Diode Forward Voltage	V _{GS} = 0 V, I _{SD} = 5.5 A	-	-	1.5	V
t _{rr}	Reverse Recovery Time	V _{GS} = 0 V, I _{SD} = 5.5 A,	-	85	-	ns
Q _{rr}	Reverse Recovery Charge	$dI_F/dt = 100 A/\mu s$	-	0.15	-	μC

Notes

- 1: Repetitive rating: pulse-width limited by maximum junction temperature.
- 2: L = 16 mH, I_{AS} = 5.5 A, V_{DD} = 50 V, R_G = 25 Ω , starting T_J = 25°C.
- 3: $I_{SD} \le 5.5$ A, di/dt ≤ 200 A/ μ s, $V_{DD} \le BV_{DSS}$, starting T_J = 25°C.
- 4: Essentially independent of operating temperature typical characteristics.

Typical Performance Characteristics

Figure 1. On-Region Characteristics

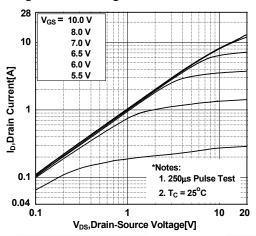


Figure 3. On-Resistance Variation vs.

Drain Current and Gate Voltage

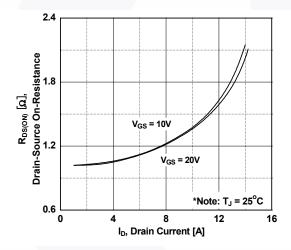


Figure 5. Capacitance Characteristics

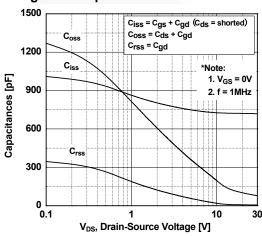


Figure 2. Transfer Characteristics

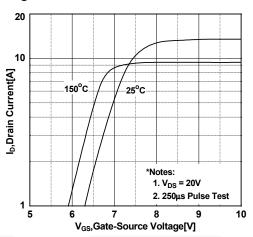


Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature

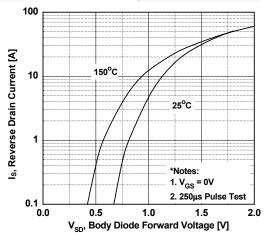
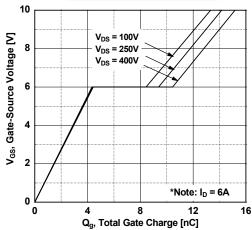


Figure 6. Gate Charge Characteristics



Typical Performance Characteristics (Continued)

Figure 7. Breakdown Voltage Variation vs. Temperature

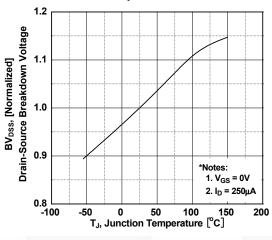


Figure 8. Maximum Safe Operating Area

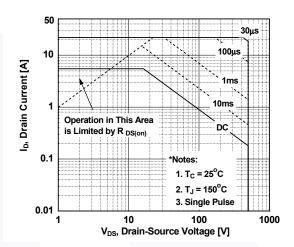


Figure 9. Maximum Drain Current vs. Case Temperature

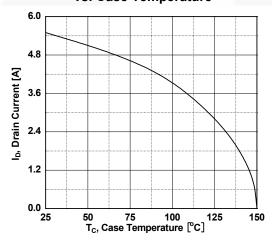
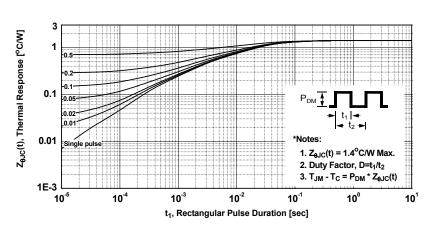


Figure 10. Transient Thermal Response Curve



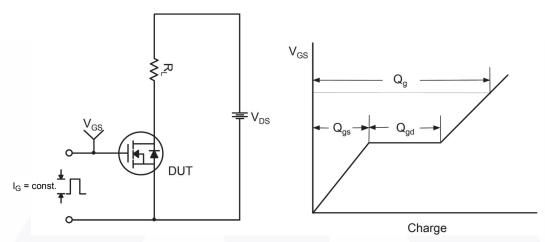


Figure 11. Gate Charge Test Circuit & Waveform

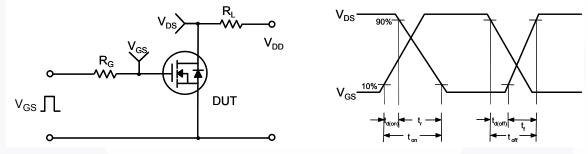


Figure 12. Resistive Switching Test Circuit & Waveforms

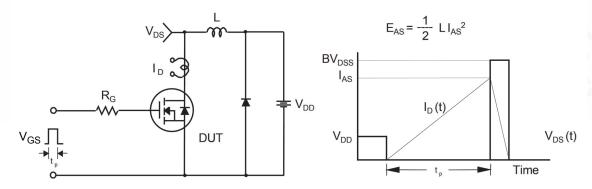


Figure 13. Unclamped Inductive Switching Test Circuit & Waveforms

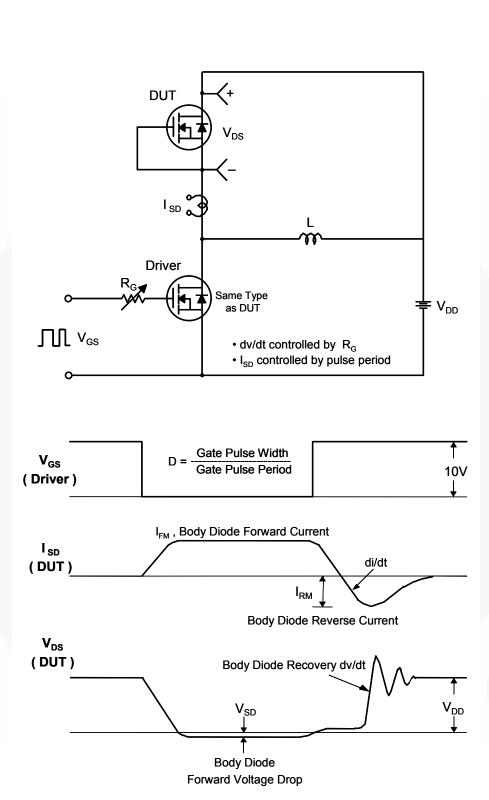


Figure 14. Peak Diode Recovery dv/dt Test Circuit & Waveforms

Mechanical Dimensions

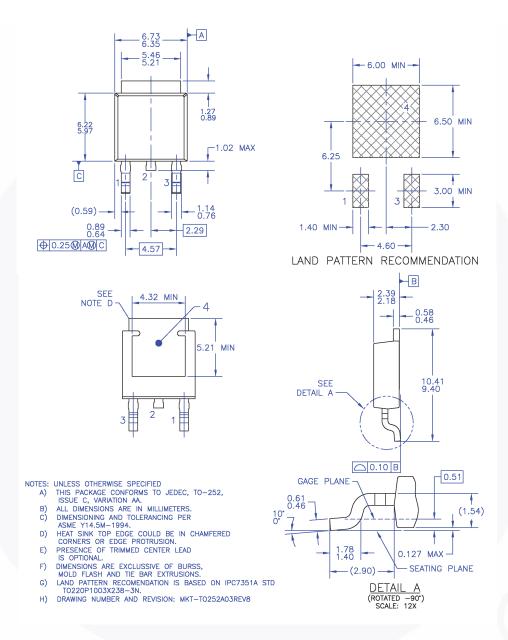


Figure 15. TO252 (D-PAK), Molded, 3-Lead, Option AA&AB

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