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# FDD8447L

## 40V N-Channel PowerTrench<sup>®</sup> MOSFET

### 40V, 50A, 8.5mΩ

#### Features

- Max  $r_{DS(on)}$  = 8.5mΩ at  $V_{GS}$  = 10V,  $I_D$  = 14A
- Max  $r_{DS(on)}$  = 11.0mΩ at  $V_{GS}$  = 4.5V,  $I_D$  = 11A
- Fast Switching
- RoHS Compliant

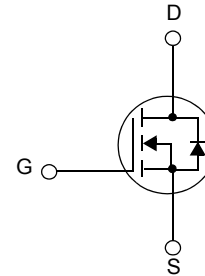
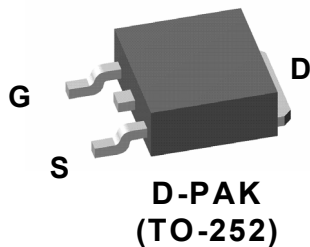


#### General Description

This N-Channel MOSFET has been produced using Fairchild Semiconductor's proprietary PowerTrench<sup>®</sup> technology to deliver low  $r_{DS(on)}$  and optimized  $BV_{DSS}$  capability to offer superior performance benefit in the application.

#### Applications

- Inverter
- Power Supplies



#### MOSFET Maximum Ratings $T_C = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Ratings	Units
$V_{DS}$	Drain to Source Voltage	40	V
$V_{GS}$	Gate to Source Voltage	±20	V
$I_D$	Drain Current -Continuous (Package limited) $T_C = 25^\circ\text{C}$	50	A
	-Continuous (Silicon limited) $T_C = 25^\circ\text{C}$	57	
	-Continuous $T_A = 25^\circ\text{C}$ (Note 1a)	15.2	
	-Pulsed	100	
$I_S$	Max Pulse Diode Current	100	A
$E_{AS}$	Drain-Source Avalanche Energy (Note 3)	153	mJ
$P_D$	Power Dissipation $T_C = 25^\circ\text{C}$	44	W
	$T_A = 25^\circ\text{C}$ (Note 1a)	3.1	
	$T_A = 25^\circ\text{C}$ (Note 1b)	1.3	
$T_J, T_{STG}$	Operating and Storage Junction Temperature Range	-55 to +150	$^\circ\text{C}$

#### Thermal Characteristics

$R_{\theta JC}$	Thermal Resistance, Junction to Case	2.8	$^\circ\text{C/W}$
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1a)	40	
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1b)	96	

#### Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
FDD8447L	FDD8447L	D-PAK(TO-252)	13"	16mm	2500 units

FDD8447L 40V N-Channel PowerTrench<sup>®</sup> MOSFET

## Electrical Characteristics $T_J = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
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### Off Characteristics

$BV_{DSS}$	Drain to Source Breakdown Voltage	$I_D = 250\mu\text{A}, V_{GS} = 0\text{V}$	40			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	$I_D = 250\mu\text{A}$ , referenced to $25^\circ\text{C}$		35		$\text{mV}/^\circ\text{C}$
$I_{DSS}$	Zero Gate Voltage Drain Current	$V_{DS} = 32\text{V}, V_{GS} = 0\text{V}$			1	$\mu\text{A}$
$I_{GSS}$	Gate to Source Leakage Current	$V_{GS} = \pm 20\text{V}, V_{DS} = 0\text{V}$			$\pm 100$	nA

### On Characteristics (Note 2)

$V_{GS(th)}$	Gate to Source Threshold Voltage	$V_{GS} = V_{DS}, I_D = 250\mu\text{A}$	1.0	1.9	3.0	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate to Source Threshold Voltage Temperature Coefficient	$I_D = 250\mu\text{A}$ , referenced to $25^\circ\text{C}$		-5		$\text{mV}/^\circ\text{C}$
$r_{DS(on)}$	Static Drain to Source On Resistance	$V_{GS} = 10\text{V}, I_D = 14\text{A}$		7.0	8.5	m $\Omega$
		$V_{GS} = 4.5\text{V}, I_D = 11\text{A}$		8.5	11.0	
		$V_{GS} = 10\text{V}, I_D = 14\text{A}, T_J = 125^\circ\text{C}$		10.4	14.0	
$g_{FS}$	Forward Transconductance	$V_{DS} = 5\text{V}, I_D = 14\text{A}$		58		S

### Dynamic Characteristics

$C_{iss}$	Input Capacitance	$V_{DS} = 20\text{V}, V_{GS} = 0\text{V}, f = 1\text{MHz}$		1970		pF
$C_{oss}$	Output Capacitance			250		pF
$C_{rss}$	Reverse Transfer Capacitance			150		pF
$R_g$	Gate Resistance	$f = 1\text{MHz}$		1.27		$\Omega$

### Switching Characteristics

$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = 20\text{V}, I_D = 1\text{A}$ $V_{GS} = 10\text{V}, R_{GEN} = 6\Omega$		12	21	ns
$t_r$	Rise Time			12	21	ns
$t_{d(off)}$	Turn-Off Delay Time			38	61	ns
$t_f$	Fall Time			9	18	ns
$Q_{g(TOT)}$	Total Gate Charge, $V_{GS} = 10\text{V}$	$V_{DD} = 20\text{V}, I_D = 14\text{A}$ $V_{GS} = 10\text{V}$		37	52	nC
$Q_{g(TOT)}$	Total Gate Charge, $V_{GS} = 5\text{V}$			20	28	nC
$Q_{gs}$	Gate to Source Gate Charge			6		nC
$Q_{gd}$	Gate to Drain "Miller" Charge			7		nC

### Drain-Source Diode Characteristics

$I_S$	Maximum Continuous Drain-Source Diode Forward Current (Note 1a)			2.6	A	
$V_{SD}$	Source to Drain Diode Forward Voltage	$V_{GS} = 0\text{V}, I_S = 14\text{A}$ (Note 2)		0.8	1.2	V
$t_{rr}$	Reverse Recovery Time	$I_F = 14\text{A}, di/dt = 100\text{A}/\mu\text{s}$		22		ns
$Q_{rr}$	Reverse Recovery Charge			11		nC

#### Notes:

- $R_{\theta JA}$  is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins.  $R_{\theta JC}$  is guaranteed by design while  $R_{\theta JA}$  is determined by the user's board design.
  - $40^\circ\text{C}/\text{W}$  when mounted on a 1 in<sup>2</sup> pad of 2 oz. copper
  - $96^\circ\text{C}/\text{W}$  when mounted on a minimum pad.
- Pulse Test: Pulse Width < 300 $\mu\text{s}$ , Duty cycle < 2.0%.
- Starting  $T_J = 25^\circ\text{C}$ ,  $L = 1\text{mH}$ ,  $I_{AS} = 17.5\text{A}$ ,  $V_{DD} = 40\text{V}$ ,  $V_{GS} = 10\text{V}$ .

## Typical Characteristics

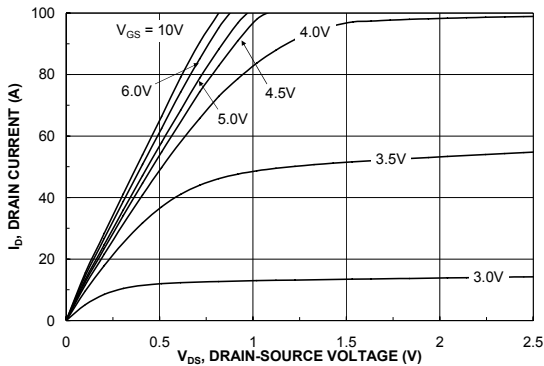


Figure 1. On-Region Characteristics

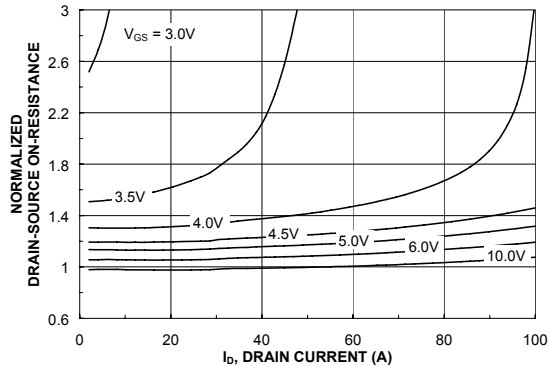


Figure 2. On-Resistance Variation with Drain Current and Gate Voltage

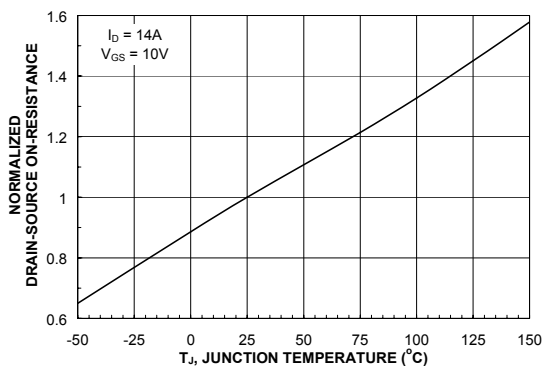


Figure 3. On-Resistance Variation with Temperature

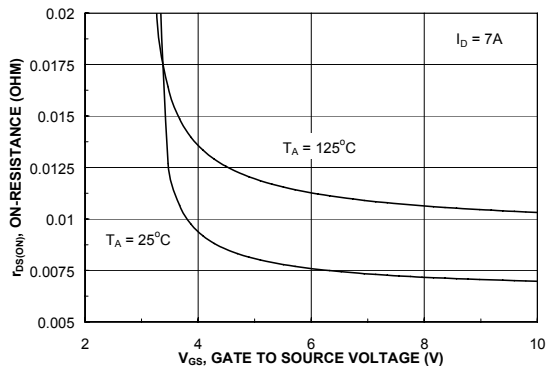


Figure 4. On-Resistance Variation with Gate-to-Source Voltage

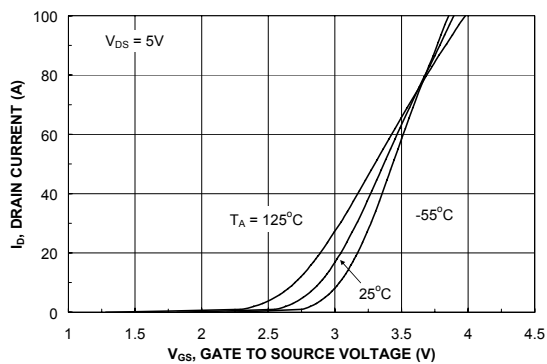


Figure 5. Transfer Characteristics

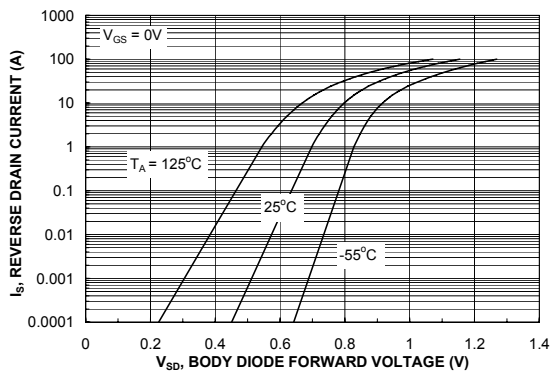


Figure 6. Body Diode Forward Voltage Variation with Source Current and Temperature

## Typical Characteristics

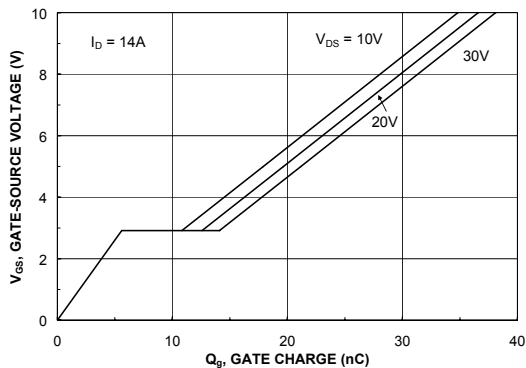


Figure 7. Gate Charge Characteristics

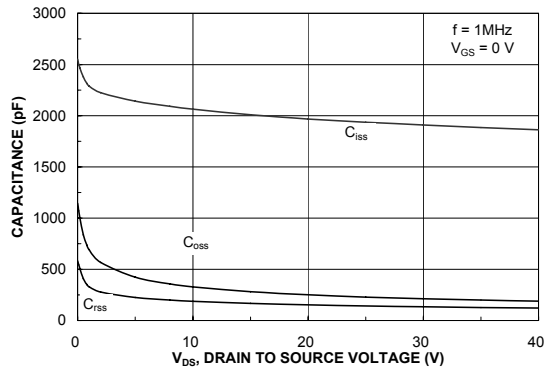


Figure 8. Capacitance Characteristics

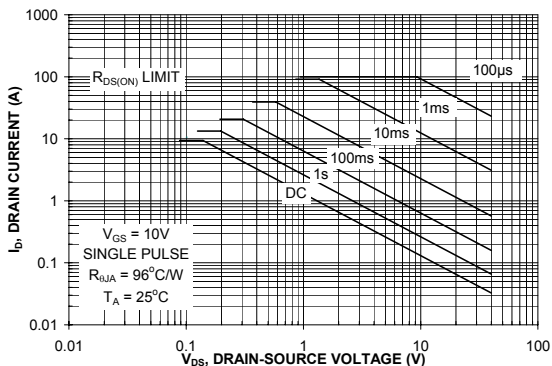


Figure 9. Maximum Safe Operating Area

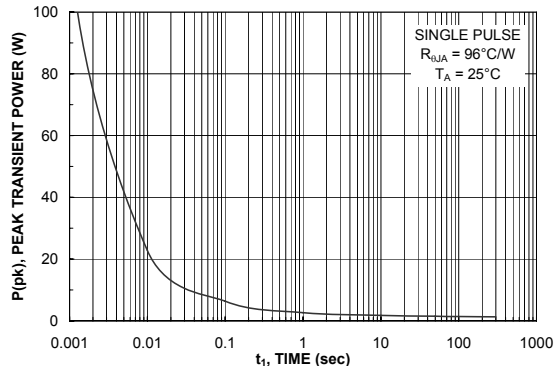


Figure 10. Single Pulse Maximum Power Dissipation

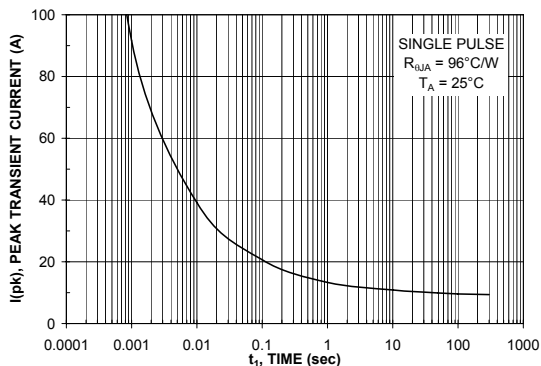


Figure 11. Single Pulse Maximum Peak Current

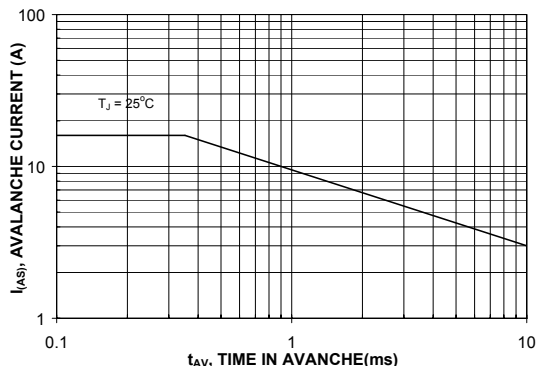
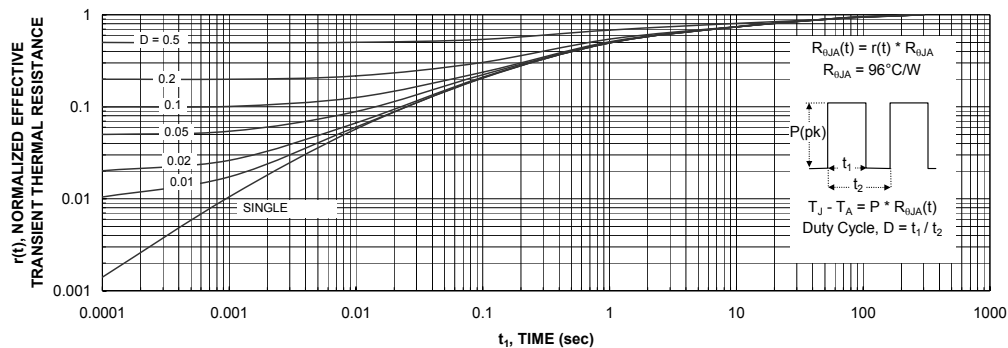


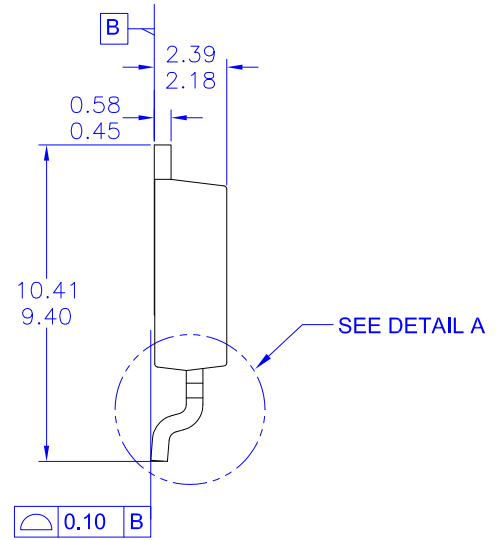
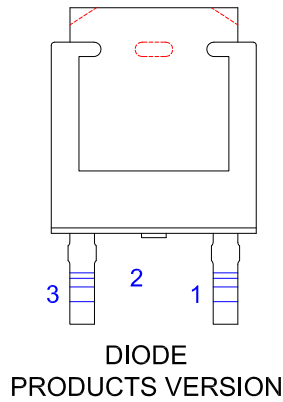
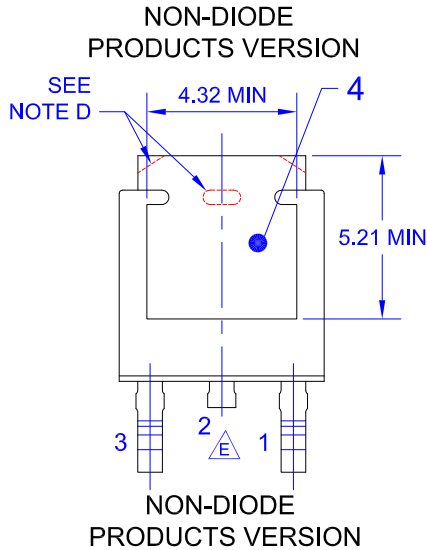
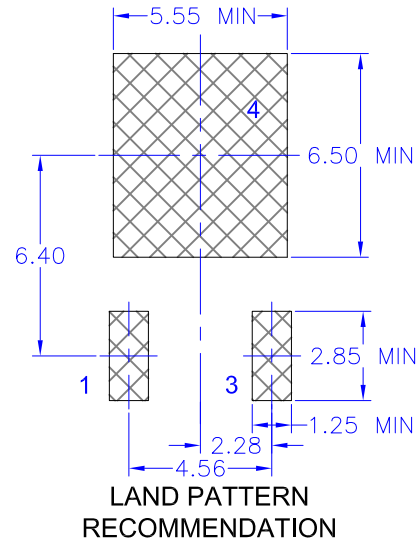
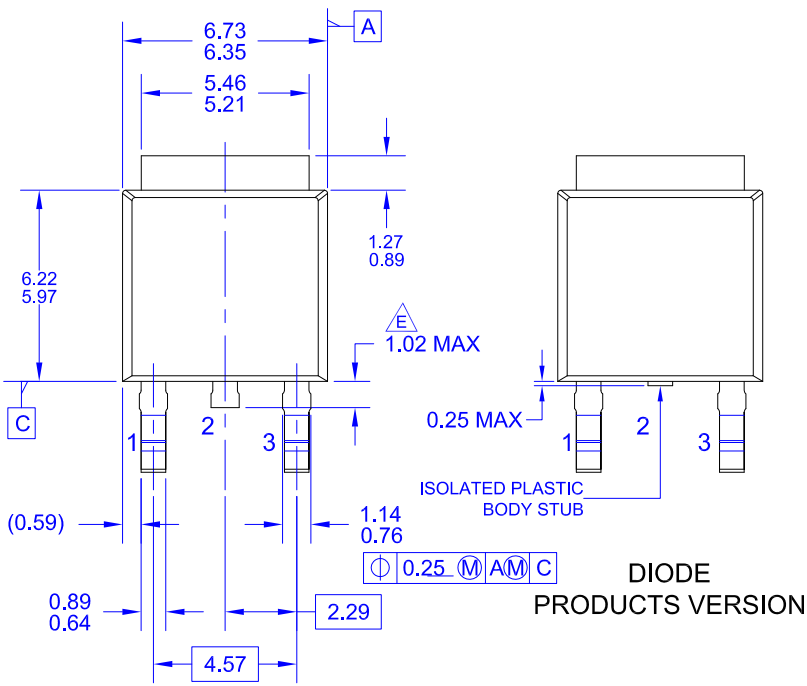
Figure 12. Unclamped Inductive Switching Capability

## Typical Characteristics



**Figure 13. Transient Thermal Response Curve**

Thermal characterization performed using the conditions described in Note 1b.  
 Transient thermal response will change depending on the circuit board design.



NOTES: UNLESS OTHERWISE SPECIFIED  
 A) THIS PACKAGE CONFORMS TO JEDEC, TO-252, ISSUE C, VARIATION AA.

B) ALL DIMENSIONS ARE IN MILLIMETERS.

C) DIMENSIONING AND TOLERANCING PER ASME Y14.5M-2009.

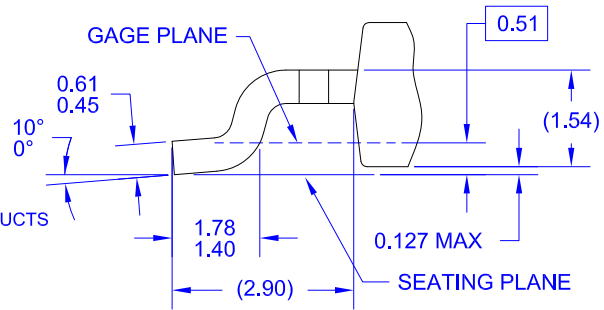
D) SUPPLIER DEPENDENT MOLD LOCKING HOLES OR CHAMFERED CORNERS OR EDGE PROTRUSION.

E) TRIMMED METAL CENTER LEAD IS PRESENT ON FOR NON-DIODE PRODUCTS

F) DIMENSIONS ARE EXCLUSIVE OF BURS, MOLD FLASH AND TIE BAR EXTRUSIONS.

G) LAND PATTERN RECOMMENDATION IS BASED ON IPC7351A STD TO228P991X239-3N.

H) DRAWING NUMBER AND REVISION: MKT-TO252A03REV11



**DETAIL A**  
(ROTATED -90°)  
SCALE: 12X



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