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# FDD86113LZ

## N-Channel Shielded Gate PowerTrench<sup>®</sup> MOSFET

100 V, 5.5 A, 104 mΩ

### Features

- Shielded Gate MOSFET Technology
- Max  $r_{DS(on)}$  = 104 mΩ at  $V_{GS} = 10$  V,  $I_D = 4.2$  A
- Max  $r_{DS(on)}$  = 156 mΩ at  $V_{GS} = 4.5$  V,  $I_D = 3.4$  A
- HBM ESD protection level > 6 kV typical (Note 4)
- High performance trench technology for extremely low  $r_{DS(on)}$
- High power and current handling capability in a widely used surface mount package
- 100% UIL Tested
- RoHS Compliant

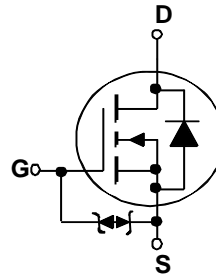
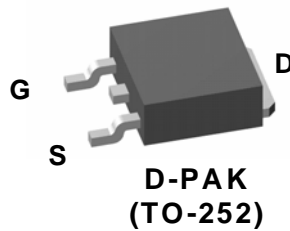


### General Description

This N-Channel logic Level MOSFETs are produced using Fairchild Semiconductor's advanced PowerTrench<sup>®</sup> process that incorporates Shielded Gate technology. This process has been optimized for the on-state resistance and yet maintain superior switching performance. G-S zener has been added to enhance ESD voltage level.

### Application

- DC-DC conversion



### MOSFET Maximum Ratings $T_C = 25$ °C unless otherwise noted

Symbol	Parameter	Ratings	Units
$V_{DS}$	Drain to Source Voltage	100	V
$V_{GS}$	Gate to Source Voltage	±20	V
$I_D$	Drain Current -Continuous $T_C = 25$ °C	5.5	A
	-Continuous $T_A = 25$ °C (Note 1a)	4.2	
	-Pulsed	15	
$E_{AS}$	Single Pulse Avalanche Energy (Note 3)	12	mJ
$P_D$	Power Dissipation $T_C = 25$ °C	29	W
	Power Dissipation $T_A = 25$ °C (Note 1a)	3.1	
$T_J, T_{STG}$	Operating and Storage Junction Temperature Range	-55 to +150	°C

### Thermal Characteristics

$R_{\theta JC}$	Thermal Resistance, Junction to Case (Note 1)	4.3	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1a)	96	

### Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
FDD86113LZ	FDD86113LZ	D-PAK(TO-252)	13 "	16 mm	2500 units

## Electrical Characteristics $T_J = 25\text{ }^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
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### Off Characteristics

$BV_{DSS}$	Drain to Source Breakdown Voltage	$I_D = 250\ \mu\text{A}, V_{GS} = 0\ \text{V}$	100			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	$I_D = 250\ \mu\text{A}$ , referenced to $25\text{ }^\circ\text{C}$		72		mV/ $^\circ\text{C}$
$I_{DSS}$	Zero Gate Voltage Drain Current	$V_{DS} = 80\ \text{V}, V_{GS} = 0\ \text{V}$			1	$\mu\text{A}$
$I_{GSS}$	Gate to Source Leakage Current	$V_{GS} = \pm 20\ \text{V}, V_{DS} = 0\ \text{V}$			$\pm 10$	$\mu\text{A}$

### On Characteristics

$V_{GS(th)}$	Gate to Source Threshold Voltage	$V_{GS} = V_{DS}, I_D = 250\ \mu\text{A}$	1	1.5	3	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate to Source Threshold Voltage Temperature Coefficient	$I_D = 250\ \mu\text{A}$ , referenced to $25\text{ }^\circ\text{C}$		-5		mV/ $^\circ\text{C}$
$r_{DS(on)}$	Static Drain to Source On Resistance	$V_{GS} = 10\ \text{V}, I_D = 4.2\ \text{A}$		87	104	m $\Omega$
		$V_{GS} = 4.5\ \text{V}, I_D = 3.4\ \text{A}$		116	156	
		$V_{GS} = 10\ \text{V}, I_D = 4.2\ \text{A}, T_J = 125\text{ }^\circ\text{C}$		142	170	
$g_{FS}$	Forward Transconductance	$V_{DS} = 5\ \text{V}, I_D = 4.2\ \text{A}$		9		S

### Dynamic Characteristics

$C_{iss}$	Input Capacitance	$V_{DS} = 50\ \text{V}, V_{GS} = 0\ \text{V}, f = 1\ \text{MHz}$		213	285	pF
$C_{oss}$	Output Capacitance			55	75	pF
$C_{riss}$	Reverse Transfer Capacitance			2.4	5	pF
$R_g$	Gate Resistance			1.4		$\Omega$

### Switching Characteristics

$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = 50\ \text{V}, I_D = 4.2\ \text{A}, V_{GS} = 10\ \text{V}, R_{GEN} = 6\ \Omega$		3.6	10	ns
$t_r$	Rise Time			1.3	10	ns
$t_{d(off)}$	Turn-Off Delay Time			9.7	20	ns
$t_f$	Fall Time			1.6	10	ns
$Q_{g(TOT)}$	Total Gate Charge		$V_{GS} = 0\ \text{V}$ to $10\ \text{V}$	$V_{DD} = 50\ \text{V}, I_D = 4.2\ \text{A}$	3.7	6
$Q_{g(TOT)}$	Total Gate Charge	$V_{GS} = 0\ \text{V}$ to $4.5\ \text{V}$	1.9		3	
$Q_{gs}$	Gate to Source Charge		0.6			nC
$Q_{gd}$	Gate to Drain "Miller" Charge		0.7			nC

### Drain-Source Diode Characteristics

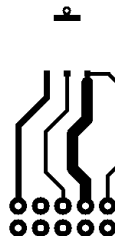
$V_{SD}$	Source to Drain Diode Forward Voltage	$V_{GS} = 0\ \text{V}, I_S = 4.2\ \text{A}$ (Note 2)		0.88	1.3	V
		$V_{GS} = 0\ \text{V}, I_S = 1.7\ \text{A}$ (Note 2)		0.80	1.2	
$t_{rr}$	Reverse Recovery Time	$I_F = 4.2\ \text{A}, di/dt = 100\ \text{A}/\mu\text{s}$		31	49	ns
$Q_{rr}$	Reverse Recovery Charge			20	33	nC

#### NOTES:

- $R_{\theta JA}$  is determined with the device mounted on a 1 in<sup>2</sup> pad 2 oz copper pad on a 1.5 x 1.5 in. board of FR-4 material.  $R_{\theta JC}$  is guaranteed by design while  $R_{\theta CA}$  is determined by the user's board design.



a)  $40\text{ }^\circ\text{C}/\text{W}$  when mounted on a 1 in<sup>2</sup> pad of 2 oz copper



b)  $96\text{ }^\circ\text{C}/\text{W}$  when mounted on a minimum pad of 2 oz copper

2. Pulse Test: Pulse Width < 300  $\mu\text{s}$ , Duty cycle < 2.0 %.

3. Starting  $T_J = 25\text{ }^\circ\text{C}$ ,  $L = 1\ \text{mH}$ ,  $I_{AS} = 5\ \text{A}$ ,  $V_{DD} = 90\ \text{V}$ ,  $V_{GS} = 10\ \text{V}$ .

4. The diode connected between gate and source serves only as protection against ESD. No gate overvoltage rating is implied.

**Typical Characteristics**  $T_J = 25\text{ }^\circ\text{C}$  unless otherwise noted

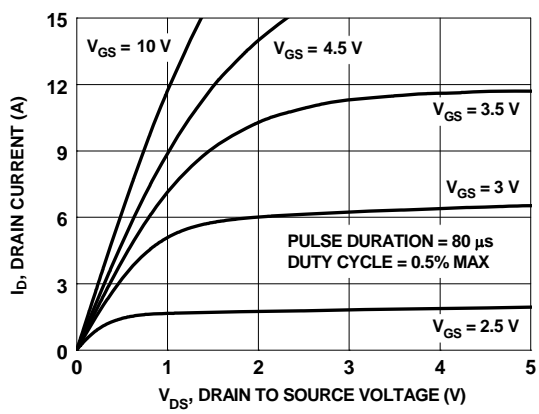


Figure 1. On-Region Characteristics

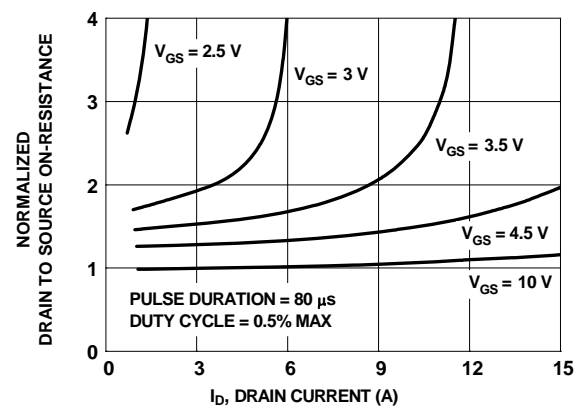


Figure 2. Normalized On-Resistance vs Drain Current and Gate Voltage

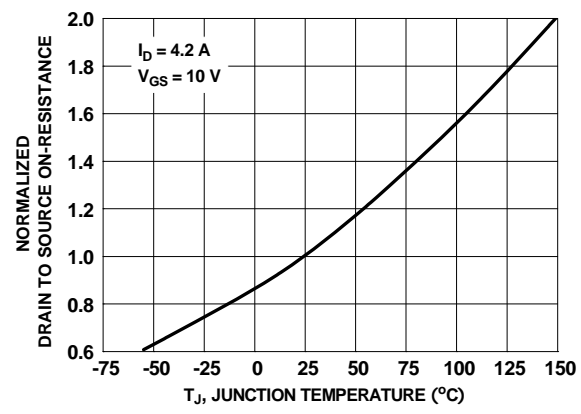


Figure 3. Normalized On-Resistance vs Junction Temperature

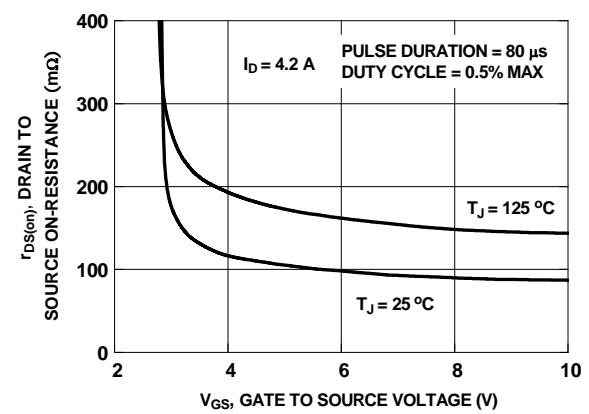


Figure 4. On-Resistance vs Gate to Source Voltage

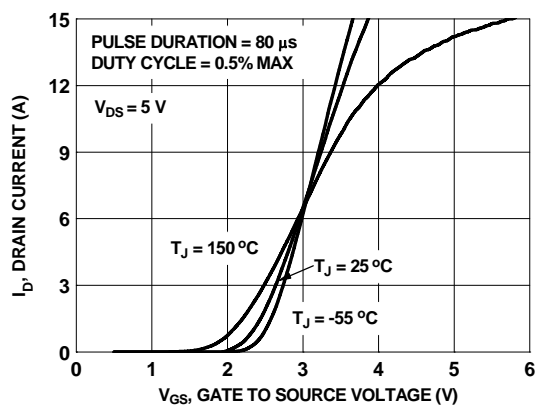


Figure 5. Transfer Characteristics

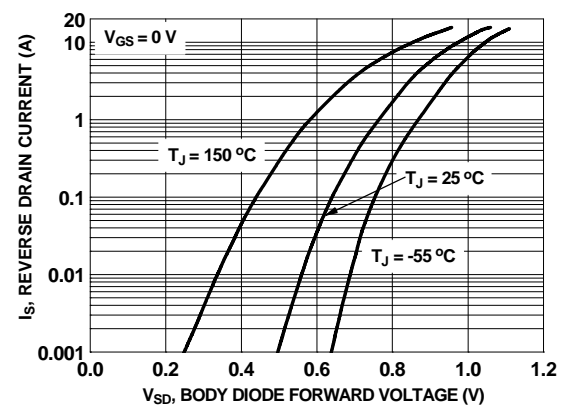
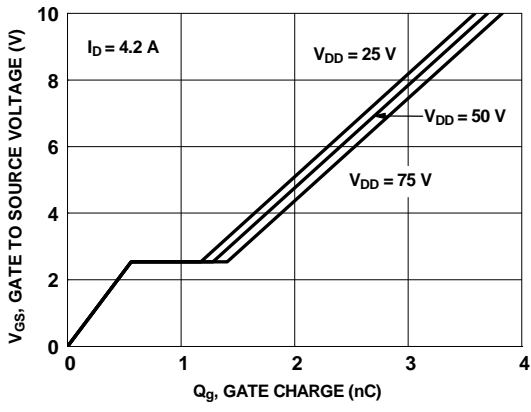
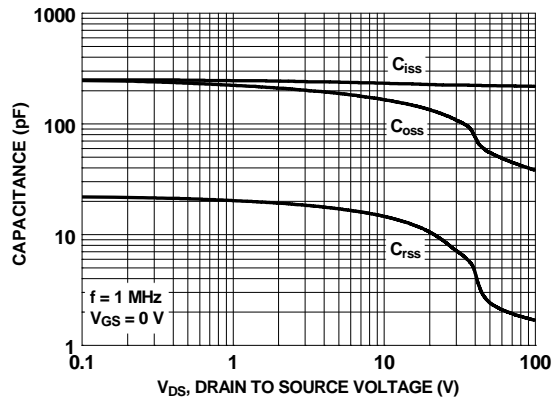


Figure 6. Source to Drain Diode Forward Voltage vs Source Current

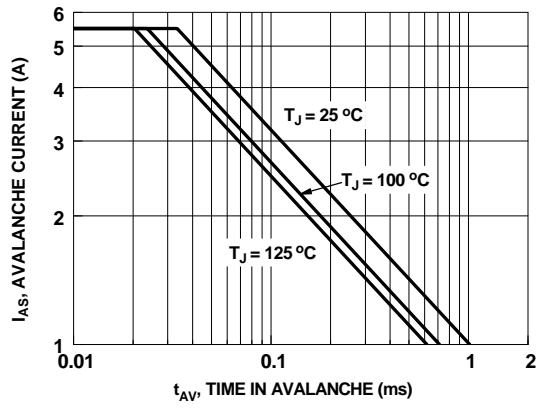
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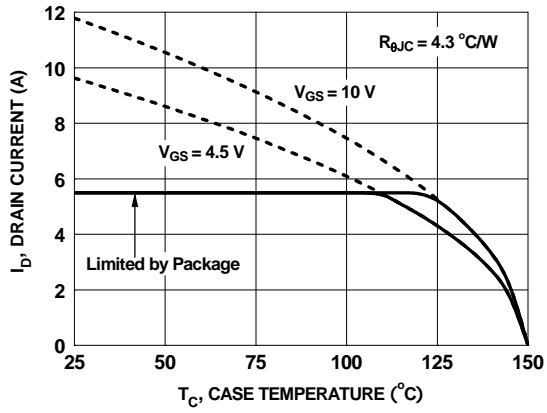
**Figure 7. Gate Charge Characteristics**



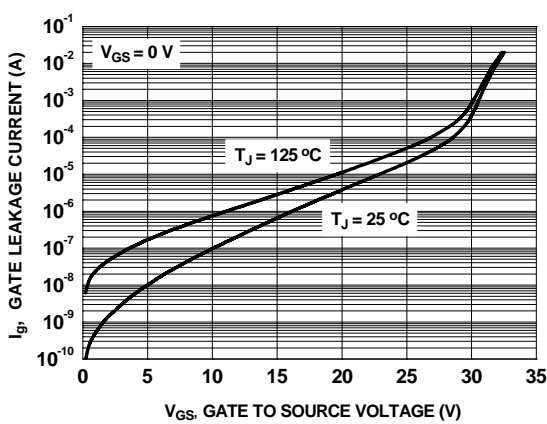
**Figure 8. Capacitance vs Drain to Source Voltage**



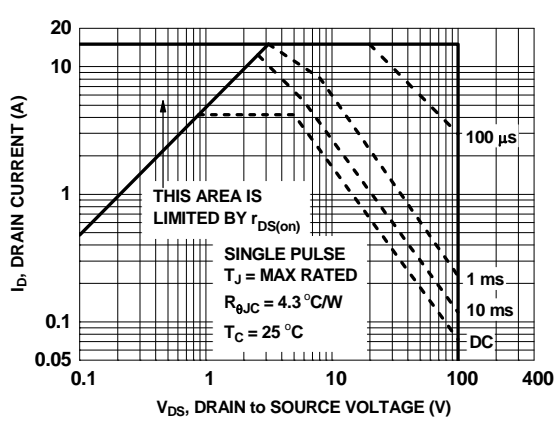
**Figure 9. Unclamped Inductive Switching Capability**



**Figure 10. Maximum Continuous Drain Current vs Case Temperature**

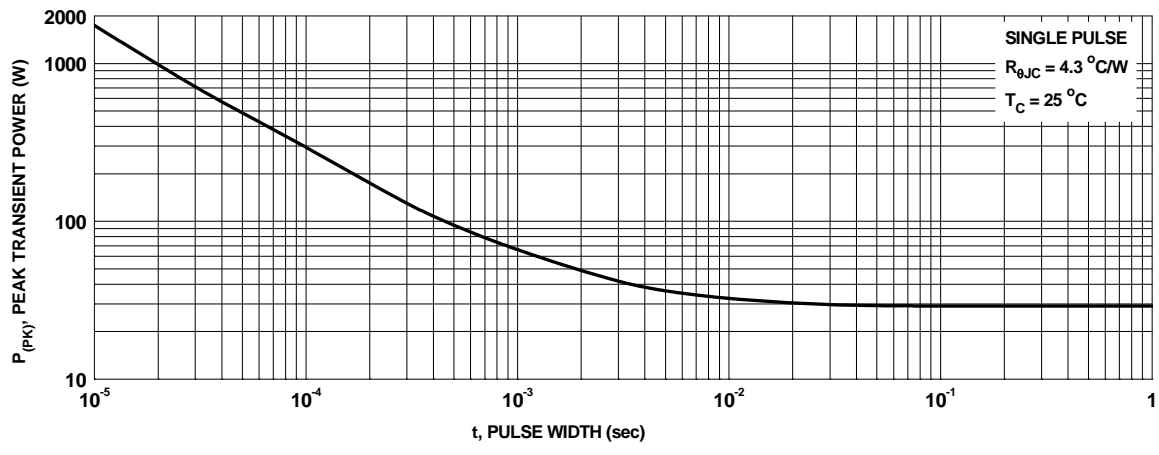


**Figure 11. Gate Leakage Current vs Gate to Source Voltage**

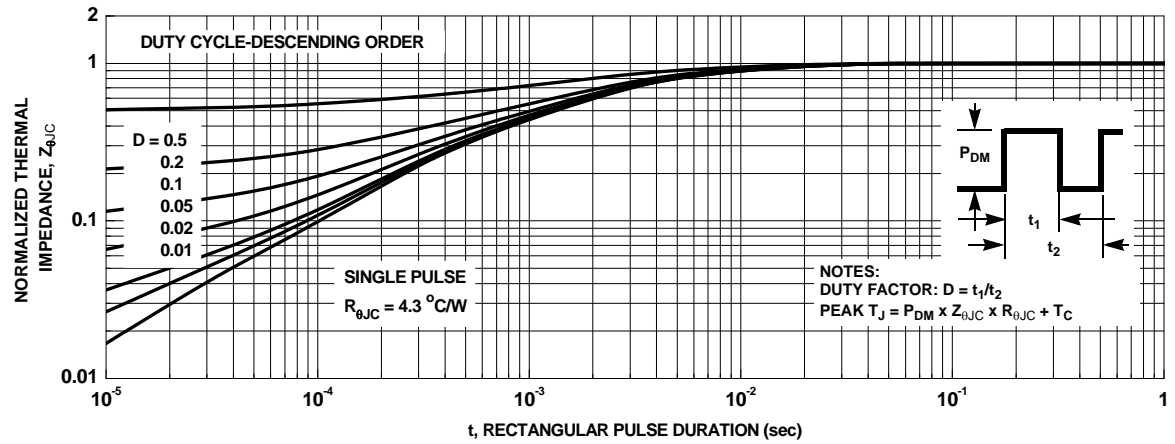


**Figure 12. Forward Bias Safe Operating Area**

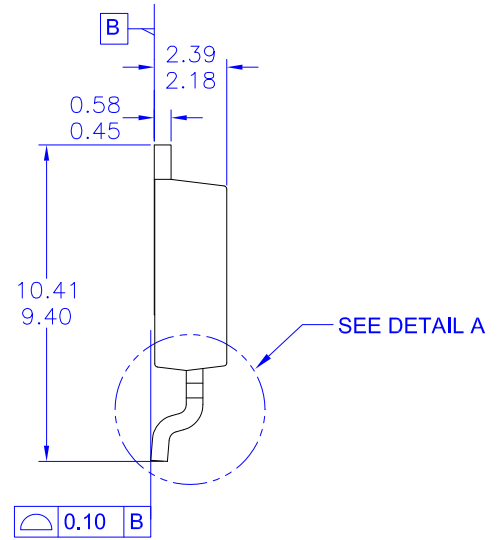
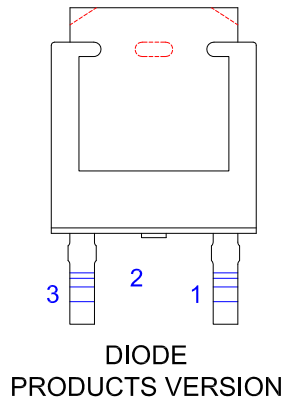
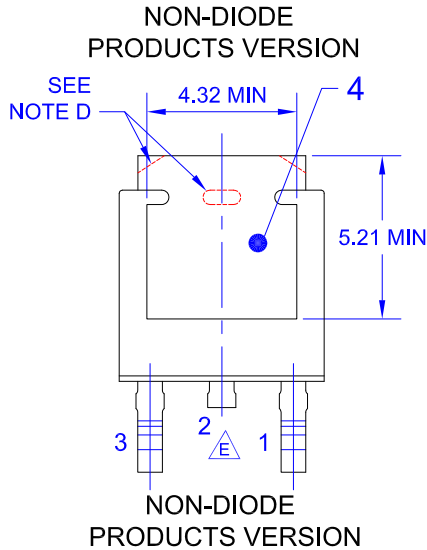
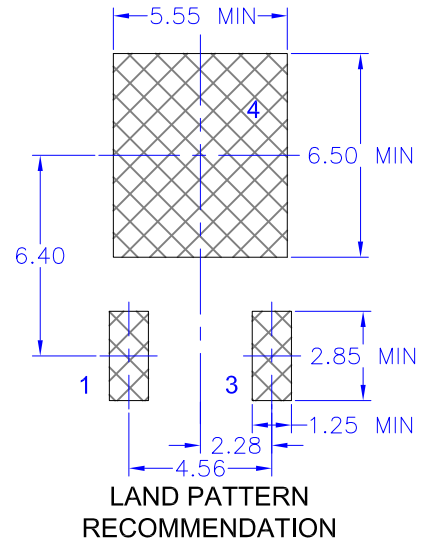
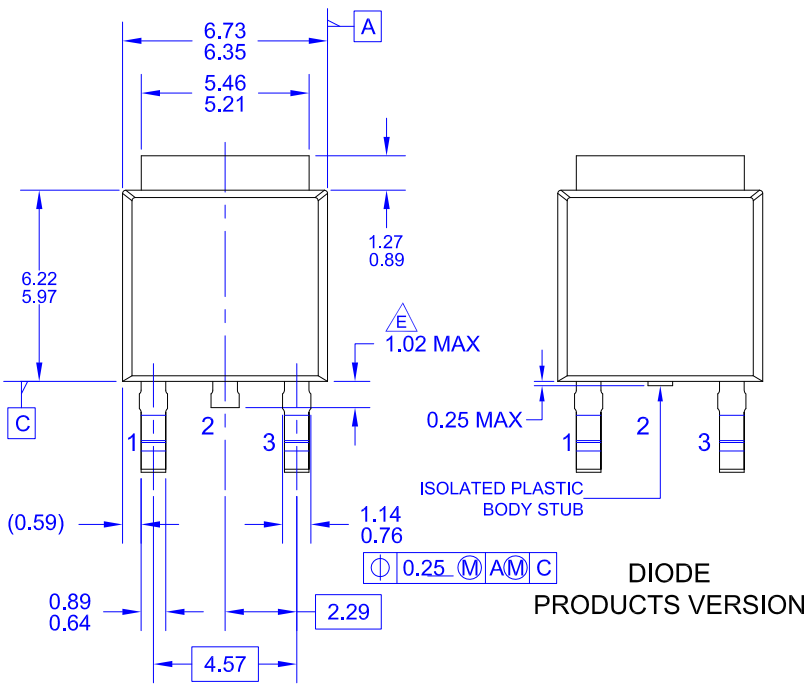
**Typical Characteristics**  $T_J = 25\text{ }^\circ\text{C}$  unless otherwise noted



**Figure 13. Single Pulse Maximum Power Dissipation**



**Figure 14. Junction-to-Case Transient Thermal Response Curve**



NOTES: UNLESS OTHERWISE SPECIFIED  
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B) ALL DIMENSIONS ARE IN MILLIMETERS.

C) DIMENSIONING AND TOLERANCING PER ASME Y14.5M-2009.

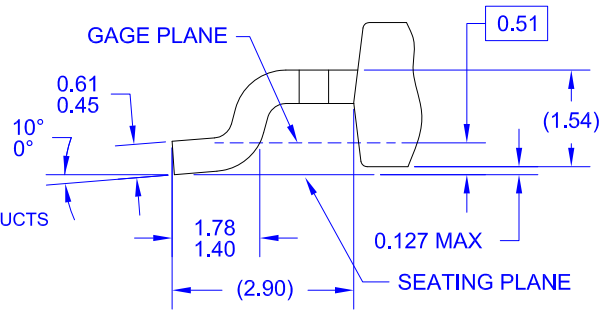
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E) TRIMMED METAL CENTER LEAD IS PRESENT ON FOR NON-DIODE PRODUCTS

F) DIMENSIONS ARE EXCLUSIVE OF BURS, MOLD FLASH AND TIE BAR EXTRUSIONS.

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