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FDD86250

N-Channel Shielded Gate PowerTrench[®] MOSFET

150 V, 51 A, 22 mΩ

Features

- Shielded Gate MOSFET Technology
- Max $r_{DS(on)}$ = 22 mΩ at $V_{GS} = 10\text{ V}$, $I_D = 8\text{ A}$
- Max $r_{DS(on)}$ = 31 mΩ at $V_{GS} = 6\text{ V}$, $I_D = 6.5\text{ A}$
- 100% UIL tested
- RoHS Compliant

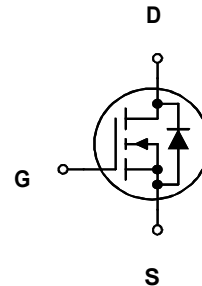
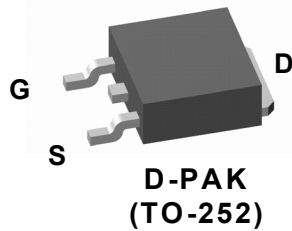


General Description

This N-Channel MOSFET is produced using Fairchild Semiconductor's advanced PowerTrench[®] process that incorporates Shielded Gate technology. This process has been optimized for the on-state resistance and yet maintain superior switching performance.

Application

- DC - DC Conversion



MOSFET Maximum Ratings $T_C = 25\text{ °C}$ unless otherwise noted.

Symbol	Parameter	Ratings	Units
V_{DS}	Drain to Source Voltage	150	V
V_{GS}	Gate to Source Voltage	±20	V
I_D	Drain Current -Continuous	$T_C = 25\text{ °C}$ (Note 5)	51
	-Continuous	$T_C = 100\text{ °C}$ (Note 5)	27
	-Continuous	$T_A = 25\text{ °C}$ (Note 1a)	8
	-Pulsed	(Note 4)	164
E_{AS}	Single Pulse Avalanche Energy	(Note 3)	180
P_D	Power Dissipation	$T_C = 25\text{ °C}$	132
	Power Dissipation	$T_A = 25\text{ °C}$ (Note 1a)	3.1
T_J, T_{STG}	Operating and Storage Junction Temperature Range	-55 to +150	°C

Thermal Characteristics

$R_{\theta JC}$	Thermal Resistance, Junction-to-Case	0.94	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient (Note 1a)	40	

Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
FDD86250	FDD86250	D-PAK(TO-252)	13 "	16 mm	2500 units

Electrical Characteristics $T_J = 25\text{ }^\circ\text{C}$ unless otherwise noted.

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
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Off Characteristics

BV_{DSS}	Drain to Source Breakdown Voltage	$I_D = 250\text{ }\mu\text{A}, V_{GS} = 0\text{ V}$	150			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	$I_D = 250\text{ }\mu\text{A}$, referenced to $25\text{ }^\circ\text{C}$		106		$\text{mV}/^\circ\text{C}$
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = 120\text{ V}, V_{GS} = 0\text{ V}$			1	μA
I_{GSS}	Gate to Source Leakage Current	$V_{GS} = \pm 20\text{ V}, V_{DS} = 0\text{ V}$			± 100	nA

On Characteristics

$V_{GS(th)}$	Gate to Source Threshold Voltage	$V_{GS} = V_{DS}, I_D = 250\text{ }\mu\text{A}$	2.0	2.9	4.0	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate to Source Threshold Voltage Temperature Coefficient	$I_D = 250\text{ }\mu\text{A}$, referenced to $25\text{ }^\circ\text{C}$		-10		$\text{mV}/^\circ\text{C}$
$r_{DS(on)}$	Static Drain to Source On Resistance	$V_{GS} = 10\text{ V}, I_D = 8\text{ A}$		18.4	22	m Ω
		$V_{GS} = 6\text{ V}, I_D = 6.5\text{ A}$		21.4	31	
		$V_{GS} = 10\text{ V}, I_D = 8\text{ A}, T_J = 125\text{ }^\circ\text{C}$		35.8	45	
g_{FS}	Forward Transconductance	$V_{DS} = 10\text{ V}, I_D = 8\text{ A}$		28		S

Dynamic Characteristics

C_{iss}	Input Capacitance	$V_{DS} = 75\text{ V}, V_{GS} = 0\text{ V},$ $f = 1\text{ MHz}$		1585	2110	pF
C_{oss}	Output Capacitance			167	225	pF
C_{rss}	Reverse Transfer Capacitance			7	15	pF
R_g	Gate Resistance			0.6		Ω

Switching Characteristics

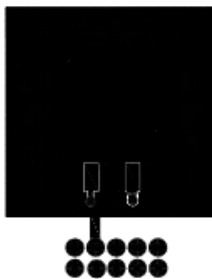
$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = 75\text{ V}, I_D = 8\text{ A},$ $V_{GS} = 10\text{ V}, R_{GEN} = 6\text{ }\Omega$		11.2	20	ns	
t_r	Rise Time			3.7	10	ns	
$t_{d(off)}$	Turn-Off Delay Time			20	32	ns	
t_f	Fall Time			4	10	ns	
Q_g	Total Gate Charge		$V_{GS} = 0\text{ V to } 10\text{ V}$		23	33	nC
Q_g	Total Gate Charge	$V_{GS} = 0\text{ V to } 5\text{ V}$	$V_{DD} = 75\text{ V},$ $I_D = 8\text{ A}$		12.8	18	nC
Q_{gs}	Gate to Source Charge				6.7		nC
Q_{gd}	Gate to Drain "Miller" Charge				4.7		nC

Drain-Source Diode Characteristics

V_{SD}	Source-Drain Diode Forward Voltage	$V_{GS} = 0\text{ V}, I_S = 8\text{ A}$ (Note 2)		0.78	1.3	V
		$V_{GS} = 0\text{ V}, I_S = 2.6\text{ A}$ (Note 2)		0.73	1.2	
t_{rr}	Reverse Recovery Time	$I_F = 8\text{ A}, di/dt = 100\text{ A}/\mu\text{s}$		71	113	ns
Q_{rr}	Reverse Recovery Charge			104	166	nC

Notes:

- 1: $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design while $R_{\theta JA}$ is determined by the user's board design.



a) $40\text{ }^\circ\text{C/W}$ when mounted on a 1 in^2 pad of 2 oz. copper



b) $96\text{ }^\circ\text{C/W}$ when mounted on a minimum pad

2: Pulse Test: Pulse Width < $300\text{ }\mu\text{s}$, Duty cycle < 2.0%.

3: Starting $T_J = 25\text{ }^\circ\text{C}$, $L = 1.0\text{ mH}$, $I_{AS} = 19\text{ A}$, $V_{DD} = 135\text{ V}$, $V_{GS} = 10\text{ V}$.

4: Pulsed I_D please refer to Fig 11 SOA graph for more details.

5: Computed continuous current limited to Max Junction Temperature only, actual continuous current will be limited by thermal & electro-mechanical application board design.

Typical Characteristics $T_J = 25\text{ }^\circ\text{C}$ unless otherwise noted.

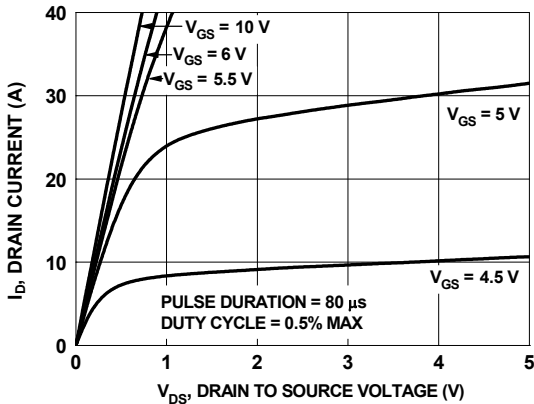


Figure 1. On-Region Characteristics

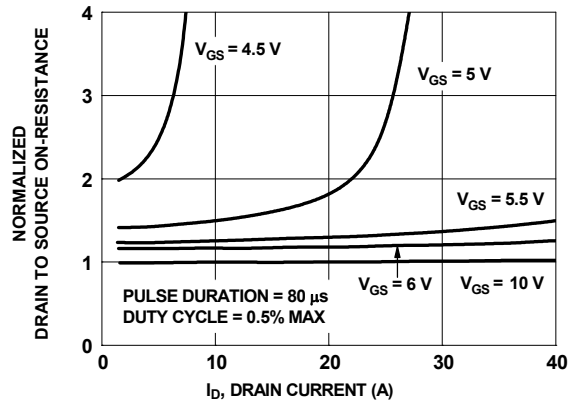


Figure 2. Normalized On-Resistance vs. Drain Current and Gate Voltage

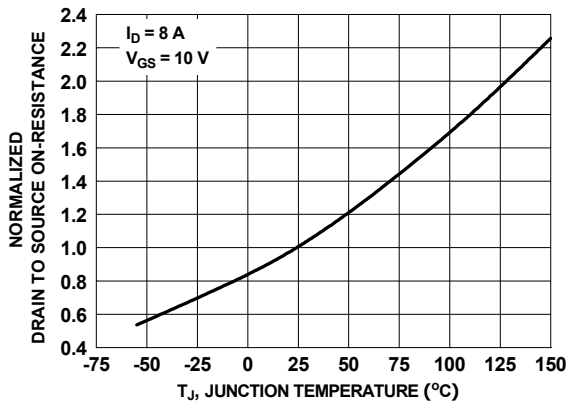


Figure 3. Normalized On-Resistance vs. Junction Temperature

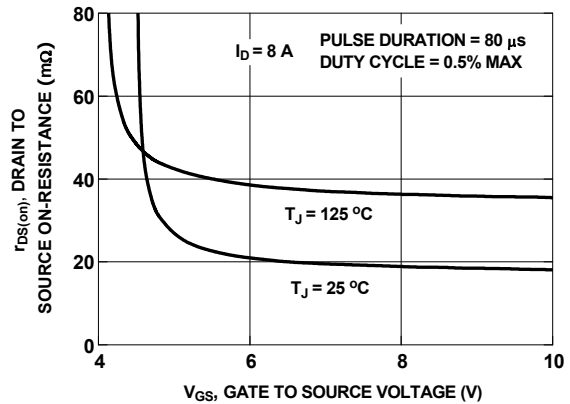


Figure 4. On-Resistance vs. Gate to Source Voltage

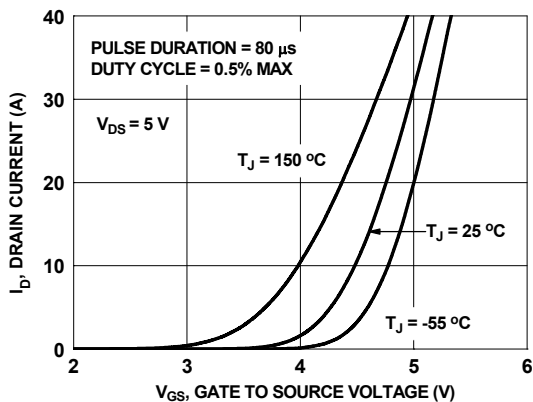


Figure 5. Transfer Characteristics

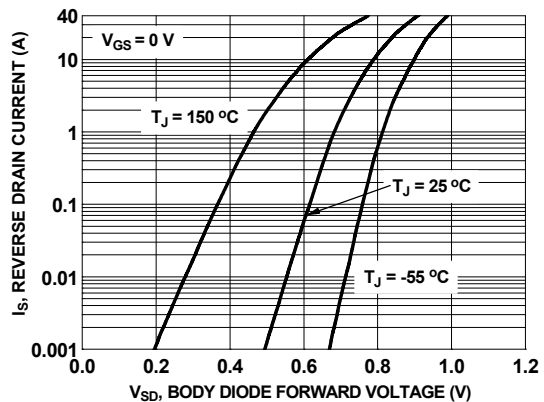


Figure 6. Source to Drain Diode Forward Voltage vs. Source Current

Typical Characteristics $T_J = 25^\circ\text{C}$ unless otherwise noted.

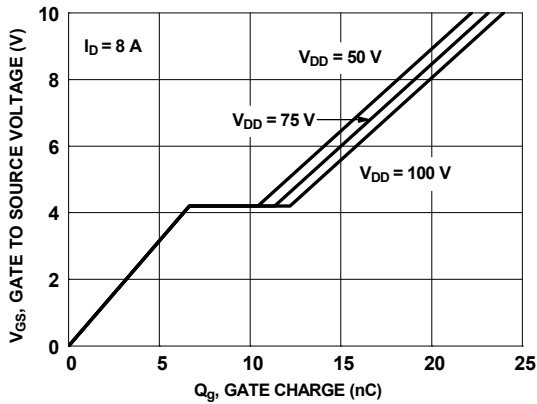


Figure 7. Gate Charge Characteristics

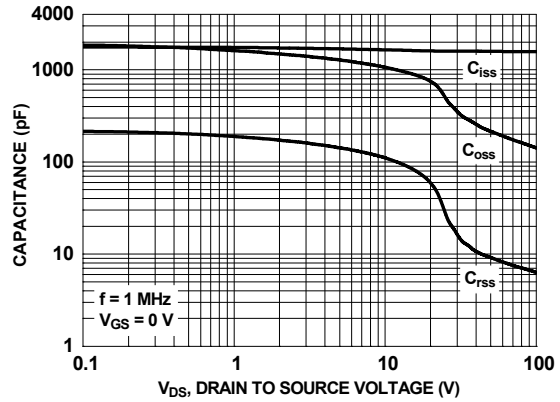


Figure 8. Capacitance vs. Drain to Source Voltage

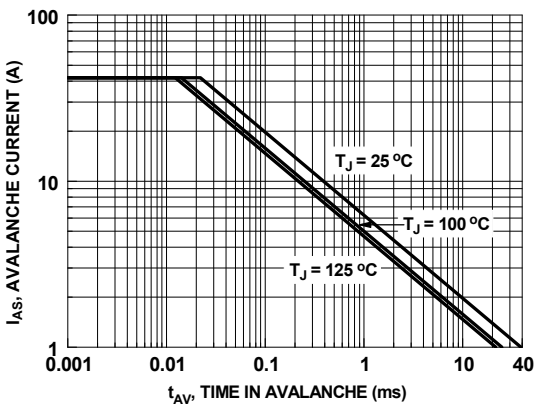


Figure 9. Unclamped Inductive Switching Capability

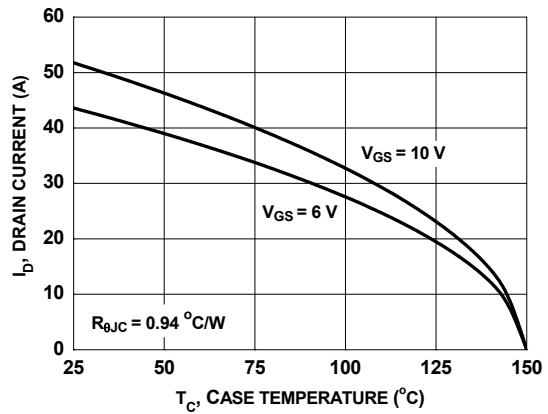


Figure 10. Maximum Continuous Drain Current vs. Case Temperature

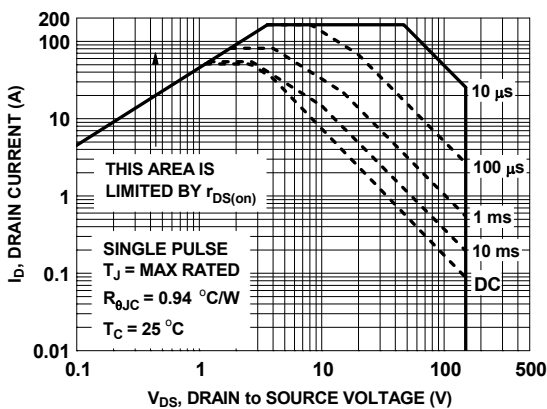


Figure 11. Forward Bias Safe Operating Area

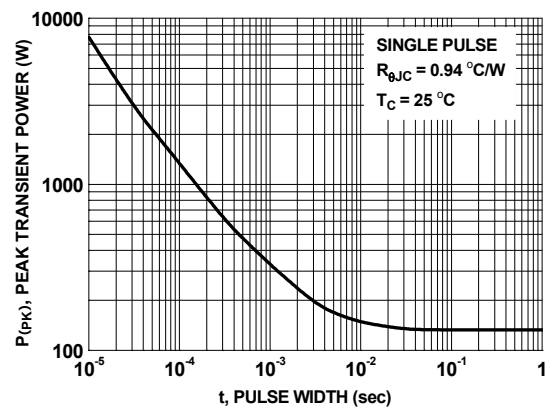


Figure 12. Single Pulse Maximum Power Dissipation

Typical Characteristics $T_J = 25\text{ }^\circ\text{C}$ unless otherwise noted.

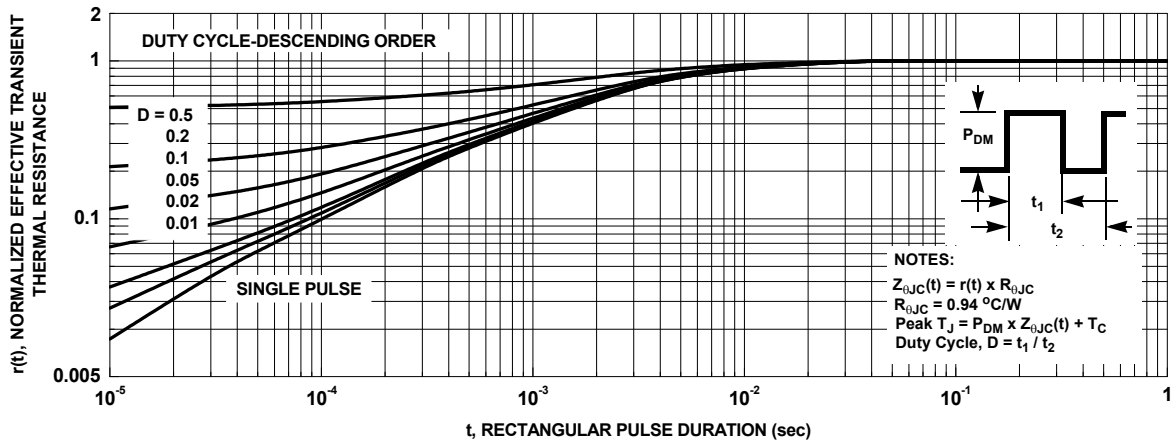
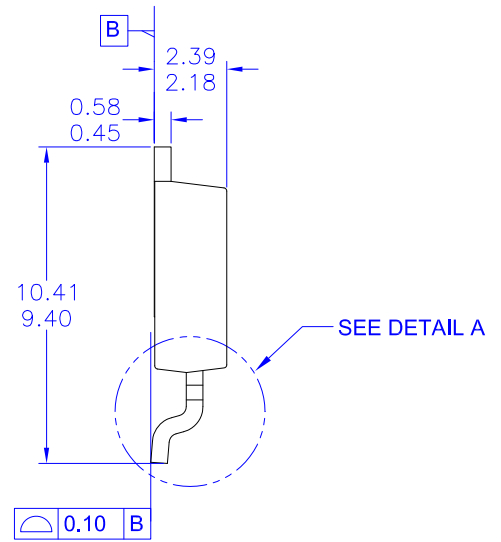
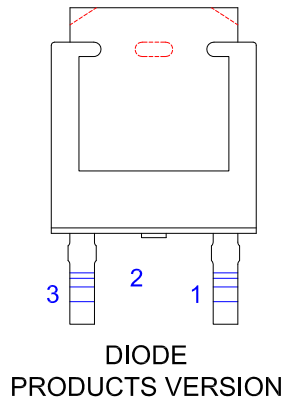
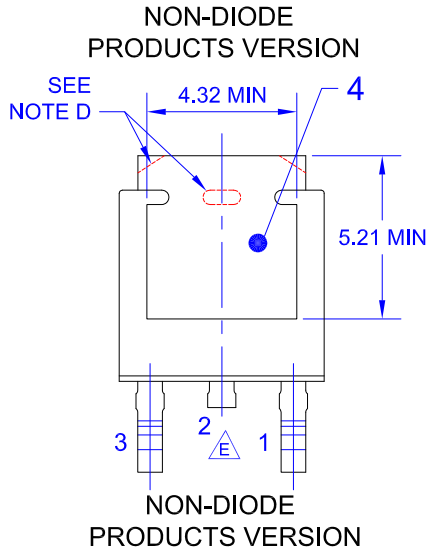
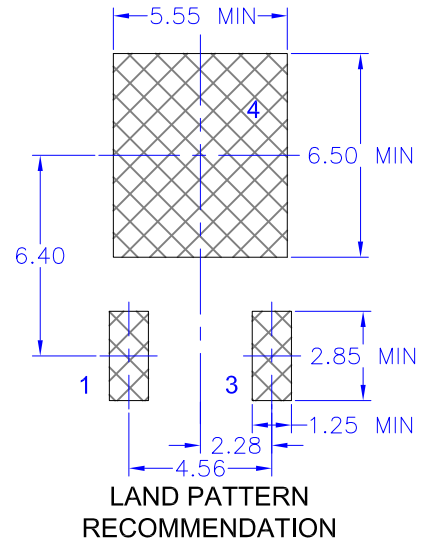
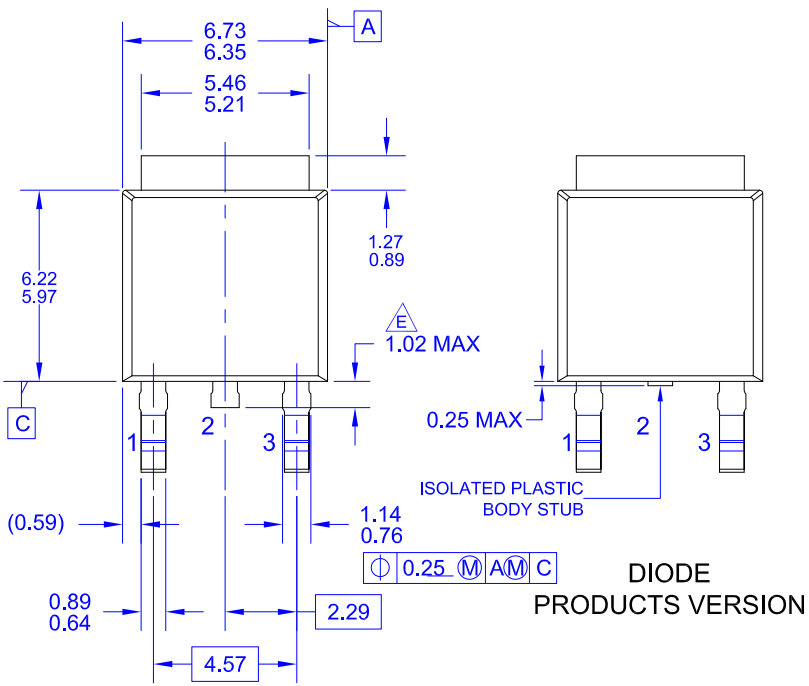


Figure 13. Junction-to-Case Transient Thermal Response Curve



NOTES: UNLESS OTHERWISE SPECIFIED
 A) THIS PACKAGE CONFORMS TO JEDEC, TO-252, ISSUE C, VARIATION AA.

B) ALL DIMENSIONS ARE IN MILLIMETERS.

C) DIMENSIONING AND TOLERANCING PER ASME Y14.5M-2009.

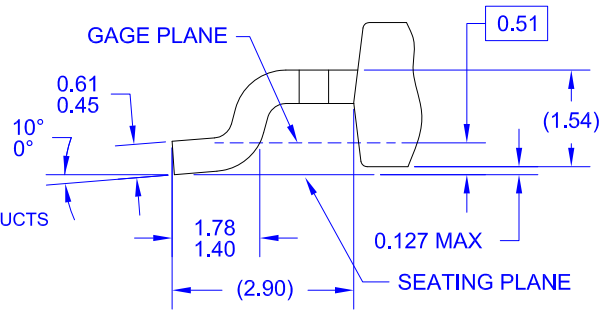
D) SUPPLIER DEPENDENT MOLD LOCKING HOLES OR CHAMFERED CORNERS OR EDGE PROTRUSION.

E) TRIMMED METAL CENTER LEAD IS PRESENT ON FOR NON-DIODE PRODUCTS

F) DIMENSIONS ARE EXCLUSIVE OF BURS, MOLD FLASH AND TIE BAR EXTRUSIONS.

G) LAND PATTERN RECOMMENDATION IS BASED ON IPC7351A STD TO228P991X239-3N.

H) DRAWING NUMBER AND REVISION: MKT-TO252A03REV11



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