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FAIRCHILD

March 2015

# FDD8878 / FDU8878
# N-Channel PowerTrench® MOSFET
## 30V, 40A, 15mΩ

## Features

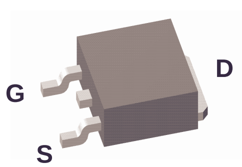
- $r_{DS(ON)}$ = 15mΩ, $V_{GS}$ = 10V, $I_D$ = 35A
- $r_{DS(ON)}$ = 18.5mΩ, $V_{GS}$ = 4.5V, $I_D$ = 35A
- High performance trench technology for extremely low $r_{DS(ON)}$
- Low gate charge
- High power and current handling capability
- RoHS Compliant

## General Description

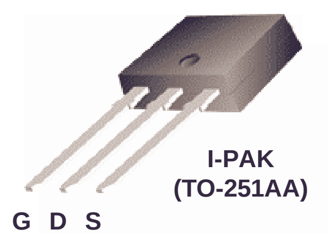
This N-Channel MOSFET has been designed specifically to improve the overall efficiency of DC/DC converters using either synchronous or conventional switching PWM controllers. It has been optimized for low gate charge, low $r_{DS(ON)}$ and fast switching speed.

## Application

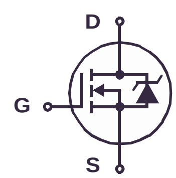
- DC / DC Converters




D-PAK
(TO-252)




I-PAK
(TO-251AA)



## Absolute Maximum Ratings $T_C$ = 25°C unless otherwise noted

| Symbol | Parameter | Ratings | Units |
|---|---|---|---|
| $V_{DSS}$ | Drain to Source Voltage | 30 | V |
| $V_{GS}$ | Gate to Source Voltage | ±20 | V |
| $I_D$ | Drain Current<br>Continuous ($T_C$ = 25°C, $V_{GS}$ = 10V) (Note 1) | 40 | A |
| | Continuous ($T_C$ = 25°C, $V_{GS}$ = 4.5V) (Note 1) | 36 | A |
| | Continuous ($T_{amb}$ = 25°C, $V_{GS}$ = 10V, with $R_{\theta JA}$ = 52°C/W) | 11 | A |
| | Pulsed | Figure 4 | A |
| $E_{AS}$ | Single Pulse Avalanche Energy (Note 2) | 25 | mJ |
| $P_D$ | Power dissipation | 40 | W |
| | Derate above 25°C | 0.27 | W/°C |
| $T_J$, $T_{STG}$ | Operating and Storage Temperature | -55 to 175 | °C |

## Thermal Characteristics

| | | | |
|---|---|---|---|
| $R_{\theta JC}$ | Thermal Resistance Junction to Case TO-252, TO-251 | 3.75 | °C/W |
| $R_{\theta JA}$ | Thermal Resistance Junction to Ambient TO-252, TO-251 | 100 | °C/W |
| $R_{\theta JA}$ | Thermal Resistance Junction to Ambient TO-252, 1in² copper pad area | 52 | °C/W |

## Package Marking and Ordering Information

| Device Marking | Device | Package | Reel Size | Tape Width | Quantity |
|---|---|---|---|---|---|
| FDD8878 | FDD8878 | TO-252AA | 13” | 16mm | 2500 units |
| FDU8878 | FDU8878 | TO-251AA | Tube | N/A | 75 units |

## Electrical Characteristics $T_C$ = 25°C unless otherwise noted

| Symbol | Parameter | Test Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| **Off Characteristics** | | | | | | |
| $B_{VDSS}$ | Drain to Source Breakdown Voltage | $I_D$ = 250µA, $V_{GS}$ = 0V | 30 | - | - | V |
| $I_{DSS}$ | Zero Gate Voltage Drain Current | $V_{DS}$ = 24V | - | - | 1 | µA |
| | | $V_{GS}$ = 0V, $T_C$ = 150°C | - | - | 250 | |
| $I_{GSS}$ | Gate to Source Leakage Current | $V_{GS}$ = ±20V | - | - | ±100 | nA |
| **On Characteristics** | | | | | | |
| $V_{GS(TH)}$ | Gate to Source Threshold Voltage | $V_{GS}$ = $V_{DS}$, $I_D$ = 250µA | 1.2 | - | 2.5 | V |
| $r_{DS(ON)}$ | Drain to Source On Resistance | $I_D$ = 35A, $V_{GS}$ = 10V | - | 0.011 | 0.015 | Ω |
| | | $I_D$ = 35A, $V_{GS}$ = 4.5V | - | 0.014 | 0.0185 | |
| | | $I_D$ = 35A, $V_{GS}$ = 10V, $T_J$ = 175°C | - | 0.018 | 0.024 | |

## Dynamic Characteristics

| | | | | | | |
|---|---|---|---|---|---|---|
| $C_{ISS}$ | Input Capacitance | $V_{DS}$ = 15V, $V_{GS}$ = 0V, f = 1MHz | - | 880 | - | pF |
| $C_{OSS}$ | Output Capacitance | | - | 195 | - | pF |
| $C_{RSS}$ | Reverse Transfer Capacitance | | - | 110 | - | pF |
| $R_G$ | Gate Resistance | $V_{GS}$ = 0.5V, f = 1MHz | - | 3.1 | - | Ω |
| $Q_{g(TOT)}$ | Total Gate Charge at 10V | $V_{GS}$ = 0V to 10V; $V_{DD}$ = 15V, $I_D$ = 35A, $I_g$ = 1.0mA | - | 19 | 26 | nC |
| $Q_{g(5)}$ | Total Gate Charge at 5V | $V_{GS}$ = 0V to 5V | - | 10 | 14 | nC |
| $Q_{g(TH)}$ | Threshold Gate Charge | $V_{GS}$ = 0V to 1V | - | 0.9 | 1.3 | nC |
| $Q_{gs}$ | Gate to Source Gate Charge | | - | 2.6 | - | nC |
| $Q_{gs2}$ | Gate Charge Threshold to Plateau | | - | 1.7 | - | nC |
| $Q_{gd}$ | Gate to Drain “Miller” Charge | | - | 4.5 | - | nC |

## Switching Characteristics ($V_{GS}$ = 10V)

| | | | | | | |
|---|---|---|---|---|---|---|
| $t_{ON}$ | Turn-On Time | $V_{DD}$ = 15V, $I_D$ = 35A, $V_{GS}$ = 4.5V, $R_{GS}$ = 16Ω | - | - | 129 | ns |
| $t_{d(ON)}$ | Turn-On Delay Time | | - | 7 | - | ns |
| $t_r$ | Rise Time | | - | 79 | - | ns |
| $t_{d(OFF)}$ | Turn-Off Delay Time | | - | 38 | - | ns |
| $t_f$ | Fall Time | | - | 27 | - | ns |
| $t_{OFF}$ | Turn-Off Time | | - | - | 97 | ns |

## Drain-Source Diode Characteristics

| | | | | | | |
|---|---|---|---|---|---|---|
| $V_{SD}$ | Source to Drain Diode Voltage | $I_{SD}$ = 35A | - | - | 1.25 | V |
| | | $I_{SD}$ = 3.2A | - | - | 1.0 | V |
| $t_{rr}$ | Reverse Recovery Time | $I_{SD}$ = 35A, $dI_{SD}/dt$ = 100A/µs | - | - | 23 | ns |
| $Q_{RR}$ | Reverse Recovered Charge | $I_{SD}$ = 35A, $dI_{SD}/dt$ = 100A/µs | - | - | 9 | nC |

**Notes:**
**1:** Package current limitation is 35A.
**2:** Starting $T_J$ = 25°C, L = 65uH, $I_{AS}$ = 28A, $V_{DD}$ = 27V, $V_{GS}$ = 10V.

## Typical Characteristics $T_C = 25°C$ unless otherwise noted

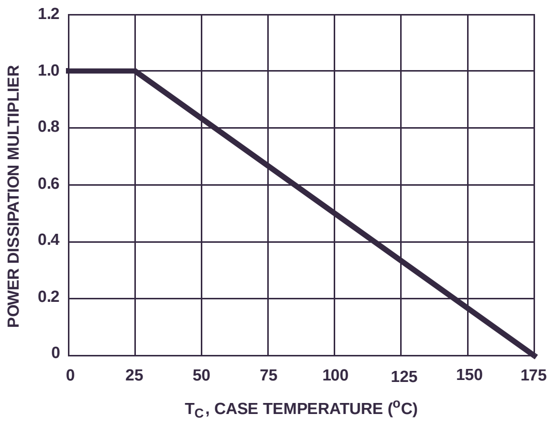



**Figure 1. Normalized Power Dissipation vs Case Temperature**

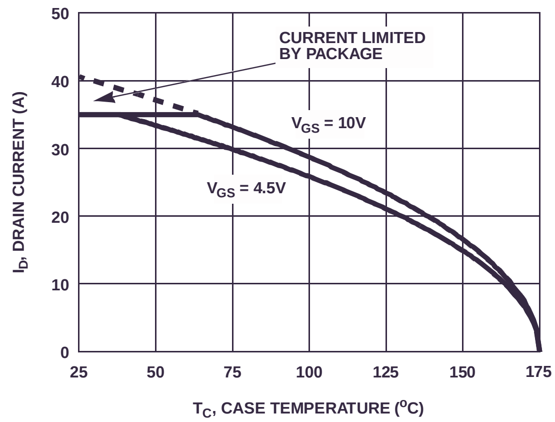



**Figure 2. Maximum Continuous Drain Current vs Case Temperature**

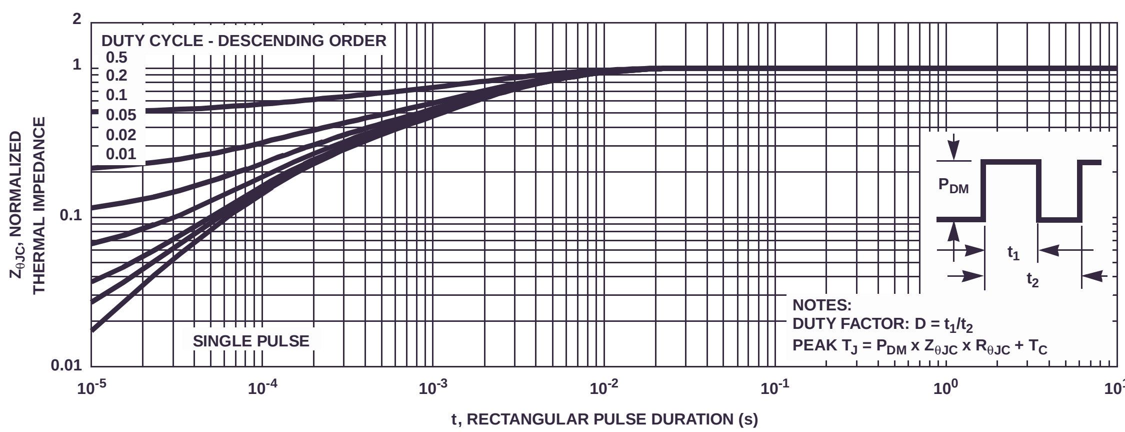



**Figure 3. Normalized Maximum Transient Thermal Impedance**

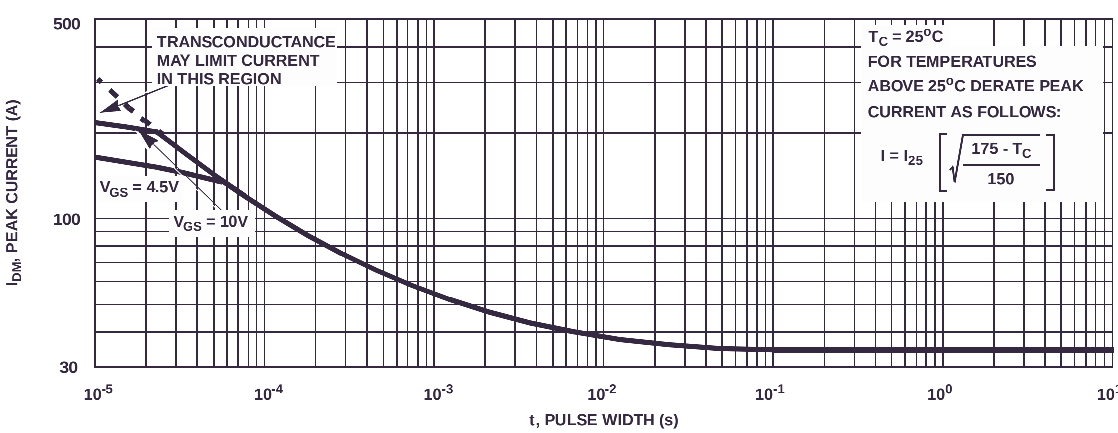



**Figure 4. Peak Current Capability**

## Typical Characteristics $T_C$ = 25°C unless otherwise noted

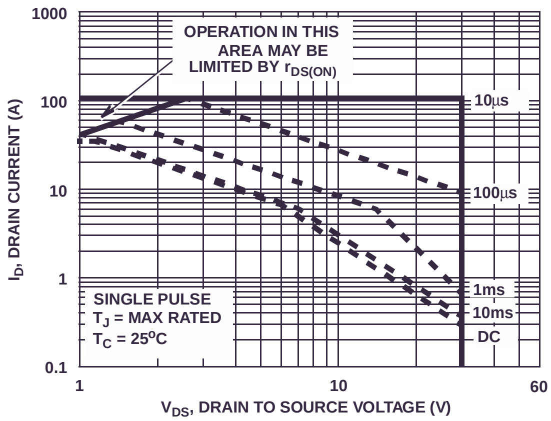
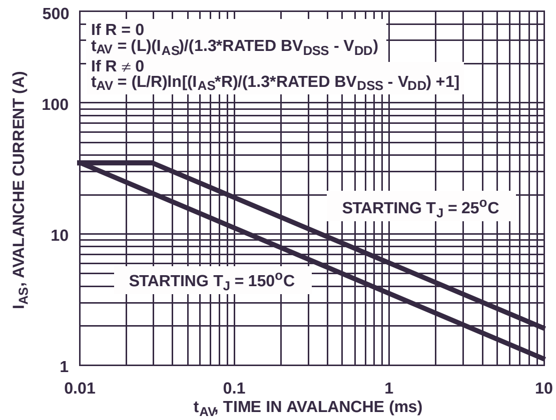



**Figure 5. Forward Bias Safe Operating Area**




NOTE: Refer to Fairchild Application Notes AN7514 and AN7515

**Figure 6. Unclamped Inductive Switching Capability**

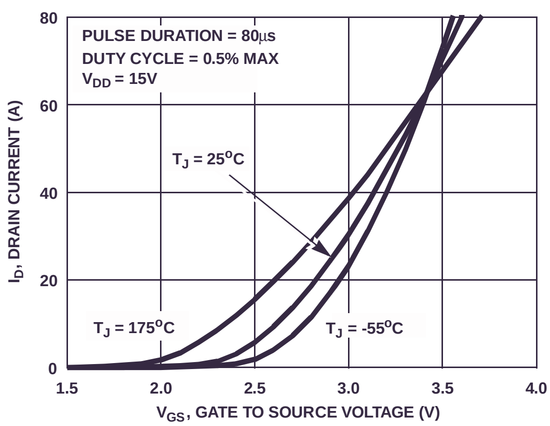



**Figure 7. Transfer Characteristics**

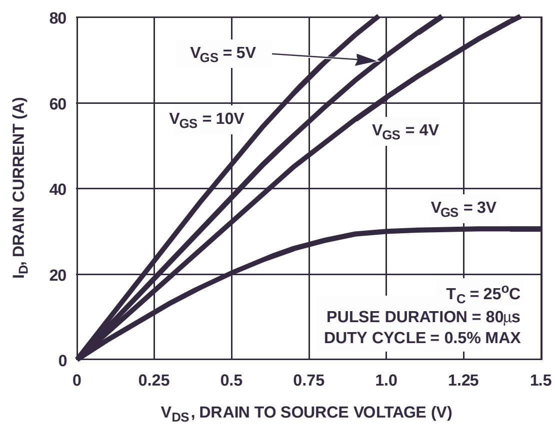



**Figure 8. Saturation Characteristics**

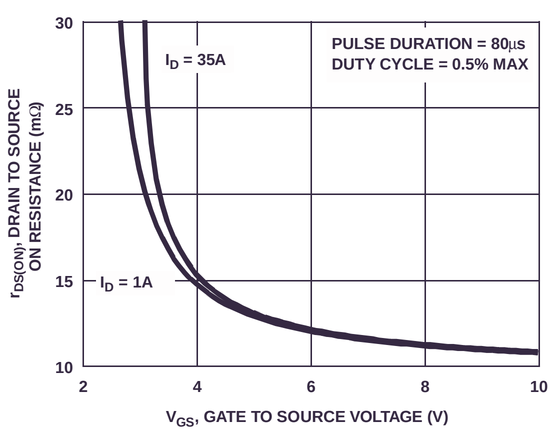



**Figure 9. Drain to Source On Resistance vs Gate Voltage and Drain Current**

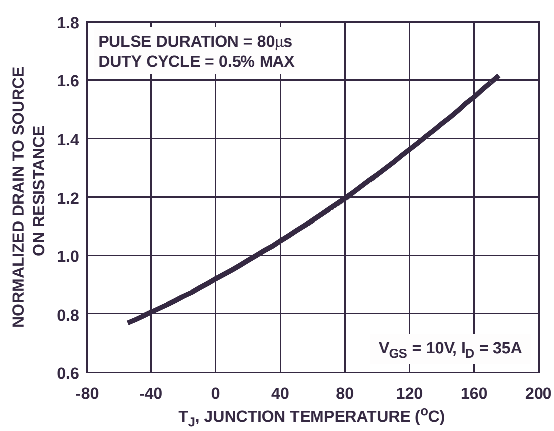



**Figure 10. Normalized Drain to Source On Resistance vs Junction Temperature**

## Typical Characteristics $T_C$ = 25°C unless otherwise noted

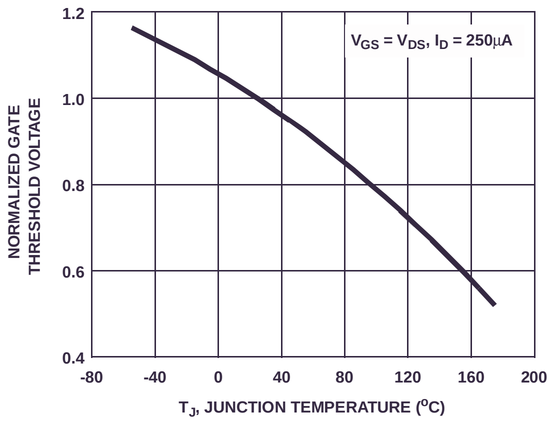



**Figure 11. Normalized Gate Threshold Voltage vs Junction Temperature**

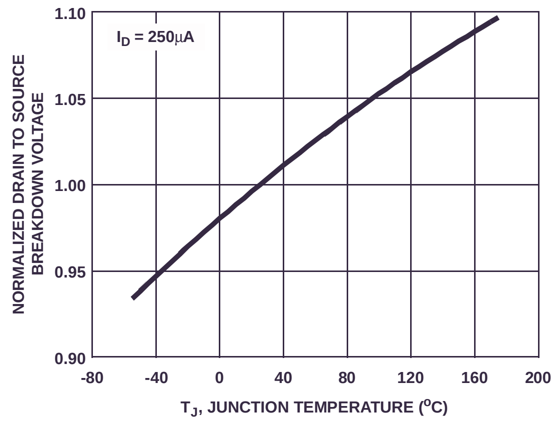



**Figure 12. Normalized Drain to Source Breakdown Voltage vs Junction Temperature**

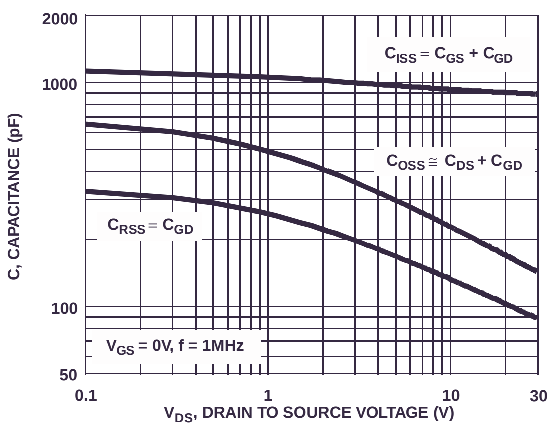



**Figure 13. Capacitance vs Drain to Source Voltage**

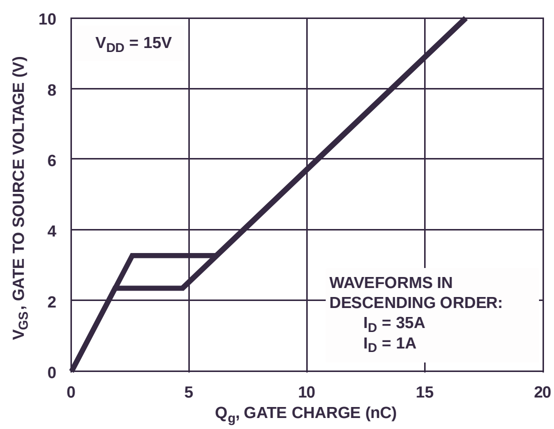



**Figure 14. Gate Charge Waveforms for Constant Gate Current**

## Test Circuits and Waveforms

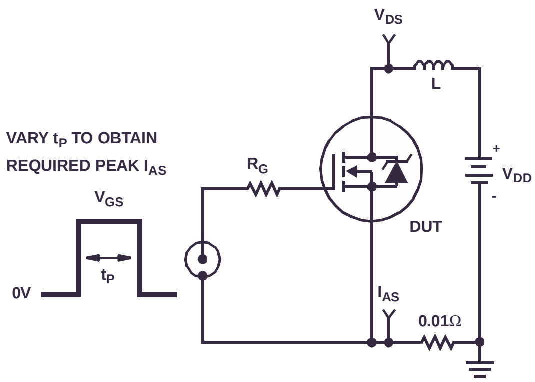



**Figure 15. Unclamped Energy Test Circuit**

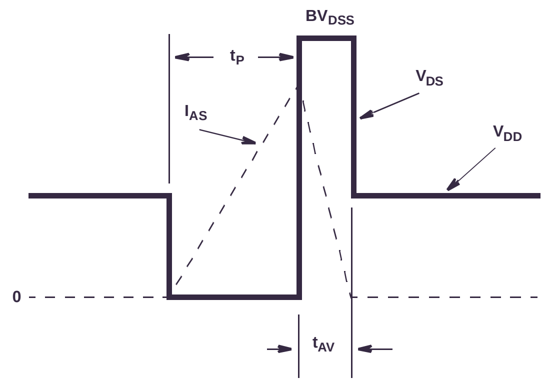



**Figure 16. Unclamped Energy Waveforms**

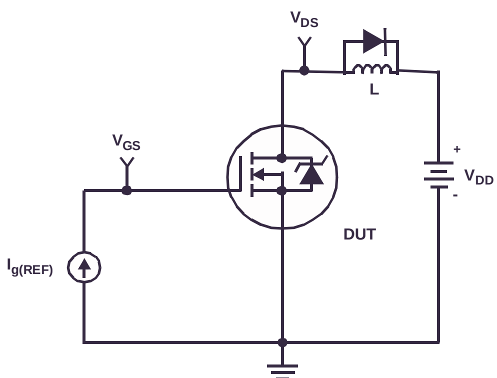



**Figure 17. Gate Charge Test Circuit**

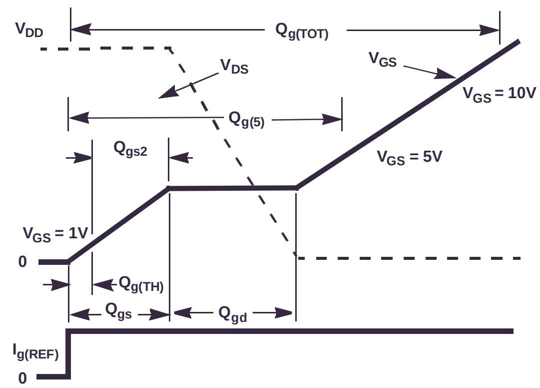



**Figure 18. Gate Charge Waveforms**

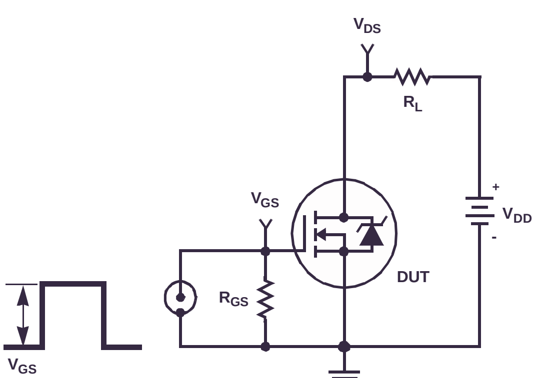



**Figure 19. Switching Time Test Circuit**

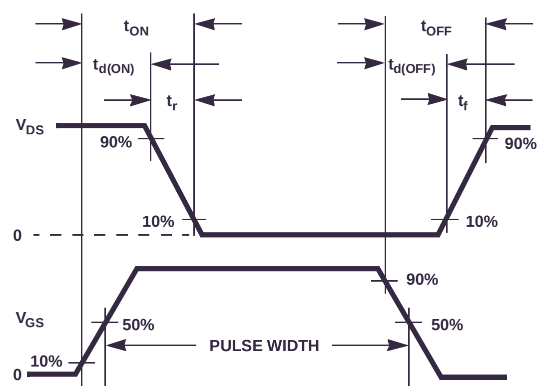



**Figure 20. Switching Time Waveforms**

## *Thermal Resistance vs. Mounting Pad Area*

The maximum rated junction temperature, $T_{JM}$, and the thermal resistance of the heat dissipating path determines the maximum allowable device power dissipation, $P_{DM}$, in an application. Therefore the application's ambient temperature, $T_A$ ($^oC$), and thermal resistance $R_{\theta JA}$ ($^oC/W$) must be reviewed to ensure that $T_{JM}$ is never exceeded. Equation 1 mathematically represents the relationship and serves as the basis for establishing the rating of the part.

$$P_{DM} = \frac{(T_{JM} - T_A)}{R_{\theta JA}} \qquad \text{(EQ. 1)}$$

In using surface mount devices such as the TO-252 package, the environment in which it is applied will have a significant influence on the part's current and maximum power dissipation ratings. Precise determination of $P_{DM}$ is complex and influenced by many factors:

1. Mounting pad area onto which the device is attached and whether there is copper on one side or both sides of the board.
2. The number of copper layers and the thickness of the board.
3. The use of external heat sinks.
4. The use of thermal vias.
5. Air flow and board orientation.
6. For non steady state applications, the pulse width, the duty cycle and the transient thermal response of the part, the board and the environment they are in.

Fairchild provides thermal information to assist the designer's preliminary application evaluation. Figure 21 defines the $R_{\theta JA}$ for the device as a function of the top copper (component side) area. This is for a horizontally positioned FR-4 board with 1oz copper after 1000 seconds of steady state power with no air flow. This graph provides the necessary information for calculation of the steady state junction temperature or power dissipation. Pulse applications can be evaluated using the Fairchild device Spice thermal model or manually utilizing the normalized maximum transient thermal impedance curve.

Thermal resistances corresponding to other copper areas can be obtained from Figure 21 or by calculation using Equation 2 or 3. Equation 2 is used for copper area defined in inches square and equation 3 is for area in centimeters square. The area, in square inches or square centimeters is the top copper area including the gate and source pads.

$$R_{\theta JA} = 33.32 + \frac{23.84}{(0.268 + Area)} \qquad \text{(EQ. 2)}$$

Area in Inches Squared

$$R_{\theta JA} = 33.32 + \frac{154}{(1.73 + Area)} \qquad \text{(EQ. 3)}$$

Area in Centimeters Squared

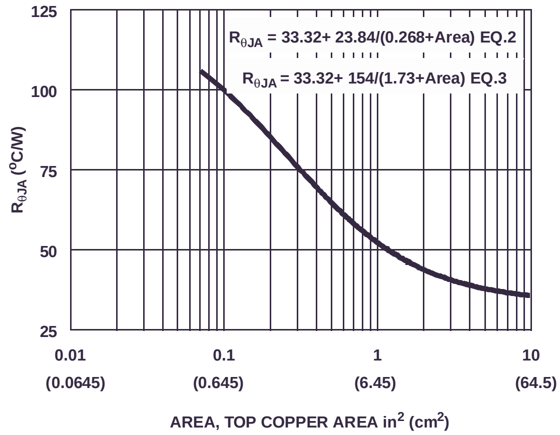
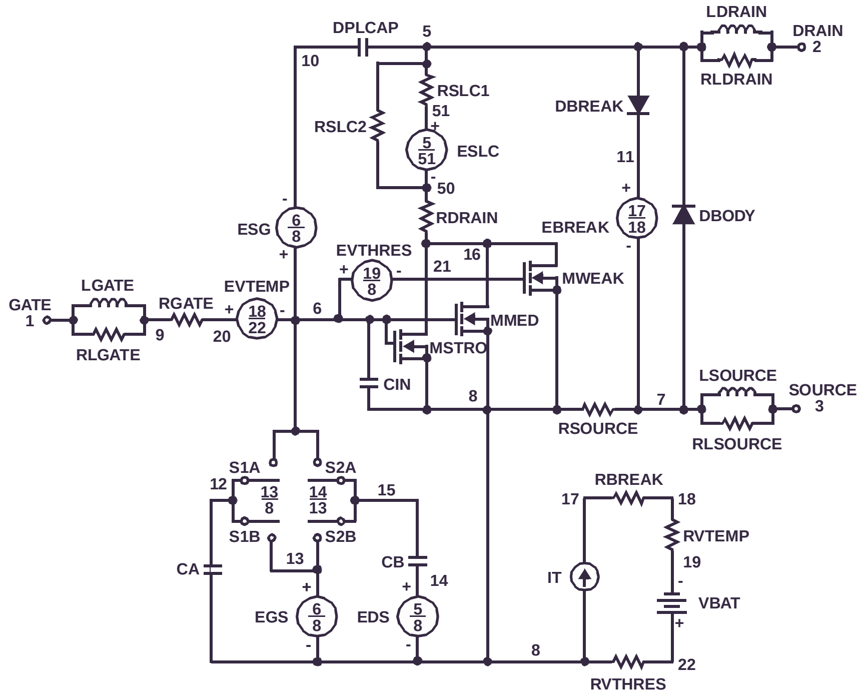



**Figure 21. Thermal Resistance vs Mounting Pad Area**

## PSPICE Electrical Model

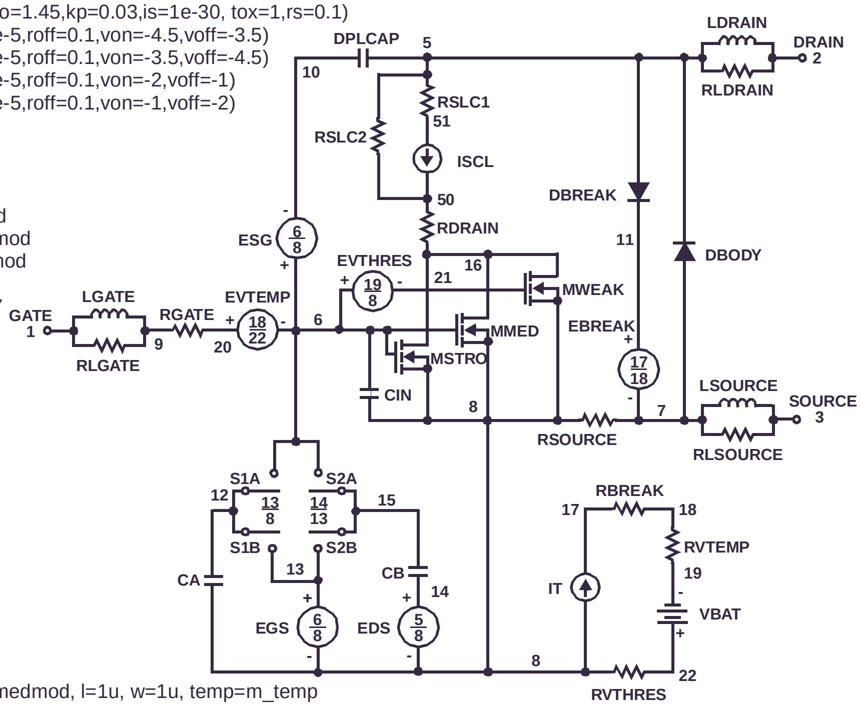



```
.SUBCKT FDD8878  2 1 3 ; rev February 2004
Ca 12 8 8.6e-10
Cb 15 14 7.2e-10
Cin 6 8 8e-10

Dbody 7 5 DbodyMOD
Dbreak 5 11 DbreakMOD
Dplcap 10 5 DplcapMOD

Ebreak 11 7 17 18 32.97
Eds 14 8 5 8 1
Egs 13 8 6 8 1
Esg 6 10 6 8 1
Evthres 6 21 19 8 1
Evtemp 20 6 18 22 1

It 8 17 1

Lgate 1 9 5.4e-9
Ldrain 2 5 1.0e-9
Lsource 3 7 2e-9

RLgate 1 9 54
RLdrain 2 5 10
RLsource 3 7 20

Mmed 16 6 8 8 MmedMOD
Mstro 16 6 8 8 MstroMOD
Mweak 16 21 8 8 MweakMOD

Rbreak 17 18 RbreakMOD 1
Rdrain 50 16 RdrainMOD 6.9e-3
Rgate 9 20 3.1
RSLC1 5 51 RSLCMOD 1e-6
RSLC2 5 50 1e3
Rsource 8 7 RsourceMOD 2.7e-3
Rvthres 22 8 RvthresMOD 1
Rvtemp 18 19 RvtempMOD 1
S1a 6 12 13 8 S1AMOD
S1b 13 12 13 8 S1BMOD
S2a 6 15 14 13 S2AMOD
S2b 13 15 14 13 S2BMOD

Vbat 22 19 DC 1

ESLC 51 50  VALUE={(V(5,51)/ABS(V(5,51)))*(PWR(V(5,51)/(1e-6*125),5))}

.MODEL DbodyMOD D (IS=2.6E-12 IKF=8 N=1.01 RS=6.4e-3 TRS1=8e-4 TRS2=2e-7
+ CJO=3.4e-10 M=0.53 TT=1e-17 XTI=2)
.MODEL DbreakMOD D (RS=1.4 TRS1=1e-3 TRS2=-5e-6)
.MODEL DplcapMOD D (CJO=3.4e-10 IS=1e-30 N=10 M=0.39)

.MODEL MmedMOD NMOS (VTO=1.75 KP=7 IS=1e-30 N=10 TOX=1 L=1u W=1u RG=3.1 T_ABS=25)
.MODEL MstroMOD NMOS (VTO=2.2 KP=100 IS=1e-30 N=10 TOX=1 L=1u W=1u T_ABS=25)
.MODEL MweakMOD NMOS (VTO=1.45 KP=0.03 IS=1e-30 N=10 TOX=1 L=1u W=1u RG=31 RS=0.1 T_ABS=25)

.MODEL RbreakMOD RES (TC1=8.3e-4 TC2=-8e-7)
.MODEL RdrainMOD RES (TC1=1e-4 TC2=7.5e-6)
.MODEL RSLCMOD RES (TC1=9e-4 TC2=1e-6)
.MODEL RsourceMOD RES (TC1=1.3e-2 TC2=2e-6)
.MODEL RvthresMOD RES (TC1=-1.7e-3 TC2=-8e-6)
.MODEL RvtempMOD RES (TC1=-2.2e-3 TC2=2e-7)

.MODEL S1AMOD VSWITCH (RON=1e-5 ROFF=0.1 VON=-4.5 VOFF=-3.5)
.MODEL S1BMOD VSWITCH (RON=1e-5 ROFF=0.1 VON=-3.5 VOFF=-4.5)
.MODEL S2AMOD VSWITCH (RON=1e-5 ROFF=0.1 VON=-2 VOFF=-1)
.MODEL S2BMOD VSWITCH (RON=1e-5 ROFF=0.1 VON=-1 VOFF=-2)
.ENDS
```

Note: For further discussion of the PSPICE model, consult **A New PSPICE Sub-Circuit for the Power MOSFET Featuring Global Temperature Options**; IEEE Power Electronics Specialist Conference Records, 1991, written by William J. Hepp and C. Frank Wheatley.

## SABER Electrical Model

```
rev February 2004
template FDD8878 n2,n1,n3 =m_temp
electrical n2,n1,n3
number m_temp=25
{
var i iscl
dp..model dbodymod =  (isl=2.6e-12,ikf=8,nl=1.01,rs=6.4e-3,trs1=8e-4,trs2=2e-7,cjo=3.4e-10,m=0.53,tt=1e-17,xti=2)
dp..model dbreakmod = (rs=1.4,trs1=1e-3,trs2=-5e-6)
dp..model dplcapmod =  (cjo=3.4e-10,isl=10e-30,nl=10,m=0.39)
m..model mmedmod = (type=_n,vto=1.75,kp=7,is=1e-30, tox=1)
m..model mstrongmod = (type=_n,vto=2.2,kp=100,is=1e-30, tox=1)
m..model mweakmod = (type=_n,vto=1.45,kp=0.03,is=1e-30, tox=1,rs=0.1)
sw_vcsp..model s1amod =  (ron=1e-5,roff=0.1,von=-4.5,voff=-3.5)
sw_vcsp..model s1bmod =  (ron=1e-5,roff=0.1,von=-3.5,voff=-4.5)
sw_vcsp..model s2amod =  (ron=1e-5,roff=0.1,von=-2,voff=-1)
sw_vcsp..model s2bmod =  (ron=1e-5,roff=0.1,von=-1,voff=-2)
c.ca n12 n8 = 8.6e-10
c.cb n15 n14 = 7.2e-10
c.cin n6 n8 = 8e-10

dp.dbody n7 n5 = model=dbodymod
dp.dbreak n5 n11 = model=dbreakmod
dp.dplcap n10 n5 = model=dplcapmod

spe.ebreak n11 n7 n17 n18 = 32.97
spe.eds n14 n8 n5 n8 = 1
spe.egs n13 n8 n6 n8 = 1
spe.esg n6 n10 n6 n8 = 1
spe.evthres n6 n21 n19 n8 = 1
spe.evtemp n20 n6 n18 n22 = 1

i.it n8 n17 = 1

l.lgate n1 n9 = 5.4e-9
l.ldrain n2 n5 = 1.0e-9
l.lsource n3 n7 = 2e-9

res.rlgate n1 n9 = 54
res.rldrain n2 n5 = 10
res.rlsource n3 n7 = 20

m.mmed n16 n6 n8 n8 = model=mmedmod, l=1u, w=1u, temp=m_temp
m.mstrong n16 n6 n8 n8 = model=mstrongmod, l=1u, w=1u, temp=m_temp
m.mweak n16 n21 n8 n8 = model=mweakmod, l=1u, w=1u, temp=m_temp

res.rbreak n17 n18  = 1, tc1=8.3e-4,tc2=-8e-7
res.rdrain n50 n16  = 6.9e-3, tc1=1e-4,tc2=7.5e-6
res.rgate n9 n20 = 3.1
res.rslc1 n5 n51  = 1e-6, tc1=9e-4,tc2=1e-6
res.rslc2 n5 n50 = 1e3
res.rsource n8 n7  = 2.7e-3, tc1=1.3e-2,tc2=2e-6
res.rvthres n22 n8  = 1, tc1=-1.7e-3,tc2=-8e-6
res.rvtemp n18 n19  = 1, tc1=-2.2e-3,tc2=2e-7
sw_vcsp.s1a n6 n12 n13 n8 = model=s1amod
sw_vcsp.s1b n13 n12 n13 n8 = model=s1bmod
sw_vcsp.s2a n6 n15 n14 n13 = model=s2amod
sw_vcsp.s2b n13 n15 n14 n13 = model=s2bmod

v.vbat n22 n19 = dc=1
equations {
i (n51->n50) +=iscl
iscl: v(n51,n50) = ((v(n5,n51)/(1e-9+abs(v(n5,n51))))*((abs(v(n5,n51)*1e6/125))** 5))
}
}
```



## *PSPICE Thermal Model*

REV 23 February 2004

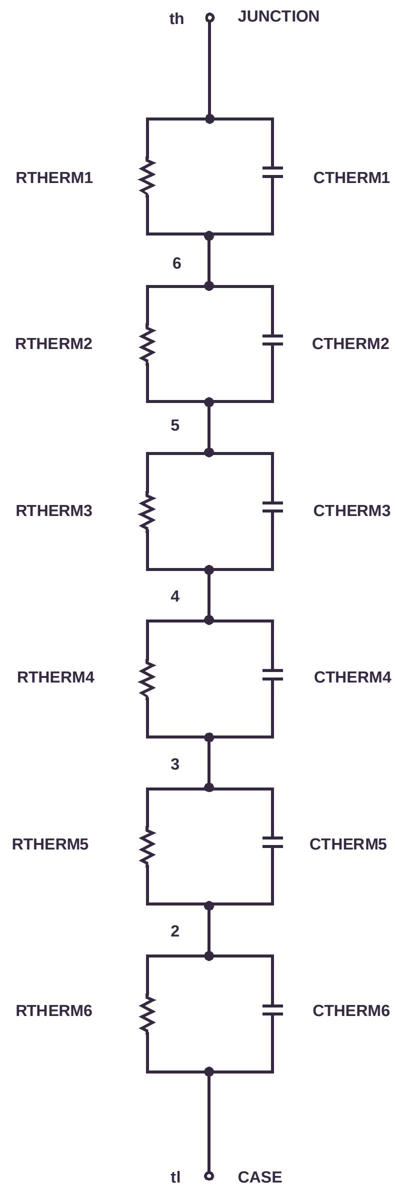
FDD8878T

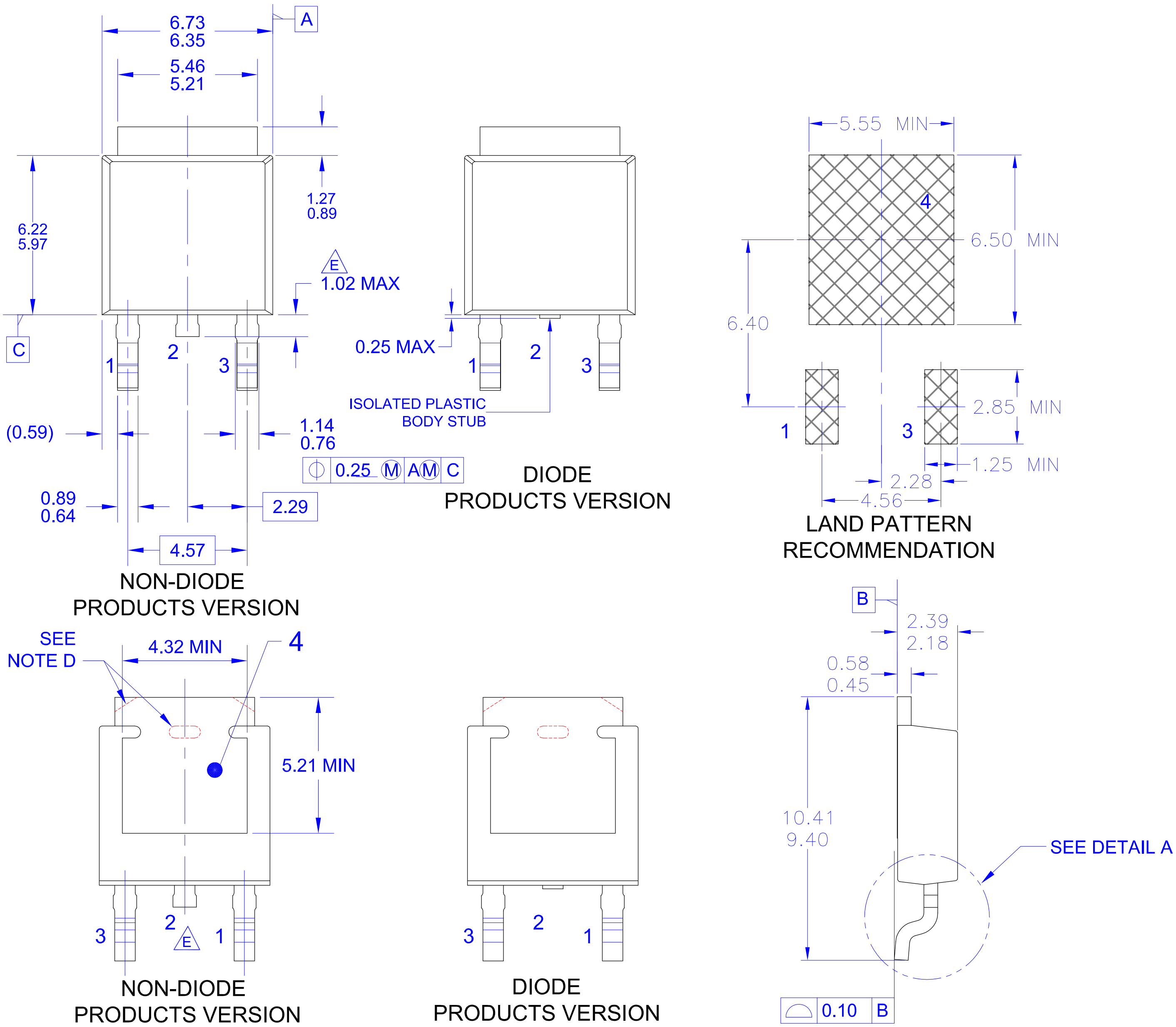
CTHERM1 TH 6 3.5e-4
CTHERM2 6 5 5e-4
CTHERM3 5 4 2.5e-3
CTHERM4 4 3 2.7e-3
CTHERM5 3 2 5e-3
CTHERM6 2 TL 1e-2

RTHERM1 TH 6 2.9e-1
RTHERM2 6 5 3.5e-1
RTHERM3 5 4 4.5e-1
RTHERM4 4 3 5.2e-1
RTHERM5 3 2 6.9e-1
RTHERM6 2 TL 7e-1

## *SABER Thermal Model*

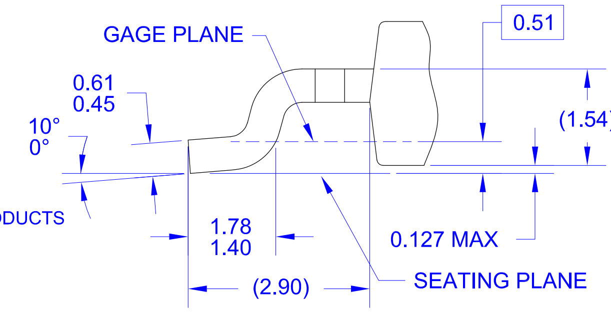
```
SABER thermal model FDD8878T
template thermal_model th tl
thermal_c th, tl
{
ctherm.ctherm1 th 6 =3.5e-4
ctherm.ctherm2 6 5 =5e-4
ctherm.ctherm3 5 4 =2.5e-3
ctherm.ctherm4 4 3 =2.7e-3
ctherm.ctherm5 3 2 =5e-3
ctherm.ctherm6 2 tl =1e-2

rtherm.rtherm1 th 6 =2.9e-1
rtherm.rtherm2 6 5 =3.5e-1
rtherm.rtherm3 5 4 =4.5e-1
rtherm.rtherm4 4 3 =5.2e-1
rtherm.rtherm5 3 2 =6.9e-1
rtherm.rtherm6 2 tl =7e-1
}
```






NOTES: UNLESS OTHERWISE SPECIFIED

A) THIS PACKAGE CONFORMS TO JEDEC, TO-252, ISSUE C, VARIATION AA.
B) ALL DIMENSIONS ARE IN MILLIMETERS.
C) DIMENSIONING AND TOLERANCING PER ASME Y14.5M-2009.
D) SUPPLIER DEPENDENT MOLD LOCKING HOLES OR CHAMFERED CORNERS OR EDGE PROTRUSION.
E) TRIMMED METAL CENTER LEAD IS PRESENT ON FOR NON-DIODE PRODUCTS
F) DIMENSIONS ARE EXCLUSIVE OF BURS, MOLD FLASH AND TIE BAR EXTRUSIONS.
G) LAND PATTERN RECOMMENDATION IS BASED ON IPC7351A STD TO228P991X239-3N.
H) DRAWING NUMBER AND REVISION: MKT-TO252A03REV11




DETAIL A
(ROTATED -90°)
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FAIRCHILD

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