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November 2013

FDD8N50NZ

N-Channel UniFETTM II MOSFET 500 V, 6.5 A, 850 m Ω

Features

- $R_{DS(on)}$ = 770 m Ω (Typ.) @ V_{GS} = 10 V, I_D = 3.25 A
- Low Gate Charge (Typ. 14 nC)
- Low C_{rss} (Typ. 5 pF)
- 100% Avalanche Tested
- · Improved dv/dt Capability
- · ESD Imoroved Capability
- · RoHS Compliant

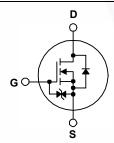
Applications

- LCD/LED/PDP TV
- · Lighting
- · Uninterruptible Power Supply

Description

UniFETTM II MOSFET is Fairchild Semiconductor's high voltage MOSFET family based on advanced planar stripe and DMOS technology. This advanced MOSFET family has the smallest on-state resistance among the planar MOSFET, and also provides superior switching performance and higher avalanche energy strength. In addition, internal gate-source ESD diode allows UniFETTM II MOSFET to withstand over 2kV HBM surge stress. This device family is suitable for switching power converter applications such as power factor correction (PFC), flat panel display (FPD) TV power, ATX and electronic lamp ballasts





MOSFET Maximum Ratings T_C = 25°C unless otherwise noted.

Symbol		Parameter		FDD8N50NZTM	Unit
V _{DSS}	Drain to Source Voltage	Drain to Source Voltage			V
V _{GSS}	Gate to Source Voltage			±25	V
	Drain Current	- Continuous (T _C = 25°C)		6.5	Α
ID	Drain Current	- Continuous (T _C = 100°C)		3.9	A
I _{DM}	Drain Current	- Pulsed	(Note 1)	26	Α
E _{AS}	Single Pulsed Avalanche Energy (Note 2)			287	mJ
I _{AR}	Avalanche Current (Note			6.5	Α
E _{AR}	Repetitive Avalanche Energy (Note 1)			9	mJ
dv/dt	Peak Diode Recovery dv/c	lt	(Note 3)	10	V/ns
Б	Dawer Dissipation	(T _C = 25°C)		90	W
P_{D}	Power Dissipation	- Derate Above 25°C		0.7	W/°C
T _J , T _{STG}	Operating and Storage Ter	-55 to +150	οС		
T _L	Maximum Lead Temperatu	re for Soldering, 1/8" from Case for 5 Seco	onds	300	°С

Thermal Characteristics

Symbol	Parameter FDD8N50NZT		Unit
$R_{\theta JC}$	Thermal Resistance, Junction to Case, Max. 1.4		°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient, Max. 62.5		°C/VV

Package Marking and Ordering Information

Pa	art Number	Top Mark	Package	Packing Method	Reel Size	Tape Width	Quantity
FDI	D8N50NZTM	FDD8N50NZ	DPAK	Tape and Reel	330 mm	16 mm	2500 units

Electrical Characteristics $T_C = 25^{\circ}C$ unless otherwise noted.

Symbol	Parameter	Test Conditions	Min.	Тур.	Max.	Unit
Off Charac	cteristics					
BV _{DSS}	Drain to Source Breakdown Voltage	$I_D = 250 \mu A, V_{GS} = 0 V, T_C = 25^{\circ}C$	500	-	-	V
ΔBV _{DSS} / ΔT _J	Breakdown Voltage Temperature Coefficient	I_D = 250 μ A, Referenced to 25°C	-	0.5	-	V/°C
	Zero Gate Voltage Drain Current	V _{DS} = 500 V, V _{GS} = 0 V	-	-	1	
I _{DSS}	Zero Gate voltage Drain Current	$V_{DS} = 400 \text{ V}, T_C = 125^{\circ}\text{C}$	-	-	10	μΑ
I _{GSS}	Gate to Body Leakage Current	V _{GS} = ±25 V, V _{DS} = 0 V	-	-	±10	μΑ

On Characteristics

$V_{GS(th)}$	Gate Threshold Voltage	$V_{GS} = V_{DS}, I_{D} = 250 \mu\text{A}$	3.0	-	5.0	V
R _{DS(on)}	Static Drain to Source On Resistance	$V_{GS} = 10 \text{ V}, I_D = 3.25 \text{ A}$	-	0.77	0.85	Ω
9 _{FS}	Forward Transconductance	V _{DS} = 20 V, I _D = 3.25 A	-	6.3	-	S

Dynamic Characteristics

C _{iss}	Input Capacitance	V 05.V.V 0.V		-	565	735	pF
C _{oss}	Output Capacitance	V _{DS} = 25 V, V _{GS} = 0 V, f = 1 MHz		-	80	105	pF
C _{rss}	Reverse Transfer Capacitance	1 - 1 WII 12		-\	5	8	pF
Q _{g(tot)}	Total Gate Charge at 10V			- \	14	18	nC
Q_{gs}	Gate to Source Gate Charge	$V_{DS} = 400 \text{ V}, I_{D} = 6.5 \text{ A},$		- \	4	-	nC
Q_{gd}	Gate to Drain "Miller" Charge	$V_{GS} = 10 \text{ V}$	(Note 4)	-	6	-	nC

Switching Characteristics

t _{d(on)}	Turn-On Delay Time		-	17	45	ns
t _r		$V_{DD} = 250 \text{ V}, I_D = 6.5 \text{ A},$	-	34	80	ns
t _{d(off)}	Turn-Off Delay Time	$R_G = 25 \Omega, V_{GS} = 10 V$	-	43	95	ns
t _f	Turn-Off Fall Time	(Note 4)	-	27	60	ns

Drain-Source Diode Characteristics

I _S	Maximum Continuous Drain to Source Dioc	Maximum Continuous Drain to Source Diode Forward Current		-	8	Α
I _{SM}	Maximum Pulsed Drain to Source Diode Forward Current		/ -	-	30	Α
V_{SD}	Drain to Source Diode Forward Voltage	$V_{GS} = 0 \text{ V}, I_{SD} = 6.5 \text{ A}$	-	-	1.4	V
t _{rr}	Reverse Recovery Time	V _{GS} = 0 V, I _{SD} = 6.5 A,	-	228	-	ns
Q _{rr}	Reverse Recovery Charge	$dI_F/dt = 100 A/\mu s$	-	1.43	/ -	μС

Notes

- 1. Repetitive rating: pulse-width limited by maximum junction temperature.
- 2. L = 13.6 mH, I $_{AS}$ = 6.5 A, V $_{DD}$ = 50 V, R $_{G}$ = 25 $\Omega,$ starting T $_{J}$ = 25 $^{\circ}C.$
- 3. I $_{SD}$ \leq 6.5 A, di/dt \leq 200 A/ μ s, V $_{DD}$ \leq BV $_{DSS}$, starting T $_{J}$ = 25°C.
- 4. Essentially Independent of Operating Temperature Typical Characteristics

Typical Performance Characteristics

Figure 1. On-Region Characteristics

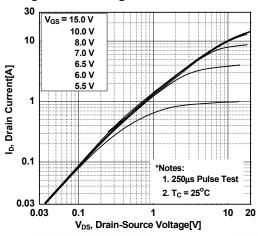


Figure 3. On-Resistance Variation vs.
Drain Current and Gate Voltage

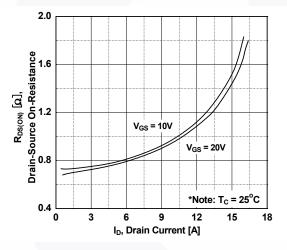


Figure 5. Capacitance Characteristics

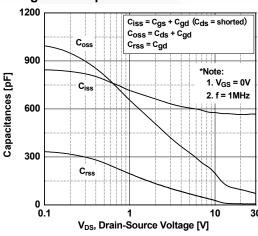


Figure 2. Transfer Characteristics

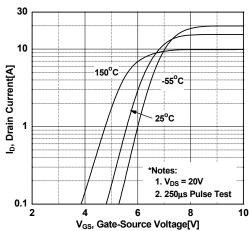


Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature

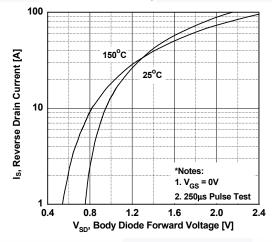
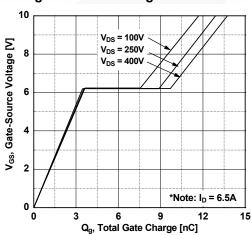


Figure 6. Gate Charge Characteristics



Typical Performance Characteristics (Continued)

Figure 7. Breakdown Voltage Variation vs. Temperature

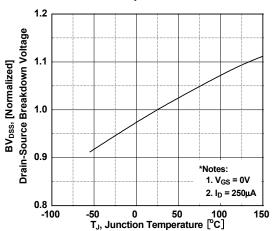


Figure 9. Maximum Safe Operating Area

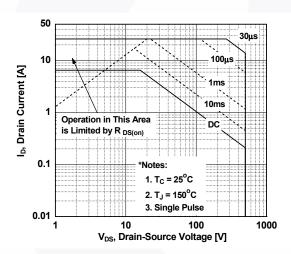


Figure 8. On-Resistance Variation vs. Temperature

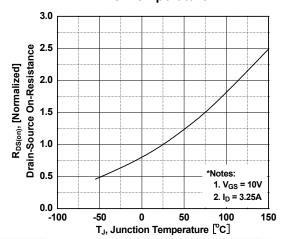


Figure 10. Maximum Drain Current vs. Case Temperature

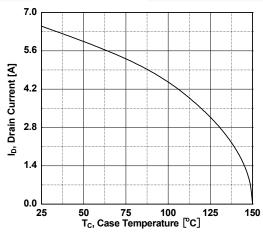
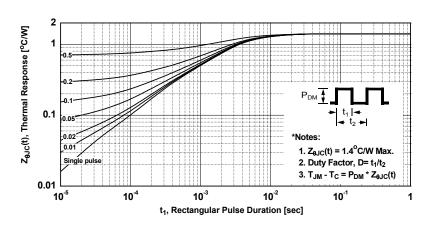


Figure 11. Transient Thermal Response Curve



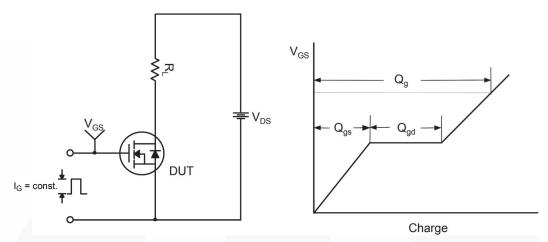


Figure 12. Gate Charge Test Circuit & Waveform



Figure 13. Resistive Switching Test Circuit & Waveforms

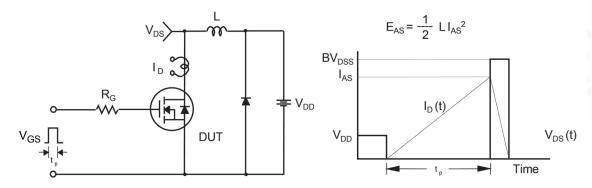


Figure 14. Unclamped Inductive Switching Test Circuit & Waveforms

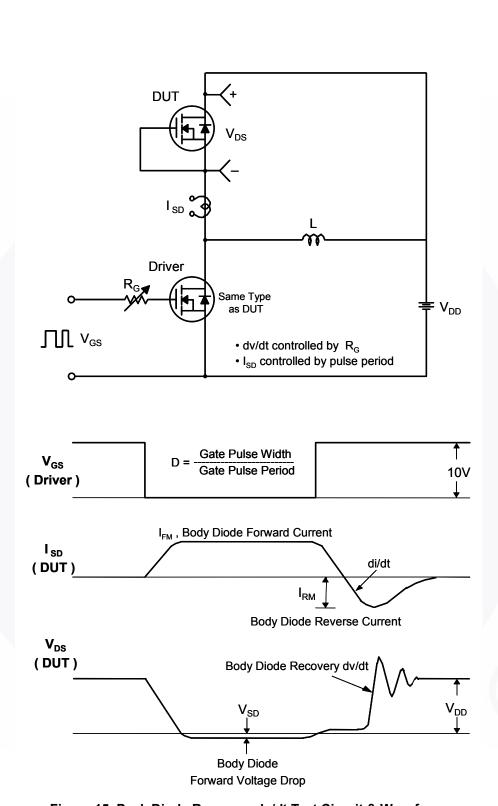


Figure 15. Peak Diode Recovery dv/dt Test Circuit & Waveforms

Mechanical Dimensions

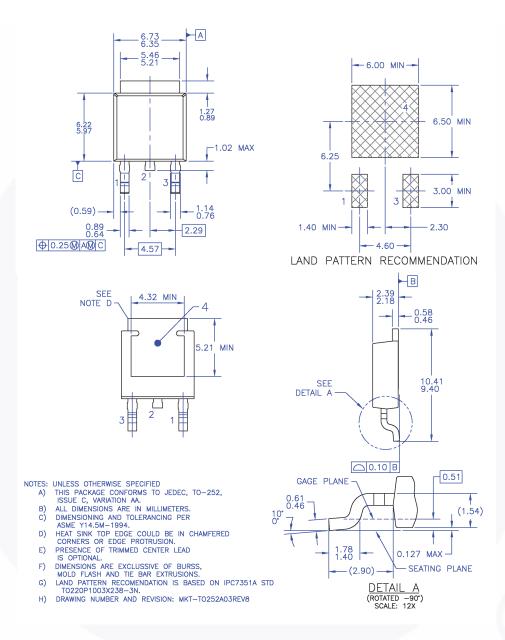


Figure 16. TO252 (D-PAK), Molded, 3-Lead, Option AA&AB

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