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ON Semiconductor®

FDD9409-F085

N-Channel PowerTrench® MOSFET **40 V, 90 A, 3.2 m**Ω

Features

- Typ $R_{DS(on)}$ = 2.3m Ω at V_{GS} = 10V, I_D = 80A
- Typ $Q_{q(tot)}$ = 42nC at V_{GS} = 10V, I_{D} = 80A
- UIS Capability
- RoHS Compliant
- Qualified to AEC Q101

Applications

- Automotive Engine Control
- Powertrain Management
- Solenoid and Motor Drivers
- Electronic Steering
- Integrated Starter/Alternator
- Distributed Power Architectures and VRM
- Primary Switch for 12V Systems

MOSFET Maximum Ratings T₁ = 25°C unless otherwise noted

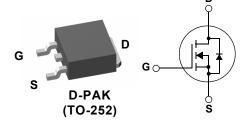
Symbol	Parameter		Ratings	Units
V _{DSS}	Drain-to-Source Voltage		40	V
V _{GS}	Gate-to-Source Voltage		±20	V
I _D	Drain Current - Continuous (V _{GS} =10) (Note 1)	T _C = 25°C	90	^
	Pulsed Drain Current	T _C = 25°C	See Figure 4	A
E _{AS}	Single-Pulse Avalanche Energy	(Note 2)	101	mJ
E _{AS} :	Power Dissipation		150	W
	Derate Above 25°C		1	W/°C
T _J , T _{STG}	Operating and Storage Temperature		-55 to + 175	°C
$R_{\theta JC}$	Thermal Resistance, Junction to Case		1	°C/W
$R_{\theta JA}$	Maximum Thermal Resistance, Junction to Ambient	(Note 3)	52	°C/W

Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
FDD9409	FDD9409-F085	D-PAK(TO-252)	13"	12mm	2500 units

Notes:

- 1: Current is limited by bondwire configuration.
- Current is inflied by borlowine configuration.
 Starting T_J = 25°C, L = 0.1mH, I_{AS} = 44A, V_{DD} = 40V during inductor charging and V_{DD} = 0V during time in avalanche.
 R_{θ,JA} is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. R_{θ,JC} is guaranteed by design while R_{θ,JA} is determined by the user's board design. The maximum rating presented here is based on mounting on a 1 in² pad of 2oz copper.



Units

Max.

Electrical Characteristics T ₁ =	= 25°C unless otherwise noted.
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Parameter

Off Ch	aracteristics						
B _{VDSS}	Drain-to-Source Breakdown Voltage	I _D = 250μA, \	V _{GS} = 0V	40	-	-	V
I _{DSS}	Drain-to-Source Leakage Current	V _{DS} =40V,	$T_{J} = 25^{\circ}C$	-	-	1	μΑ
		$V_{GS} = 0V$	$T_J = 175^{\circ}C(Note 4)$	-	-	1	mA
I _{GSS}	Gate-to-Source Leakage Current	$V_{GS} = \pm 20V$		-	-	±100	nA

Test Conditions

Min.

Тур.

On Characteristics

Symbol

$V_{GS(th)}$	Gate-to-Source Threshold Voltage	$V_{GS} = V_{DS}, I_D = 250 \mu A$		2.0	3.2	4.0	V
R _{DS(on)}	Drain-to-Source On Resistance	I _D = 80A,	$T_{\rm J} = 25^{\rm o}{\rm C}$	-	2.3	3.2	$m\Omega$
	Dialii-to-Source Oil Resistance	V _{GS} = 10V	$T_J = 175^{\circ}C(Note 4)$	-	4.1	5.7	mΩ

Dynamic Characteristics

C _{iss}	Input Capacitance	V _{DS} = 25V, V _{GS} = 0V, f = 1MHz		-	3130	-	pF
C _{oss}	Output Capacitance			-	756	-	pF
C _{rss}	Reverse Transfer Capacitance			-	48	-	pF
R_g	Gate Resistance	f = 1MHz		-	2	-	Ω
$Q_{g(ToT)}$	Total Gate Charge at 10V	V _{GS} = 0 to 10V	V _{DD} = 20V	-	42	46	nC
Q _{g(th)}	Threshold Gate Charge	$V_{GS} = 0$ to 2V	I _D = 80A	-	6	7	nC
Q_{gs}	Gate-to-Source Gate Charge		_	-	16	-	nC
Q_{gd}	Gate-to-Drain "Miller" Charge			-	7.7	-	nC

Switching Characteristics

t _{on}	Turn-On Time		-	-	72	ns
t _{d(on)}	Turn-On Delay		-	23	-	ns
t _r	Rise Time	V_{DD} = 20V, I_{D} = 80A, V_{GS} = 10V, R_{GEN} = 6 Ω	-	22	-	ns
t _{d(off)}	Turn-Off Delay		-	41	-	ns
t _f	Fall Time		-	15	-	ns
t _{off}	Turn-Off Time		-	-	76	ns

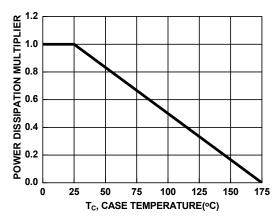
Drain-Source Diode Characteristics

V_{SD}	Source-to-Drain Diode Voltage	I _{SD} = 80A, V _{GS} = 0V	-	1.25	V	
	Source-to-Drain blode voltage	$I_{SD} = 40A, V_{GS} = 0V$	-	-	1.2	V
t _{rr}	Reverse-Recovery Time	$I_F = 80A$, $dI_{SD}/dt = 100A/\mu s$,	-	54	73	ns
Q _{rr}	Reverse-Recovery Charge	V _{DD} =32V	-	42	61	nC

Note:

4: The maximum value is specified by design at TJ = 175°C. Product is not tested to this condition in production.

Typical Characteristics



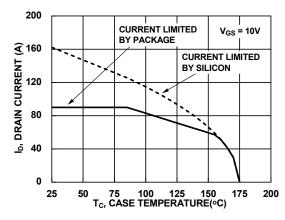


Figure 1. Normalized Power Dissipation vs. Case Temperature

Figure 2. Maximum Continuous Drain Current vs.

Case Temperature

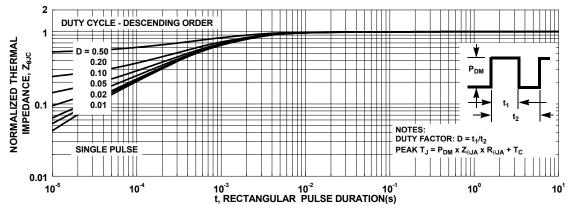


Figure 3. Normalized Maximum Transient Thermal Impedance

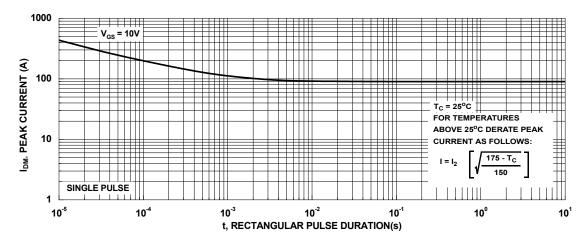


Figure 4. Peak Current Capability

Typical Characteristics

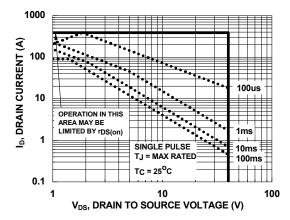
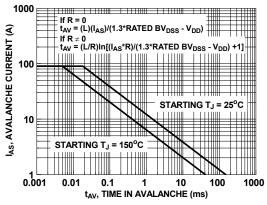


Figure 5. Forward Bias Safe Operating Area



NOTE: Refer to ON Semiconductor Application Notes AN7514 and AN7515

Figure 6. Unclamped Inductive Switching Capability

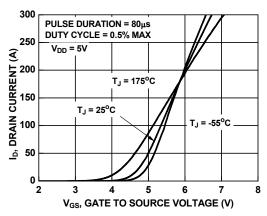


Figure 7. Transfer Characteristics

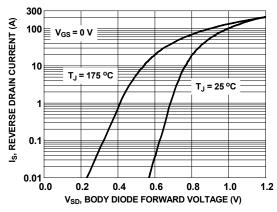


Figure 8. Forward Diode Characteristics

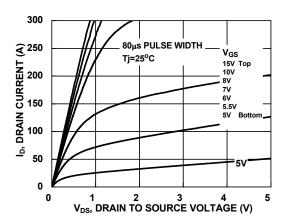


Figure 9. Saturation Characteristics

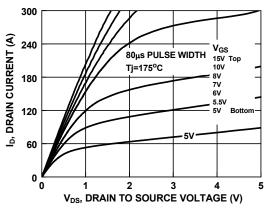


Figure 10. Saturation Characteristics

Typical Characteristics

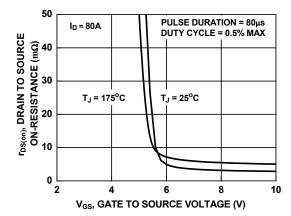


Figure 11. R_{DSON} vs. Gate Voltage

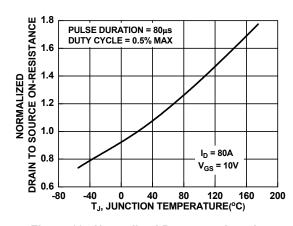


Figure 12. Normalized R_{DSON} vs. Junction Temperature

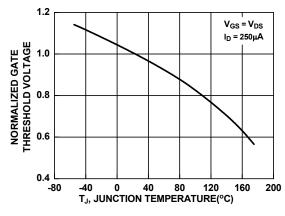


Figure 13. Normalized Gate Threshold Voltage vs. Temperature

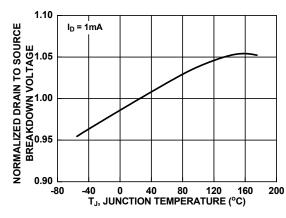


Figure 14. Normalized Drain--Source Breakdown Voltage vs. Junction Temperature

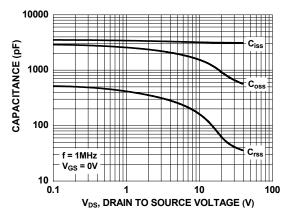


Figure 15. Capacitance vs. Drain--Source Voltage

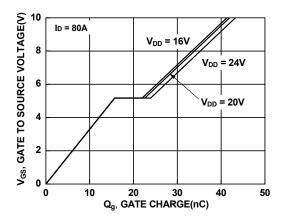


Figure 16. Gate Charge vs. Gate--Source Voltage

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