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FDFM2P110

Integrated P-Channel PowerTrench® MOSFET and Schottky Diode

General Description

FDFM2P110 combines the exceptional performance of Fairchild's PowerTrench MOSFET technology with a very low forward voltage drop Schottky barrier rectifier in a MicroFET package.

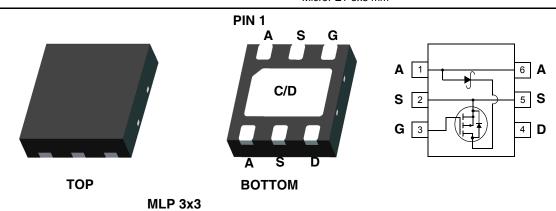
This device is designed specifically as a single package solution for Buck Boost. It features a fast switching, low gate charge MOSFET with very low on-state resistance.

Applications

■ Buck Boost

Features

- -3.5 A, -20 V $R_{DS(ON)} = 140 m\Omega$ @ $V_{GS} = -4.5 V$
 - $R_{DS(ON)} = 200 \text{m}\Omega @ V_{GS} = -2.5 \text{ V}$
- Low Profile 0.8 mm maximun in the new package MicroFET 3x3 mm



Absolute Maximum Ratings T_A = 25°C unless otherwise noted

Symbol	Parameter		Ratings	Units
V _{DSS}	Drain-Source Voltage		-20	V
V _{GSS}	Gate-Source Voltage		±12	V
ı	Drain Current -Continuous	(Note 1a)	-3.5	Α
ID	-Pulsed		-10	A
V _{RRM}	Schottky Repetitive Peak Reverse voltage		20	V
Io	Schottky Average Forward Current	(Note 1a)	2	Α
D	Power dissipation (Steady State)	(Note 1a)	2	W
P_{D}		(Note 1b)	0.8	VV
T _J , T _{STG}	Operating and Storage Junction Temperature Range		-55 to +150	°C

Thermal Characteristics

$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	(Note 1a)	60	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	(Note 1b)	145	°C/W

Package Marking and Ordering Information

Device Marking	Device	Reel Size	Tape Width	Quantity
2P110	FDFM2P110	7inch	12mm	3000 units

Electrical Characteristics T_A = 25°C unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Тур	Max	Units	
Off Characteristics							
B _{VDSS}	Drain-Source Breakdown Voltage	$I_D = -250 \mu A, V_{GS} = 0 V$	-20	-	-	V	
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	$I_D = -250\mu A$, Referenced to 25°C	-	-11	-	mV/°C	
I _{DSS}	Zero Gate Voltage Drain Current	$V_{GS} = 0V, V_{DS} = -16V$	-	-	-1	μА	
I_{GSS}	Gate-Body Leakage,	$V_{GS} = \pm 12V, V_{DS} = 0V$	-	-	±100	nA	

On Characteristics (Note 2)

$V_{GS(TH)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_{D} = -250 \mu A$	-0.6	-1.0	-1.5	V	
$\frac{\Delta V_{GS(TH)}}{\Delta T_J}$	Gate Threshold Voltage Temperature Coefficient	$I_D = -250 \mu A$, Referenced to 25°C	i	3	-	mV/°C	
	Static Drain-Source On-Resistance	$I_D = -3.5A, V_{GS} = -4.5V$	-	101	140		
R _{DS(ON)}		$I_D = -3.0A$, $V_{GS} = -2.5V$	ı	145	200	mΩ	
DS(ON)		$I_D = -3.5A$, $V_{GS} = -4.5V$, $T_J = 125^{\circ}C$	-	136	202	11122	
I _{D(ON)}	On-State Drain Current	$V_{GS} = -2.5V, V_{DS} = -5V$	-10	-	-	Α	
g _{FS}	Forward Transconductance	$I_D = -3.5A, V_{DS} = -5V$	-	6	-	S	

Dynamic Characteristics

C _{ISS}	Input Capacitance	V _{DS} = -10V, V _{GS} = 0V, f = 1MHz	-	280	-	pF
Coss	Output Capacitance		-	65	-	pF
C _{RSS}	Reverse Transfer Capacitance	I = TIVII IZ		35	-	pF
R_{G}	Gate Resistance	f = 1MHz	-	7	-	Ω

Switching Characteristics (Note 2)

t _{d(ON)}	Turn-On Delay Time		-	8	16	ns
t _r	Turn-On Rise Time	$V_{DD} = -10V, I_{D} = -1A$	-	12	22	ns
t _{d(OFF)}	Turn-Off Delay Time	$V_{GS} = -4.5V, R_{GEN} = 16\Omega$	-	11	20	ns
t _f	Turn-Off Fall Time		-	3.2	6.4	ns
Q_g	Total Gate Charge	V 10V I 0.5A	-	3	4	nC
Q_{gs}	Gate-Source Charge	$V_{DS} = -10V, I_{D} = -3.5A,$ $V_{GS} = -4.5V$	-	0.7	-	nC
Q_{gd}	Gate-Drain Charge		-	1	-	nC

Drain-Source Diode Characteristics and Maximum Ratings

I _S	Maximum Continuous Drain-Source Diode Forward Current			-	-2	Α
V_{SD}	Drain-Source Diode Forward Voltage $V_{GS} = 0V$, $I_S = -2$ A (Note 2)		-	-0.9	-1.2	V
t _{rr}	Diode Reverse Recovery Time	I _E = -3.5A, dI _E /dt=100A/μs	-	13	-	ns
Q_{rr}	Diode Reverse Recovery Charge	1 _F = -3.3A, αι _F /αι=100A/μS	ı	3	•	nC

Schottky Diode Characteristic

V_{R}	Reverse Voltage	I _R = 1mA		20	-	-	V
1_	Povorco Logicado	V _R = 5V	$T_J = 25^{\circ}C$	-		100	μΑ
^I R	Reverse Leakage		$T_J = 100^{\circ}C$		-	10	mA
V_{F}	Forward Voltage	I _F = 1A	$T_J = 25^{\circ}C$	-	0.32	0.39	V

Electrical Characteristics $T_A = 25$ °C unless otherwise noted

Notes

1. $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta CA}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.



a) 60°C/W when mounted on a 1in² pad of 2 oz copper

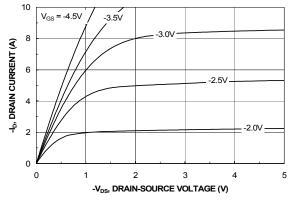


b) 145°C/W whe mounted on a minimum pad of 2 oz copper

Scale 1: 1 on letter size paper

2. Pulse Test: Pulse Width < 300 μ s, Duty Cycle < 2.0%

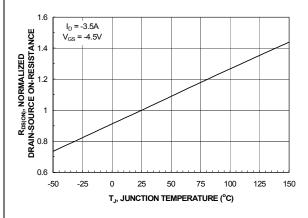
Typical Characteristics



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Figure 1. On-Region Characteristics

Figure 2. On-Resistance Variation with Drain Current and Gate Voltage



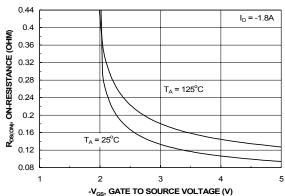
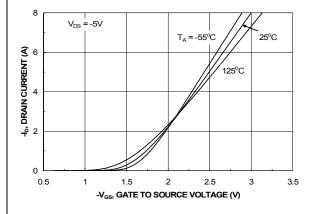


Figure 3. On-Resistance Variation with Temperature

Figure 4. On-Resistance Variation with Gate-to-Source Voltage



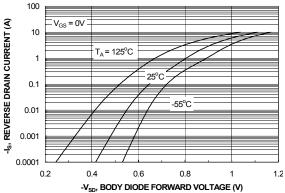
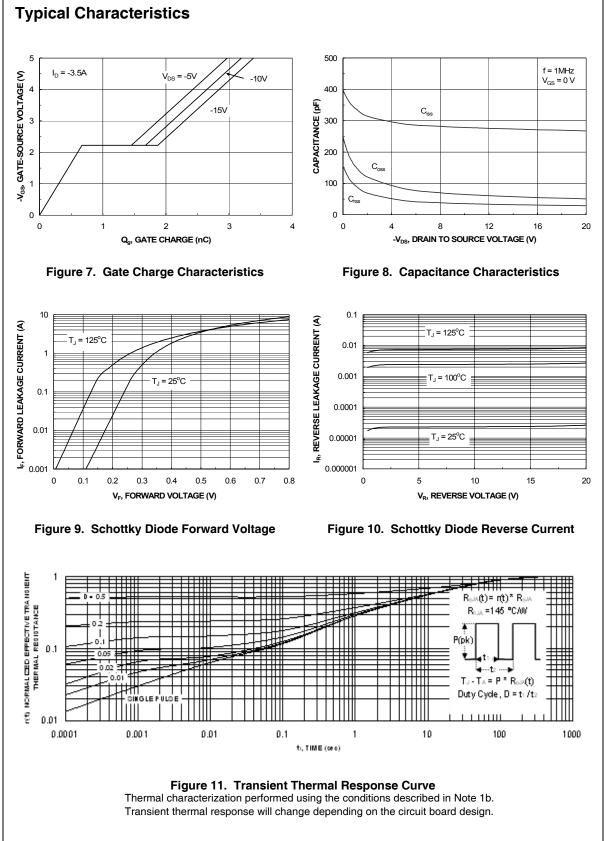
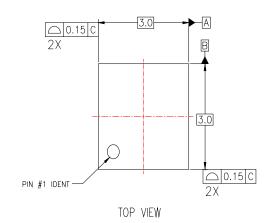
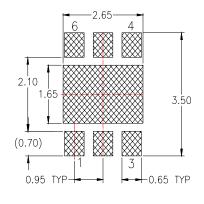


Figure 5. Transfer Characteristics

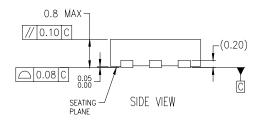
Figure 6. Body Diode Forward Voltage Variation with Source Current and Temperature

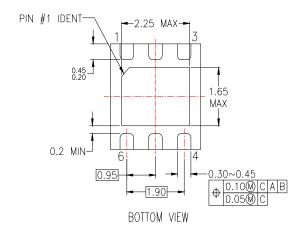


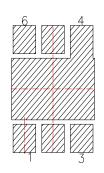




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NOTES:

- A. CONFORMS TO JEDEC REGISTRATION MO-229, VARIATION WEEA, DATED 11/2001
- B. DIMENSIONS ARE IN MILLIMETERS.
- C. DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994

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