

# ON Semiconductor

## Is Now

The logo for onsemi, featuring the word "onsemi" in a dark teal, lowercase, sans-serif font. The letter "i" is stylized with a white dot and a teal vertical bar. A small orange triangle is positioned above the top right of the "i". A trademark symbol (TM) is located to the right of the logo.

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ON Semiconductor®

# FDG6332C-F085

## 20V N & P-Channel PowerTrench® MOSFETs

### Features

- **Q1** 0.7 A, 20V.  $R_{DS(ON)} = 300\text{ m}\Omega @ V_{GS} = 4.5\text{ V}$   
 $R_{DS(ON)} = 400\text{ m}\Omega @ V_{GS} = 2.5\text{ V}$
- **Q2** -0.6 A, -20V.  $R_{DS(ON)} = 420\text{ m}\Omega @ V_{GS} = -4.5\text{ V}$   
 $R_{DS(ON)} = 630\text{ m}\Omega @ V_{GS} = -2.5\text{ V}$
- Low gate charge
- High performance trench technology for extremely low  $R_{DS(ON)}$
- SC70-6 package: small footprint (51% smaller than SSOT-6); low profile (1mm thick)
- Qualified to AEC Q101
- RoHS Compliant



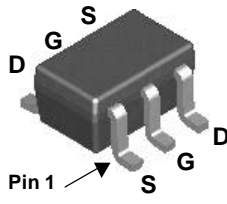
### General Description

The N & P-Channel MOSFETs are produced using ON Semiconductor's advanced PowerTrench process that has been especially tailored to minimize on-state resistance and yet maintain superior switching performance.

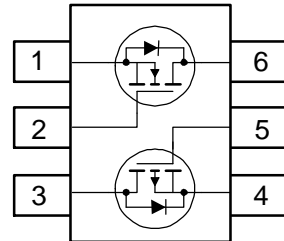
These devices have been designed to offer exceptional power dissipation in a very small footprint for applications where the bigger more expensive TSSOP-8 and SSOP-6 packages are impractical.

### Applications

- DC/DC converter
- Load switch
- LCD display inverter



SC70-6



Complementary

### Absolute Maximum Ratings T<sub>A</sub>=25°C unless otherwise noted

Symbol	Parameter	Q1	Q2	Units
V <sub>DSS</sub>	Drain-Source Voltage	20	-20	V
V <sub>GSS</sub>	Gate-Source Voltage	±12	±12	V
I <sub>D</sub>	Drain Current – Continuous (Note 1)	0.7	-0.6	A
	– Pulsed	2.1	-2	
P <sub>D</sub>	Power Dissipation for Single Operation (Note 1)	0.3		W
T <sub>J</sub> , T <sub>STG</sub>	Operating and Storage Junction Temperature Range	-55 to +150		°C

### Thermal Characteristics

R <sub>θJA</sub>	Thermal Resistance, Junction-to-Ambient (Note 1)	415	°C/W
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### Package Marking and Ordering Information

Device Marking	Device	Reel Size	Tape width	Quantity
.32	FDG6332C-F085	7"	8mm	3000 units

FDG6332C-F085 20V N & P-Channel PowerTrench MOSFETs

## Electrical Characteristics

$T_A = 25^\circ\text{C}$  unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
<b>Off Characteristics</b>						
$BV_{DSS}$	Drain-Source Breakdown Voltage	$V_{GS} = 0\text{ V}, I_D = 250\ \mu\text{A}$ $V_{GS} = 0\text{ V}, I_D = -250\ \mu\text{A}$	Q1 20 Q2 -20			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	$I_D = 250\ \mu\text{A}, \text{Ref. to } 25^\circ\text{C}$ $I_D = -250\ \mu\text{A}, \text{Ref. to } 25^\circ\text{C}$	Q1 Q2	14 -14		mV/°C
$I_{DSS}$	Zero Gate Voltage Drain Current	$V_{DS} = 16\text{ V}, V_{GS} = 0\text{ V}$ $V_{DS} = -16\text{ V}, V_{GS} = 0\text{ V}$	Q1 Q2		1 -1	$\mu\text{A}$
$I_{GSSF} / I_{GSSR}$	Gate-Body Leakage, Forward	$V_{GS} = \pm 12\text{ V}, V_{DS} = 0\text{ V}$			$\pm 100$	nA
$I_{GSSF} / I_{GSSR}$	Gate-Body Leakage, Reverse	$V_{GS} = \pm 12\text{ V}, V_{DS} = 0\text{ V}$			$\pm 100$	nA
<b>On Characteristics (Note 2)</b>						
$V_{GS(th)}$	Gate Threshold Voltage	Q1 $V_{DS} = V_{GS}, I_D = 250\ \mu\text{A}$ Q2 $V_{DS} = V_{GS}, I_D = -250\ \mu\text{A}$	0.6 -0.6	1.1 -1.2	1.5 -1.5	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate Threshold Voltage Temperature Coefficient	Q1 $I_D = 250\ \mu\text{A}, \text{Ref. To } 25^\circ\text{C}$ Q2 $I_D = -250\ \mu\text{A}, \text{Ref. to } 25^\circ\text{C}$		-2.8 3		mV/°C
$R_{DS(on)}$	Static Drain-Source On-Resistance	Q1 $V_{GS} = 4.5\text{ V}, I_D = 0.7\text{ A}$ $V_{GS} = 2.5\text{ V}, I_D = 0.6\text{ A}$ $V_{GS} = 4.5\text{ V}, I_D = 0.7\text{ A}, T_J = 125^\circ\text{C}$ Q2 $V_{GS} = -4.5\text{ V}, I_D = -0.6\text{ A}$ $V_{GS} = -2.5\text{ V}, I_D = -0.5\text{ A}$ $V_{GS} = -4.5\text{ V}, I_D = -0.6\text{ A}, T_J = 125^\circ\text{C}$		180 293 247	300 400 442	m $\Omega$
$g_{FS}$	Forward Transconductance	Q1 $V_{DS} = 5\text{ V}, I_D = 0.7\text{ A}$ Q2 $V_{DS} = -5\text{ V}, I_D = -0.6\text{ A}$		2.8 1.8		S
$I_{D(on)}$	On-State Drain Current	Q1 $V_{GS} = 4.5\text{ V}, V_{DS} = 5\text{ V}$ Q2 $V_{GS} = -4.5\text{ V}, V_{DS} = -5\text{ V}$	1 -2			A
<b>Dynamic Characteristics</b>						
$C_{iss}$	Input Capacitance	Q1 $V_{DS} = 10\text{ V}, V_{GS} = 0\text{ V}, f = 1.0\text{ MHz}$ Q2 $V_{DS} = -10\text{ V}, V_{GS} = 0\text{ V}, f = 1.0\text{ MHz}$		113 114		pF
$C_{oss}$	Output Capacitance	Q1 $V_{DS} = 10\text{ V}, V_{GS} = 0\text{ V}, f = 1.0\text{ MHz}$ Q2 $V_{DS} = -10\text{ V}, V_{GS} = 0\text{ V}, f = 1.0\text{ MHz}$		34 24		pF
$C_{riss}$	Reverse Transfer Capacitance	Q1 $V_{DS} = 10\text{ V}, V_{GS} = 0\text{ V}, f = 1.0\text{ MHz}$ Q2 $V_{DS} = -10\text{ V}, V_{GS} = 0\text{ V}, f = 1.0\text{ MHz}$		16 9		pF
<b>Switching Characteristics (Note 2)</b>						
$t_{d(on)}$	Turn-On Delay Time	Q1 For Q1: $V_{DS} = 10\text{ V}, I_D = 1\text{ A}$ Q2 $V_{GS} = 4.5\text{ V}, R_{GEN} = 6\ \Omega$		5 5.5	10 11	ns
$t_r$	Turn-On Rise Time	Q1 For Q1: $V_{DS} = 10\text{ V}, I_D = 1\text{ A}$ Q2 $V_{GS} = 4.5\text{ V}, R_{GEN} = 6\ \Omega$		7 14	15 25	ns
$t_{d(off)}$	Turn-Off Delay Time	Q1 $V_{DS} = -10\text{ V}, I_D = -1\text{ A}$ Q2 $V_{GS} = -4.5\text{ V}, R_{GEN} = 6\ \Omega$		9 6	18 12	ns
$t_f$	Turn-Off Fall Time	Q1 $V_{DS} = -10\text{ V}, I_D = -1\text{ A}$ Q2 $V_{GS} = -4.5\text{ V}, R_{GEN} = 6\ \Omega$		1.5 1.7	3 3.4	ns
$Q_g$	Total Gate Charge	Q1 For Q1: $V_{DS} = 10\text{ V}, I_D = 0.7\text{ A}$ Q2 $V_{GS} = 4.5\text{ V}, R_{GEN} = 6\ \Omega$		1.1 1.4	1.5 2	nC
$Q_{gs}$	Gate-Source Charge	Q1 For Q1: $V_{DS} = 10\text{ V}, I_D = 0.7\text{ A}$ Q2 $V_{GS} = 4.5\text{ V}, R_{GEN} = 6\ \Omega$		0.24 0.3		nC
$Q_{gd}$	Gate-Drain Charge	Q1 $V_{DS} = -10\text{ V}, I_D = -0.6\text{ A}$ Q2 $V_{GS} = -4.5\text{ V}, R_{GEN} = 6\ \Omega$		0.3 0.4		nC

### Electrical Characteristics

$T_A = 25^\circ\text{C}$  unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units	
<b>Drain–Source Diode Characteristics and Maximum Ratings</b>							
$I_S$	Maximum Continuous Drain–Source Diode Forward Current	Q1			0.25	A	
		Q2			–0.25		
$V_{SD}$	Drain–Source Diode Forward Voltage	Q1	$V_{GS} = 0\text{ V}, I_S = 0.25\text{ A}$ (Note 2)		0.74	1.2	V
		Q2	$V_{GS} = 0\text{ V}, I_S = -0.25\text{ A}$ (Note 2)		–0.77	–1.2	

**Notes:**

1.  $R_{\theta JA}$  is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins.  $R_{\theta JC}$  is guaranteed by design while  $R_{\theta JA}$  is determined by the user's board design.  $R_{\theta JA} = 415^\circ\text{C/W}$  when mounted on a minimum pad of FR-4 PCB in a still air environment.

2. Pulse Test: Pulse Width < 300 $\mu\text{s}$ , Duty Cycle < 2.0%

### Typical Characteristics: N-Channel

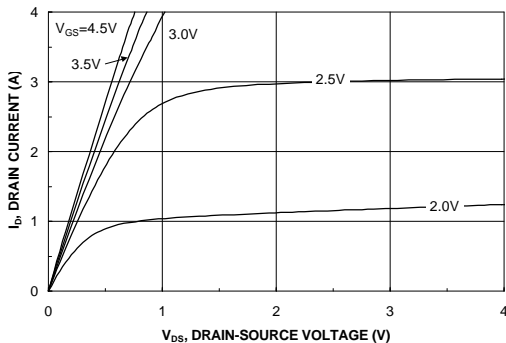


Figure 1. On-Region Characteristics.

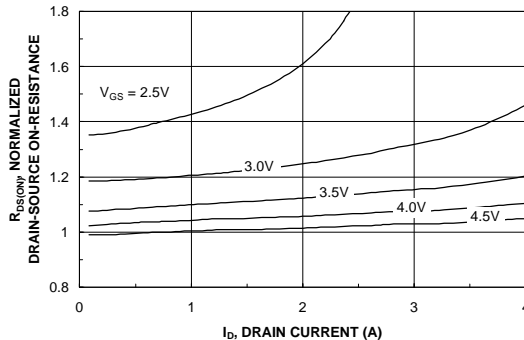


Figure 2. On-Resistance Variation with Drain Current and Gate Voltage.

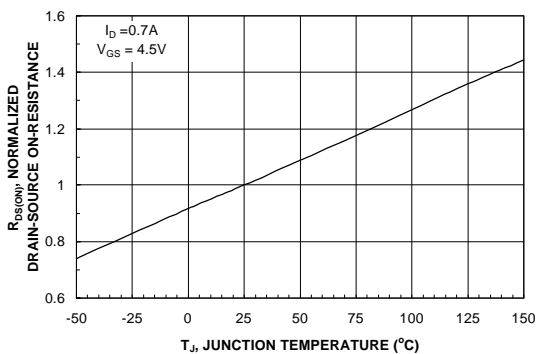


Figure 3. On-Resistance Variation with Temperature.

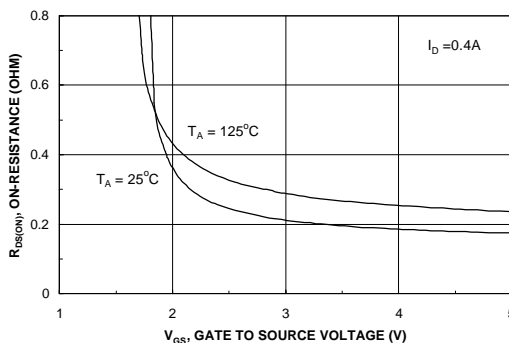


Figure 4. On-Resistance Variation with Gate-to-Source Voltage.

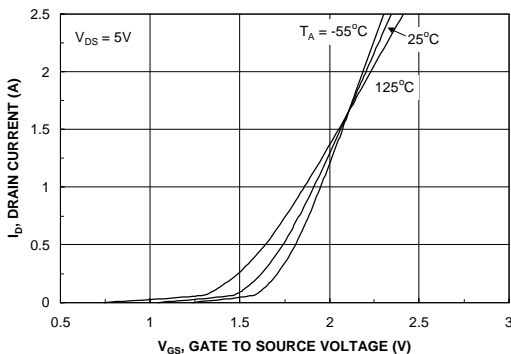


Figure 5. Transfer Characteristics.

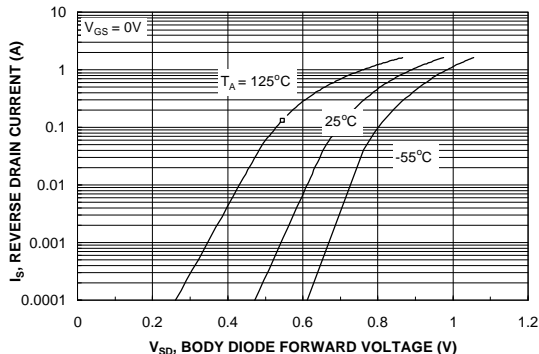


Figure 6. Body Diode Forward Voltage Variation with Source Current and Temperature.

## Typical Characteristics: N-Channel

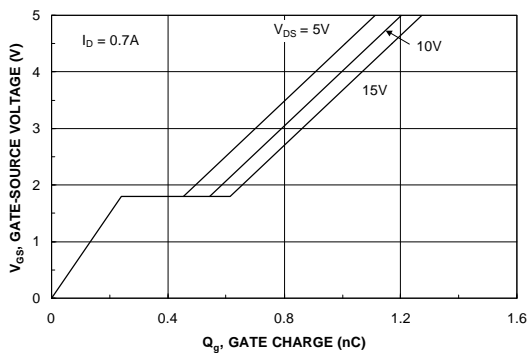


Figure 7. Gate Charge Characteristics.

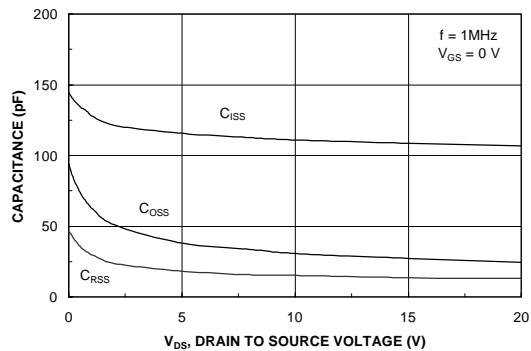


Figure 8. Capacitance Characteristics.

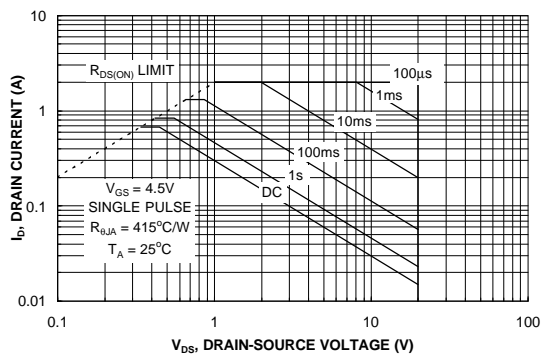


Figure 9. Maximum Safe Operating Area.

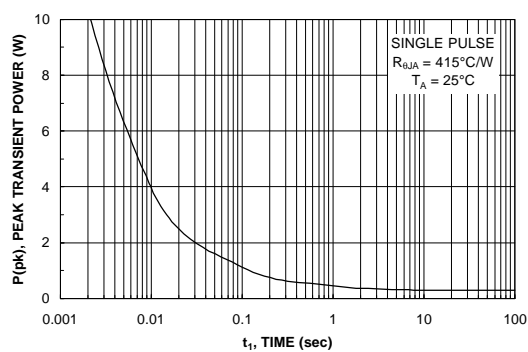


Figure 10. Single Pulse Maximum Power Dissipation.

### Typical Characteristics: P-Channel

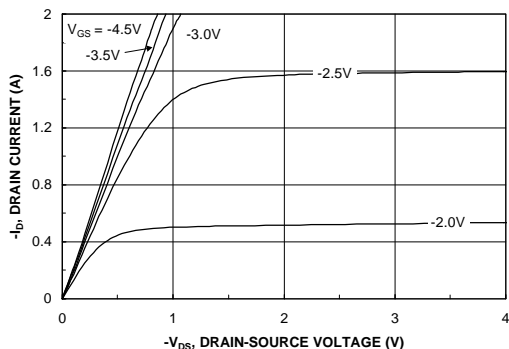


Figure 11. On-Region Characteristics.

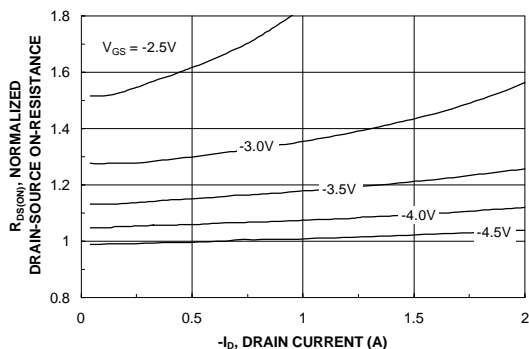


Figure 12. On-Resistance Variation with Drain Current and Gate Voltage.

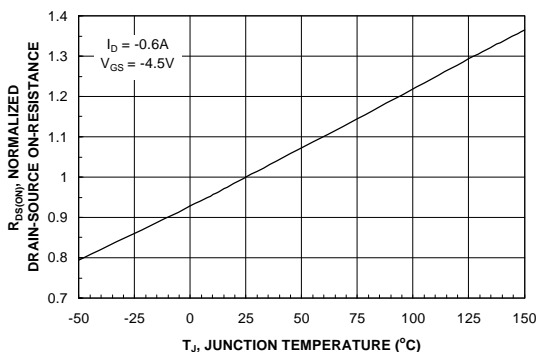


Figure 13. On-Resistance Variation with Temperature.

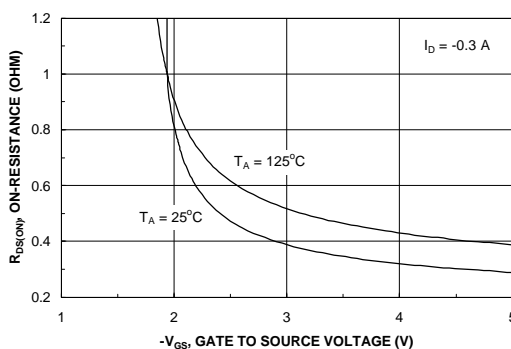


Figure 14. On-Resistance Variation with Gate-to-Source Voltage.

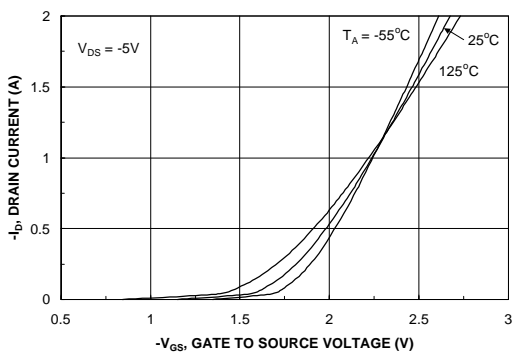


Figure 15. Transfer Characteristics.

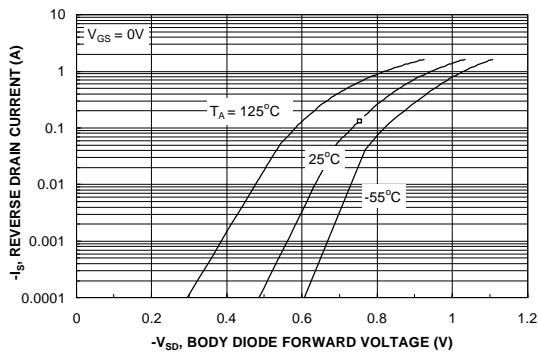
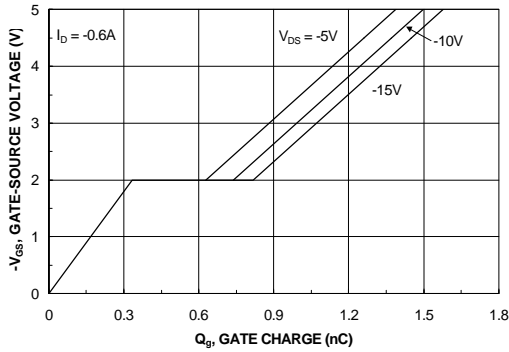
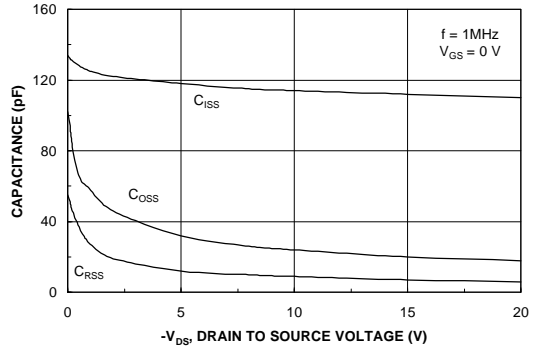


Figure 16. Body Diode Forward Voltage Variation with Source Current and Temperature.

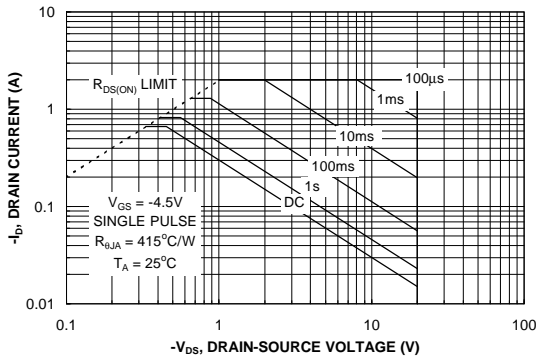
**Typical Characteristics: P-Channel**



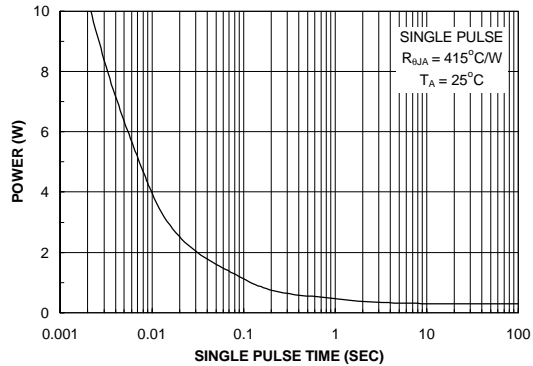
**Figure 17. Gate Charge Characteristics.**



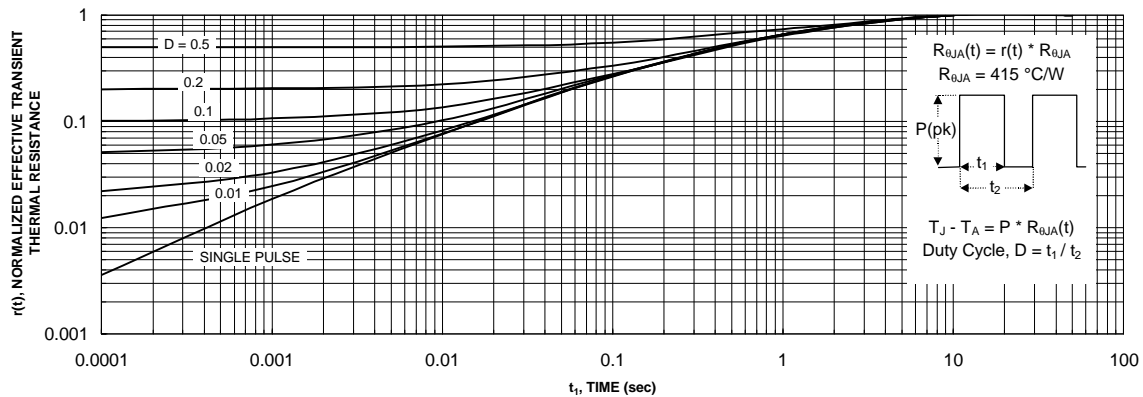
**Figure 18. Capacitance Characteristics.**



**Figure 19. Maximum Safe Operating Area.**



**Figure 20. Single Pulse Maximum Power Dissipation.**



**Figure 21. Transient Thermal Response Curve.**

Thermal characterization performed using the conditions described in Note 1. Transient thermal response will change depending on the circuit board design.



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