MOSFET – N-Channel, UniFET™, FRFET®

500 V, 45 A, 120 mΩ

FDH45N50F

Description

UniFET MOSFET is ON Semiconductor's high voltage MOSFET family based on planar stripe and DMOS technology. This MOSFET is tailored to reduce on−state resistance, and to provide better switching performance and higher avalanche energy strength. The body diode's reverse recovery performance of UniFET FRFET MOSFET has been enhanced by lifetime control. Its t_{rr} is less than 100 nsec and the reverse dv/dt immunity is 15 V/ns while normal planar MOSFETs have over 200 nsec and 4.5 V/nsec respectively. Therefore, it can remove additional component and improve system reliability in certain applications in which the performance of MOSFET's body diode is significant. This device family is suitable for switching power converter applications such as power factor correction (PFC), flat panel display (FPD) TV power, ATX and electronic lamp ballasts.

Features

- $R_{DS(on)}$ = 105 mΩ (Typ.) @ V_{GS} = 10 V, I_D = 22.5 A
- Low Gate Charge (Typ. 105 nC)
- Low C_{rss} (Typ. 62 pF)
- 100% Avalanche Tested
- These Devices are Pb−Free, Halogen Free/BFR Free and are RoHS Compliant

Applications

- Lighting
- Uninterruptible Power Supply
- AC−DC Power Supply

ON Semiconductor®

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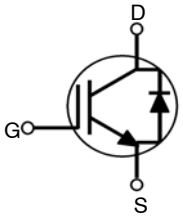
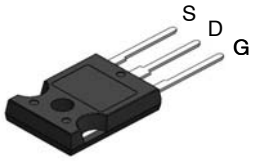
V_{DS}	$R_{DS(ON)}$ MAX	I_D MAX
500 V	120 mΩ @ 10 V	45 A

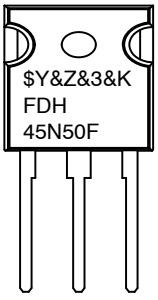


N-CHANNEL MOSFET



TO−247−3LD
CASE 340CK

MARKING DIAGRAM



$Y	= ON Semiconductor Logo
&Z	= Assembly Plant Code
&3	= Numeric Date Code
&K	= Lot Code
FDH45N50F	= Specific Device Code

ORDERING INFORMATION

See detailed ordering and shipping information on page 2 of this data sheet.

ABSOLUTE MAXIMUM RATINGS (T_C = 25°C unless otherwise noted)

Symbol	Parameter		FDH45N50F−F133	Unit
V_{DSS}	Drain to Source Voltage		500	V
I_D	Drain Current −	−Continuous (T_C = 25°C) −Continuous (T_C = 100°C)	45 28.4	A A
I_{DM}	Drain Current	−Pulsed (Note 1)	180	A
V_{GSS}	Gate−Source Voltage		±30	V
E_{AS}	Single Pulsed Avalanche Energy (Note 2)		1868	mJ
I_{AR}	Avalanche Current (Note 1)		45	A
E_{AR}	Repetitive Avalanche Energy (Note 1)		62.5	mJ
dv/dt	Peak Diode Recovery dv/dt (Note 3)		50	V/ns
P_D	Power Dissipation	(T_C = 25°C) −Derate Above 25°C	625 5	W W/°C
T_J, T_{STG}	Operating and Storage Temperature Range		−55 to + 150	°C
T_L	Maximum Lead Temperature for Soldering, 1/8″ from Case for 5 Second		300	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Repetitive Rating: Pulse width limited by maximum junction temperature.
2. L = 1.46 mH, I_{AS} = 48 A, V_{DD} = 50 V, R_G = 25 Ω, Starting T_J = 25 °C.
3. I_{SD} ≤ 45 A, di/dt ≤ 200 A/μs, V_{DD} ≤ BV_{DSS}, Starting T_J = 25 °C.

PACKAGE MARKING AND ORDERING INFORMATION

Device Marking	Device	Package	Package Method	Reel Size	Tape Width	Quantity
FDH45N50F−F133	FDH45N50F	TO−247−3	Tube	−	−	30 Units

THERMAL CHARACTERISTICS

Symbol	Parameter	FDH45N50F−F133	Unit
$R_{\theta JC}$	Thermal Resistance, Junction to Case, Max.	0.2	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient, Max.	40	

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
OFF CHARACTERISTICS						
BV_{DSS}	Drain to Source Breakdown Voltage	I_D = 250 μA, V_{GS} = 0 V	500	–	–	V
ΔBV_{DSS} / ΔT_J	Breakdown Voltage Temperature Coefficient	I_D = 250 μA, Referenced to 25°C	–	0.5	–	V/°C
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 500 V, V_{GS} = 0 V	–	–	25	μA
		V_{DS} = 400 V, T_C = 125°C	–	–	250	μA
I_{GSSF}	Gate−Body Leakage Current, Forward	V_{GS} = 30 V, V_{DS} = 0 V	–	–	100	nA
I_{GSSR}	Gate−Body Leakage Current, Reverse	V_{GS} = −30 V, V_{DS} = 0 V	–	–	−100	nA
ON CHARACTERISTICS						
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = 250 μA	3	–	5	V
$R_{DS(on)}$	Static Drain−Source On−Resistance	V_{GS} = 10 V, I_D = 22.5 A	–	0.105	0.12	Ω
g_{FS}	Forward Transconductance	V_{DS} = 40 V, I_D = 22.5 A	–	49	–	S
DYNAMIC CHARACTERISTICS						
C_{iss}	Input Capacitance	V_{DS} = 25 V, V_{GS} = 0 V, f = 1 MHz	–	5100	6630	pF
C_{oss}	Output Capacitance		–	790	1030	pF
C_{rss}	Reverse Transfer Capacitance		–	62	–	pF
C_{oss}	Output Capacitance	V_{DS} = 400 V, V_{GS} = 0 V, f = 1 MHz	–	161	–	pF
C_{oss}eff.	Effective Output Capacitance	V_{DS} = 0 V to 400 V, V_{GS} = 0 V	–	342	–	pF
SWITCHING CHARACTERISTICS						
$t_{d(on)}$	Turn-On Delay Time	V_{DD} = 250 V, I_D = 48 A, V_{GS} = 10 V, R_G = 25 Ω (Note 4)	–	140	290	ns
t_r	Turn−On Rise Time		–	500	1010	ns
$t_{d(off)}$	Turn-Off Delay Time		–	215	440	ns
t_f	Turn−Off Fall Time		–	245	500	ns
Q_g	Total Gate Charge	V_{DS} = 400 V, I_D = 48 A, V_{GS} = 10 V (Note 4)	–	105	137	nC
Q_{gs}	Gate−Source Charge		–	33	–	nC
Q_{gd}	Gate−Drain Charge		–	45	–	nC
DRAIN-SOURCE DIODE CHARACTERISTICS AND MAXIMUM RATINGS						
I_S	Maximum Continuous Drain−Source Diode Forward Current		–	–	45	A
I_{SM}	Maximum Pulsed Drain−Source Diode Forward Current		–	–	180	A
V_{SD}	Source to Drain Diode Voltage	V_{GS} = 0 V, I_S = 45 A	–	–	1.4	V
t_{rr}	Reverse Recovery Time	V_{GS} = 0 V, I_S = 45 A, dI_F/dt = 100 A/μs	–	188	–	ns
Q_{rr}	Reverse Recovery Charge		–	0.64	–	μC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

4. Essentially Independent of Operating Temperature Typical Characteristics.

TYPICAL CHARACTERISTICS

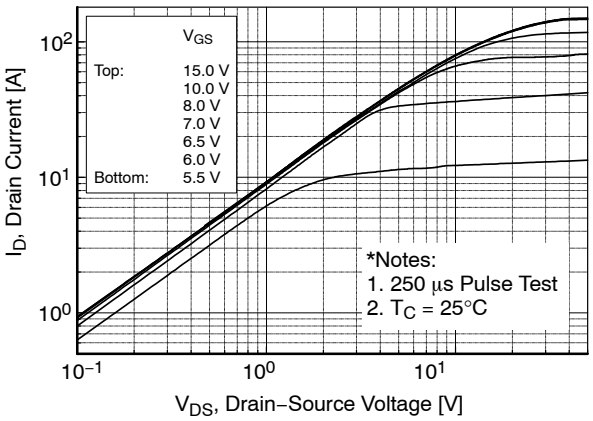


Figure 1. On−Region Characteristics

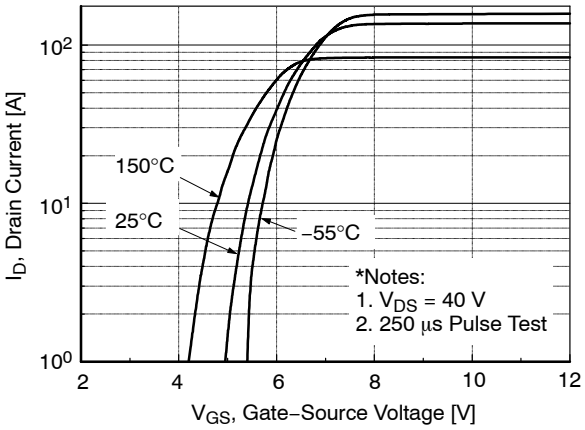


Figure 2. Transfer Characteristics

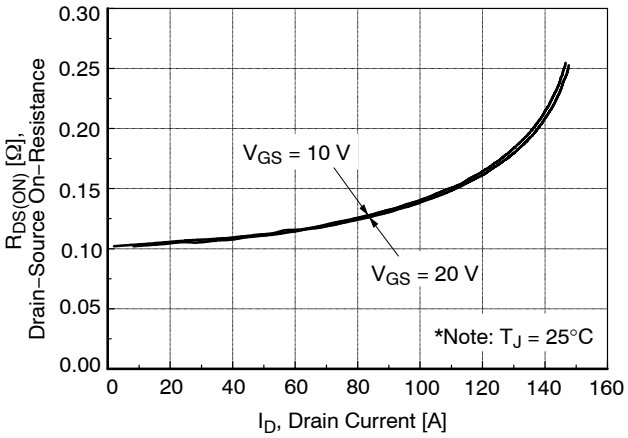


Figure 3. On−Resistance Variation vs. Drain Current and Gate voltage

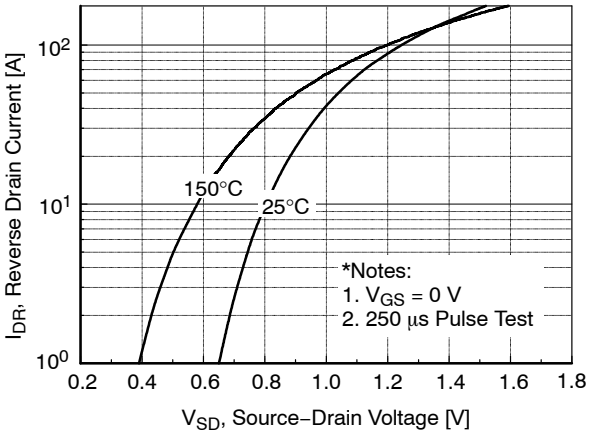


Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature

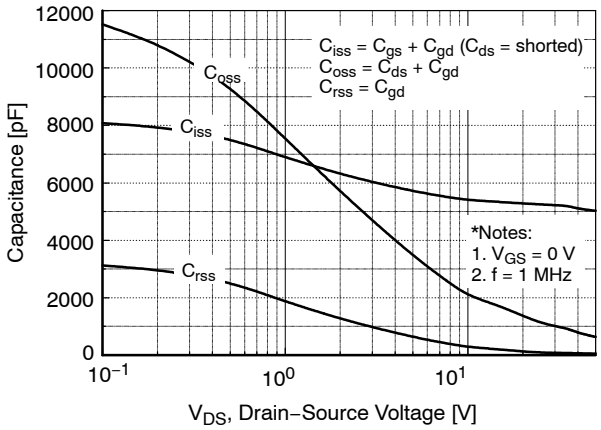


Figure 5. Capacitance Characteristics

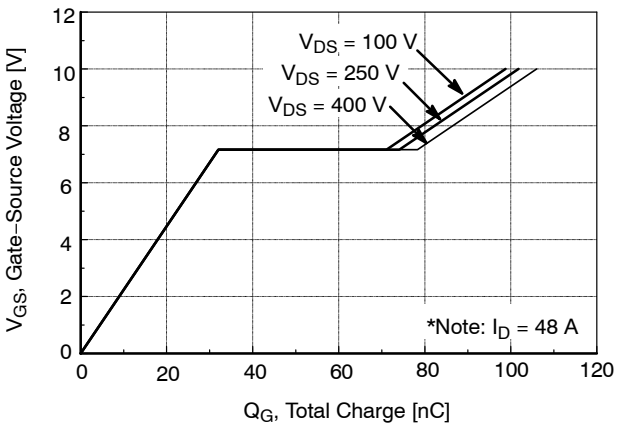


Figure 6. Gate Charge Characteristics

TYPICAL CHARACTERISTICS

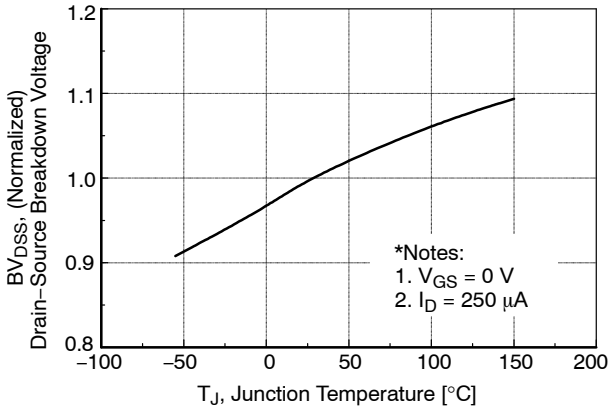


Figure 7. Breakdown Voltage Variation vs. Temperature

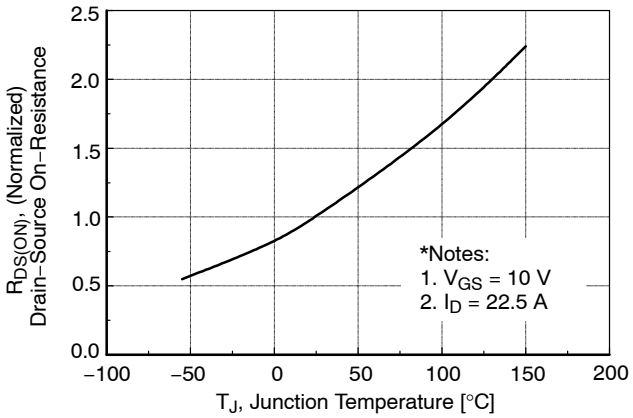


Figure 8. On−Resistance Variation vs. Temperature

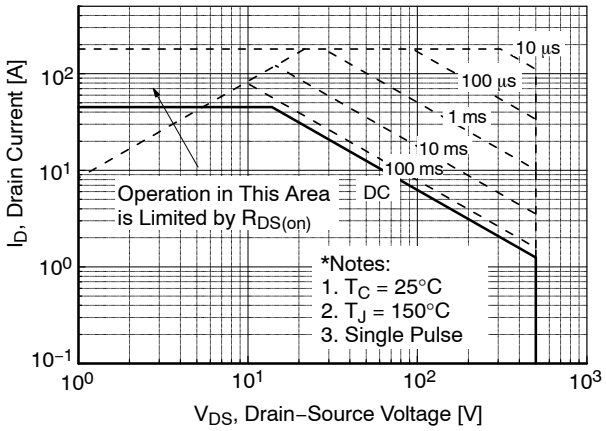


Figure 9. Maximum Safe Operating Area

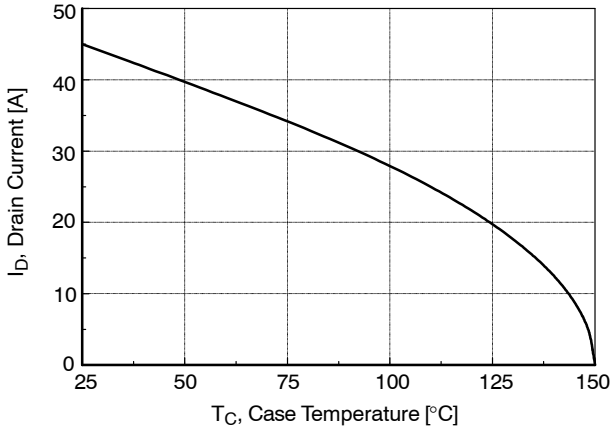


Figure 10. Maximum Drain Current vs. Case Temperature

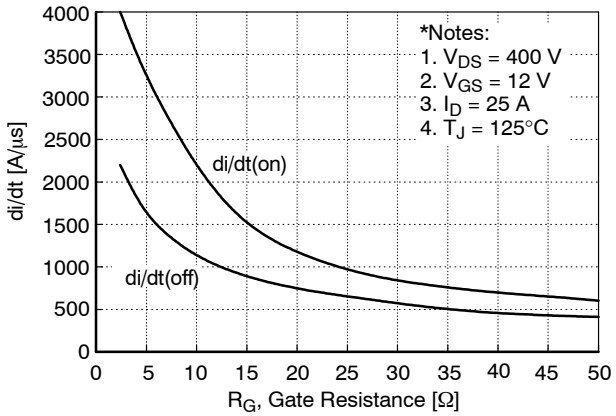


Figure 11. Typical Drain Current Slope vs. Gate Resistance

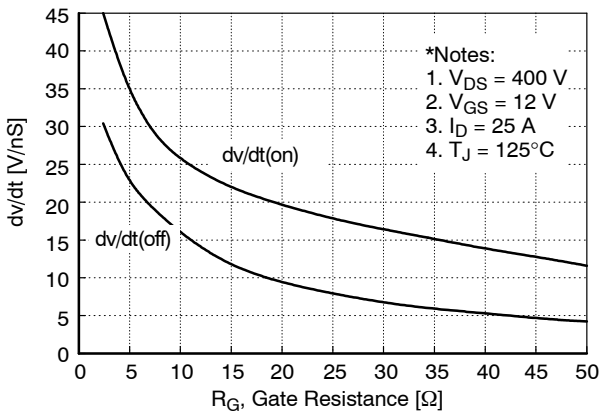


Figure 12. Typical Drain−Source Voltage Slope vs. Gate Resistance

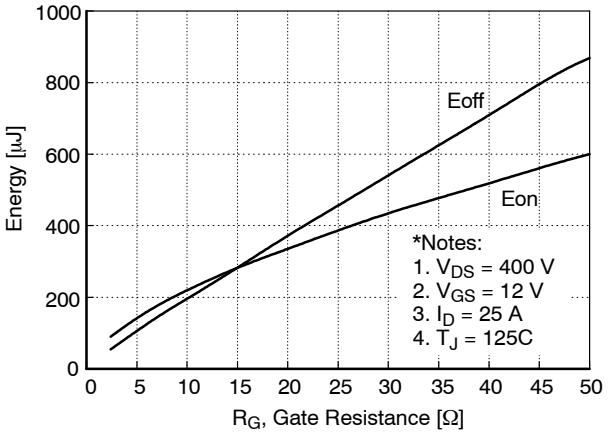


Figure 13. Typical Switching Losses vs. Gate Resistance

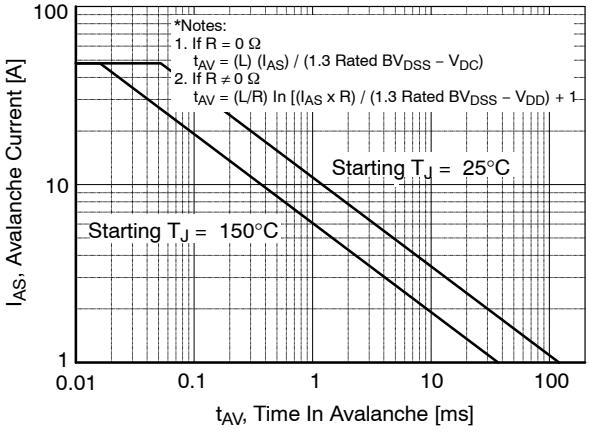


Figure 14. Unclamped Inductive Switching Capability

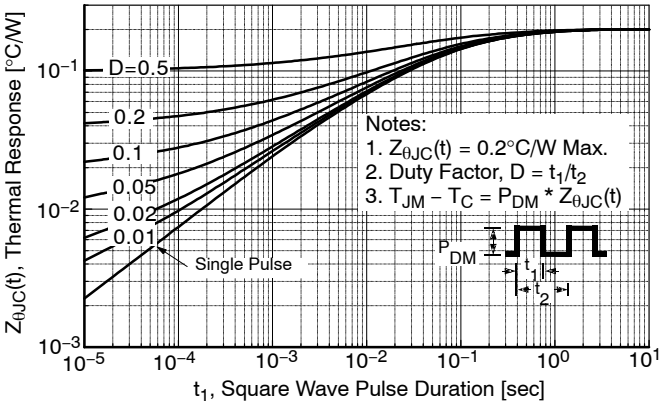


Figure 15. Transient Thermal Resistance Curve

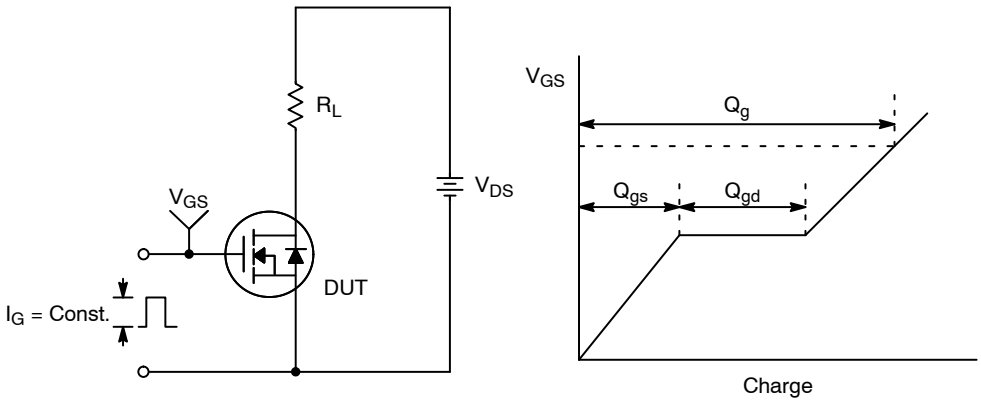


Figure 16. Gate Charge Test Circuit & Waveform

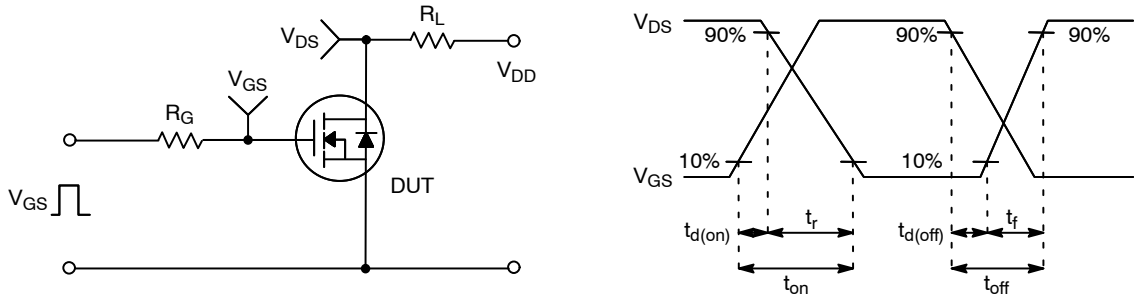


Figure 17. Resistive Switching Test Circuit & Waveforms

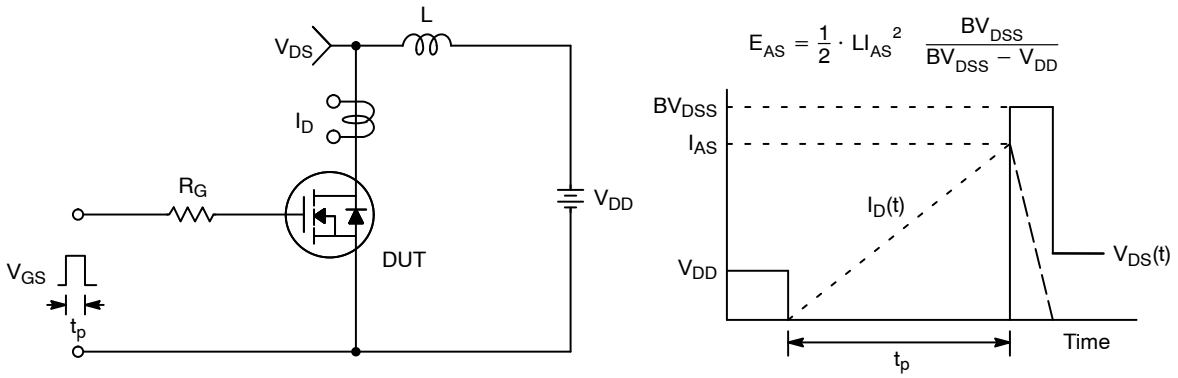


Figure 18. Unclamped Inductive Switching Test Circuit & Waveforms

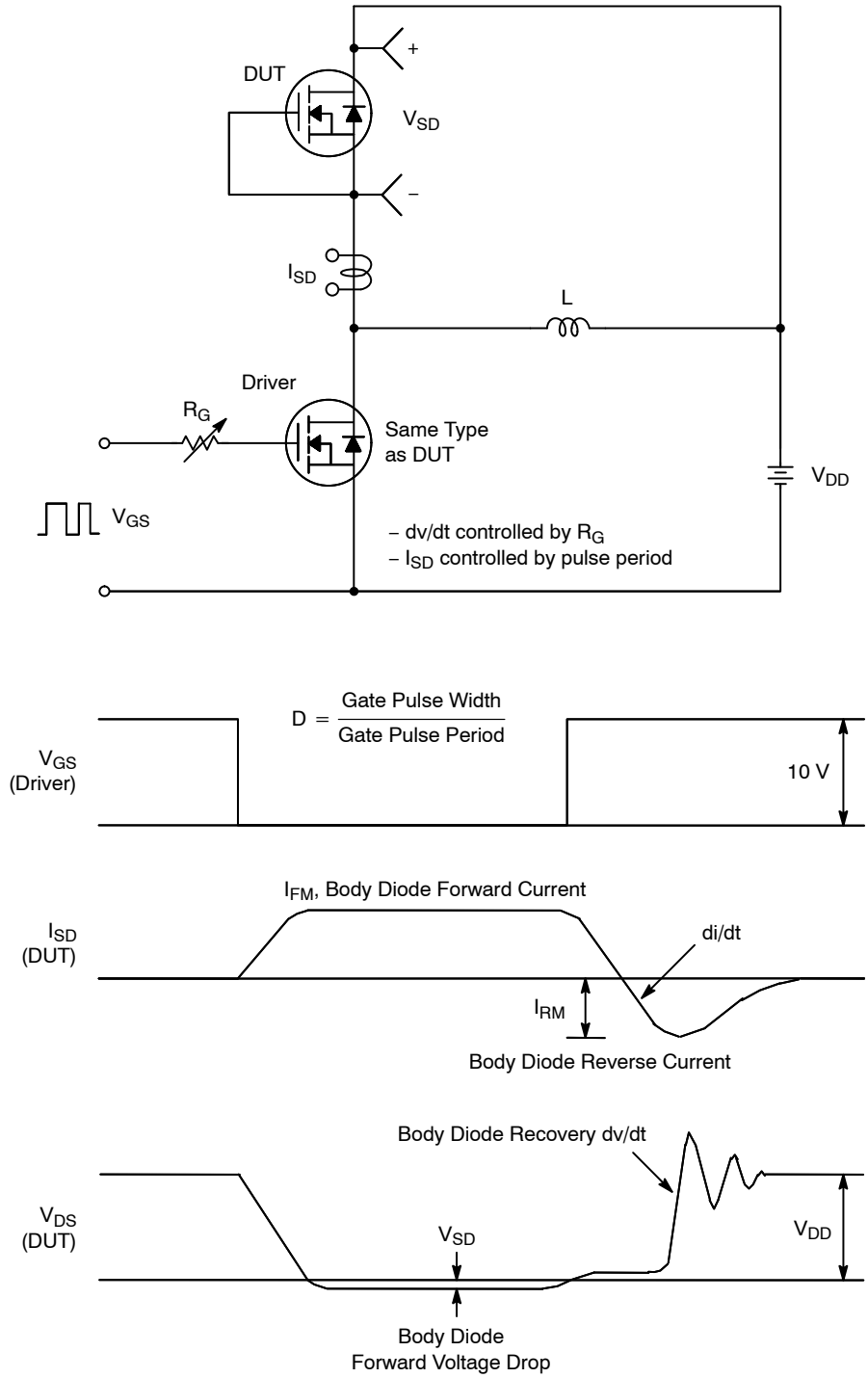


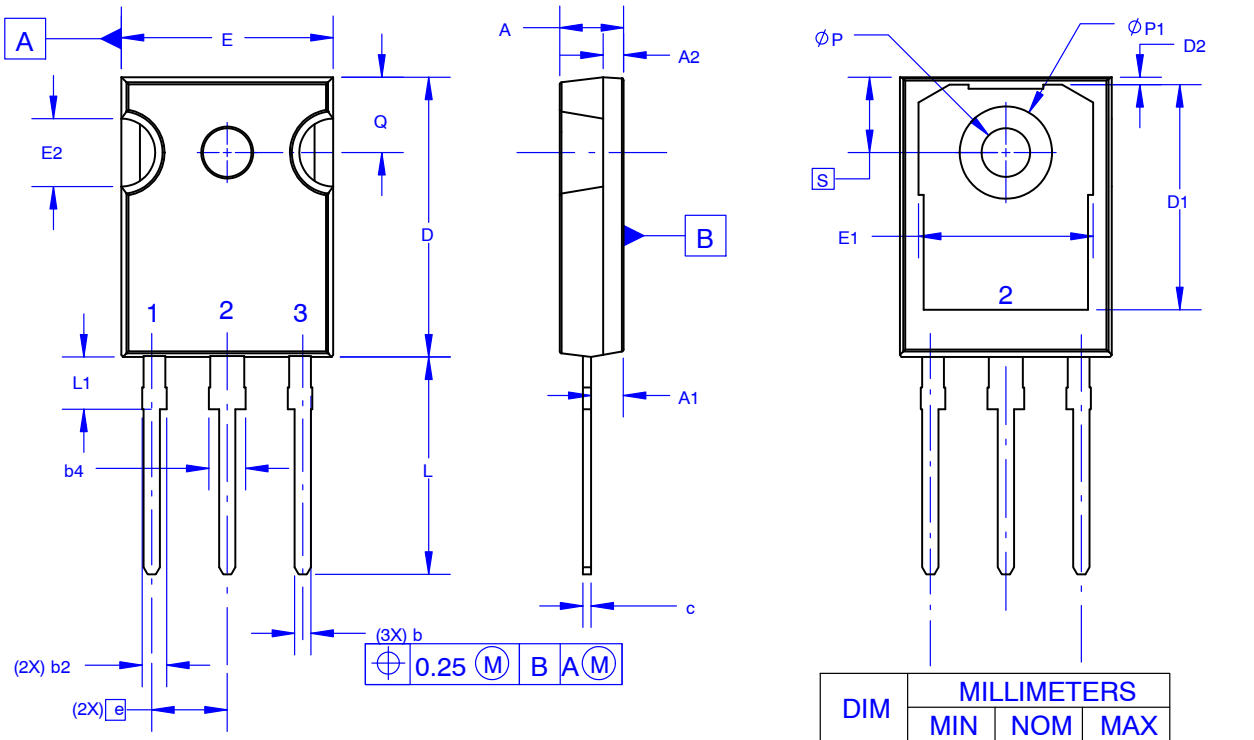
Figure 19. Peak Diode Recovery dv/dt Test Circuit & Waveforms

MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

ON Semiconductor®

TO−247−3LD SHORT LEAD
CASE 340CK
ISSUE A

DATE 31 JAN 2019

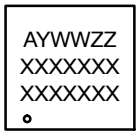


DIM	MILLIMETERS		
	MIN	NOM	MAX
A	4.58	4.70	4.82
A1	2.20	2.40	2.60
A2	1.40	1.50	1.60
b	1.17	1.26	1.35
b2	1.53	1.65	1.77
b4	2.42	2.54	2.66
c	0.51	0.61	0.71
D	20.32	20.57	20.82
D1	13.08	~	~
D2	0.51	0.93	1.35
E	15.37	15.62	15.87
E1	12.81	~	~
E2	4.96	5.08	5.20
e	~	5.56	~
L	15.75	16.00	16.25
L1	3.69	3.81	3.93
ØP	3.51	3.58	3.65
ØP1	6.60	6.80	7.00
Q	5.34	5.46	5.58
S	5.34	5.46	5.58

NOTES: UNLESS OTHERWISE SPECIFIED.

A. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.
B. ALL DIMENSIONS ARE IN MILLIMETERS.
C. DRAWING CONFORMS TO ASME Y14.5 - 2009.
D. DIMENSION A1 TO BE MEASURED IN THE REGION DEFINED BY L1.
E. LEAD FINISH IS UNCONTROLLED IN THE REGION DEFINED BY L1.

GENERIC
MARKING DIAGRAM*



XXXX = Specific Device Code
A = Assembly Location
Y = Year
WW = Work Week
ZZ = Assembly Lot Code

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

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DESCRIPTION:	**TO−247−3LD SHORT LEAD**	**PAGE 1 OF 1**

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