

# MOSFET - Power, Single P-Channel, **POWERTRENCH**<sup>®</sup>

-20 V, -11 A, 13 mΩ



**ON Semiconductor**<sup>®</sup>

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## FDMA008P20LZ

### General Description

This device is designed specifically for battery charge or load switching in cellular handset and other ultraportable applications. It features a MOSFET with low on-state resistance and zener diode protection against ESD.

The WDFN6 (MicroFET 2.05x2.05) package offers exceptional thermal performance for its physical size and is well suited to linear mode applications.

### Features

- Max  $r_{DS(on)}$  = 13 mΩ at  $V_{GS} = -4.5$  V,  $I_D = -2.5$  A
- Max  $r_{DS(on)}$  = 16 mΩ at  $V_{GS} = -2.5$  V,  $I_D = -1.4$  A
- Max  $r_{DS(on)}$  = 20 mΩ at  $V_{GS} = -1.8$  V,  $I_D = -1.0$  A
- Max  $r_{DS(on)}$  = 30 mΩ at  $V_{GS} = -1.5$  V,  $I_D = -0.85$  A
- Low Profile – 0.8 mm Maximum – in the New Package WDFN6 (MicroFET 2.05 × 2.05 mm)
- HBM ESD Protection Level > 1 kV Typical (Note 3)
- Free from Halogenated Compounds and Antimony Oxides
- RoHS Compliant

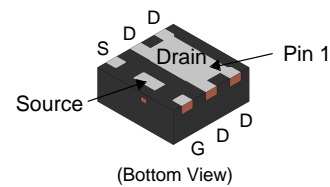
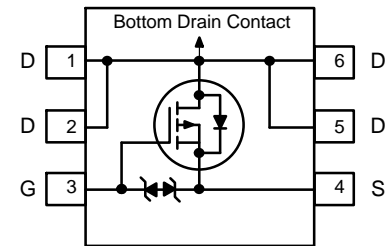
### MOSFET MAXIMUM RATINGS ( $T_A = 25^\circ\text{C}$ unless otherwise noted)

Symbol	Parameter	Ratings	Unit	
$V_{DS}$	Drain to Source Voltage	-20	V	
$V_{GS}$	Gate to Source Voltage	±8	V	
$I_D$	Drain Current	Continuous (Note 1a)	-11	A
		Pulsed (Note 5)	-164	
$E_{AS}$	Single Pulse Avalanche Energy (Note 4)	54	mJ	
$P_D$	Power Dissipation	(Note 1a)	2.4	W
		(Note 1b)	0.9	
$T_J, T_{STG}$	Operating and Storage Junction Temperature Range	-55 to +150	°C	

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

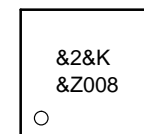
### THERMAL CHARACTERISTICS

Symbol	Parameter	Ratings	Unit	
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	(Note 1a)	52	°C/W
		(Note 1b)	145	



WDFN6 2.05x2.05, 0.65P  
CASE 483AV

### MARKING DIAGRAM



&2 = Date Code  
&K = Lot Code  
&Z = Assembly Plant Code  
008 = Specific Device Code

### ORDERING INFORMATION

Device Marking	Device	Package	Shipping <sup>†</sup>
008	FDMA008P20LZ	WDFN6 (Pb-Free)	3000 Units/Tape & Reel

<sup>†</sup>For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

# FDMA008P20LZ

## ELECTRICAL CHARACTERISTICS (T<sub>C</sub> = 25°C unless otherwise noted)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
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### OFF CHARACTERISTICS

BV <sub>DSS</sub>	Drain to Source Breakdown Voltage	I <sub>D</sub> = -250 μA, V <sub>GS</sub> = 0 V	-20			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	I <sub>D</sub> = -250 μA, referenced to 25°C		-16		mV/°C
I <sub>DSS</sub>	Zero Gate Voltage Drain Current	V <sub>DS</sub> = -16 V, V <sub>GS</sub> = 0 V			-1	μA
I <sub>GSS</sub>	Gate to Source Leakage Current	V <sub>GS</sub> = ±8 V, V <sub>DS</sub> = 0 V			±1	μA

### ON CHARACTERISTICS

V <sub>GS(th)</sub>	Gate to Source Threshold Voltage	V <sub>GS</sub> = V <sub>DS</sub> , I <sub>D</sub> = -250 μA	-0.4	-0.65	-1.4	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate to Source Threshold Voltage Temperature Coefficient	I <sub>D</sub> = -250 μA, referenced to 25°C		3		mV/°C
r <sub>DS(on)</sub>	Static Drain to Source On Resistance	V <sub>GS</sub> = -4.5 V, I <sub>D</sub> = -2.5 A		10	13	mΩ
		V <sub>GS</sub> = -2.5 V, I <sub>D</sub> = -1.4 A		12	16	
		V <sub>GS</sub> = -1.8 V, I <sub>D</sub> = -1.0 A		15	20	
		V <sub>GS</sub> = -1.5 V, I <sub>D</sub> = -0.85 A		20	30	
		V <sub>GS</sub> = -4.5 V, I <sub>D</sub> = -2.5 A, T <sub>J</sub> = 125°C		12.8		
g <sub>FS</sub>	Forward Transconductance	V <sub>DS</sub> = -5 V, I <sub>D</sub> = -2.5 A		26		S

### DYNAMIC CHARACTERISTICS

C <sub>iss</sub>	Input Capacitance	V <sub>DS</sub> = -10 V, V <sub>GS</sub> = 0 V, f = 1 MHz		3131	4383	pF
C <sub>oss</sub>	Output Capacitance			424	594	
C <sub>rss</sub>	Reverse Transfer Capacitance			386	540	
R <sub>g</sub>	Gate Resistance			13	25	

### SWITCHING CHARACTERISTICS

t <sub>d(on)</sub>	Turn-On Delay Time	V <sub>DD</sub> = -10 V, I <sub>D</sub> = -2.5 A, V <sub>GS</sub> = -4.5 V, R <sub>GEN</sub> = 6 Ω		12	21	ns
t <sub>r</sub>	Rise Time			17	30	
t <sub>d(off)</sub>	Turn-Off Delay Time			239	382	
t <sub>f</sub>	Fall Time			96	153	
Q <sub>g</sub>	Total Gate Charge	V <sub>GS</sub> = -4.5 V, V <sub>DD</sub> = -10 V, I <sub>D</sub> = -2.5 A		28	39	nC
Q <sub>gs</sub>	Gate to Source Gate Charge			3.6		
Q <sub>gd</sub>	Gate to Drain "Miller" Charge			6.2		

### DRAIN-SOURCE DIODE CHARACTERISTICS

V <sub>SD</sub>	Source to Drain Diode Forward Voltage	V <sub>GS</sub> = 0 V, I <sub>S</sub> = -2 A (Note 2)		-0.6	-1.2	V
		V <sub>GS</sub> = 0 V, I <sub>S</sub> = -2.5 A (Note 2)		-0.8	-1.3	V
t <sub>rr</sub>	Reverse Recovery Time	I <sub>F</sub> = -6.8 A, di/dt = 100 A/μS		28	46	ns
Q <sub>rr</sub>	Reverse Recovery Charge			10	17	nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

1. R<sub>θJA</sub> is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins.



a. 52 °C/W when mounted on a 1 in<sup>2</sup> pad of 2 oz copper



b. 145 °C/W when mounted on a minimum pad of 2 oz copper

2. Pulse Test: Pulse Width < 300 μs, Duty cycle < 2.0%.
3. The diode connected between the gate and the source serves only as protection against ESD. No gate overvoltage rating is implied.
4. E<sub>AS</sub> of 54 mJ is based on starting T<sub>J</sub> = 25°C, L = 3 mH, I<sub>AS</sub> = 6 A, V<sub>DD</sub> = 20 V, V<sub>GS</sub> = 4.5 V. 100% test at L = 0.1 mH, I<sub>AS</sub> = 19 A.
5. Pulsed I<sub>d</sub> please refer to Figure 10. SOA curve for more details.

TYPICAL CHARACTERISTICS ( $T_J = 25^\circ\text{C}$  unless otherwise noted)

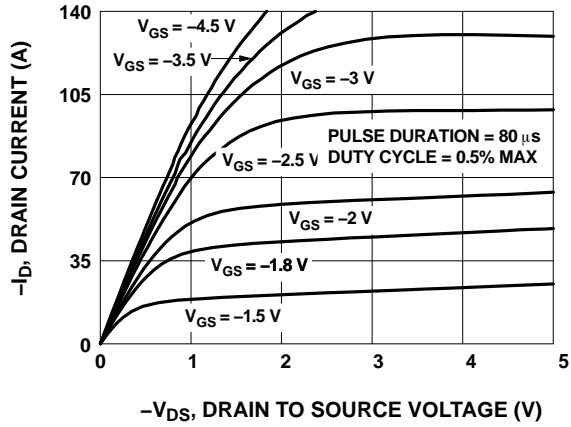


Figure 1. On-Region Characteristics

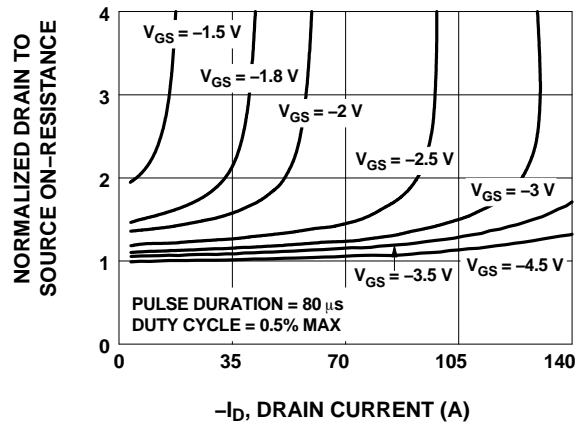


Figure 2. Normalized On-Resistance vs. Drain Current and Gate Voltage

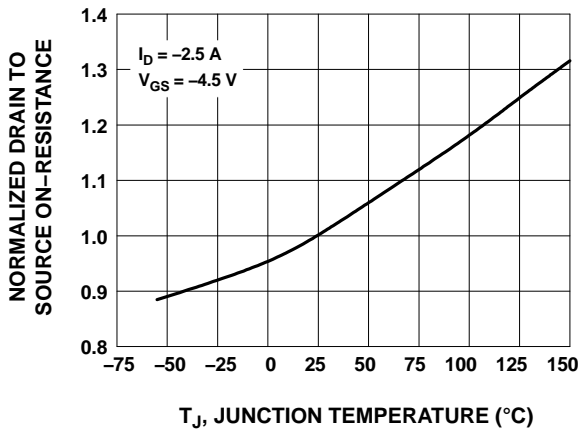


Figure 3. Normalized On-Resistance vs. Junction Temperature

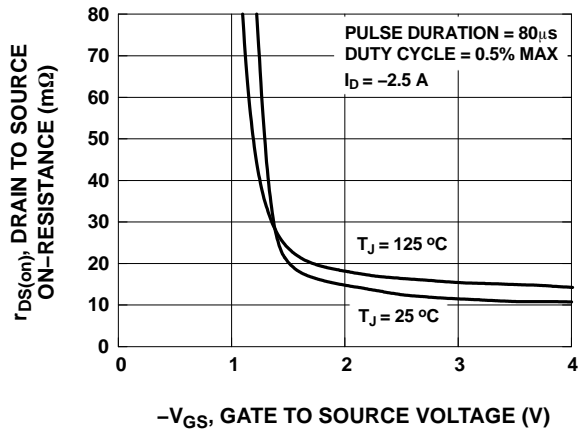


Figure 4. On-Resistance vs. Gate to Source Voltage

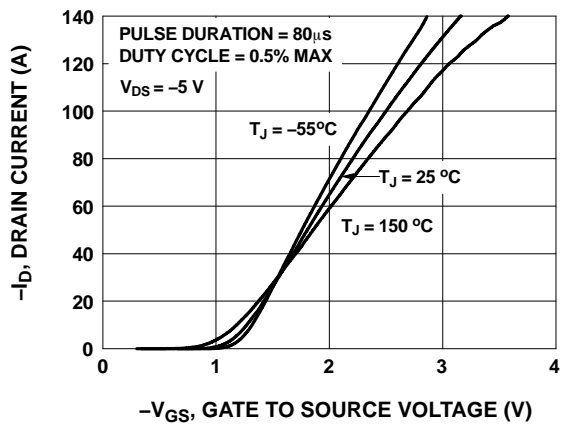


Figure 5. Transfer Characteristics

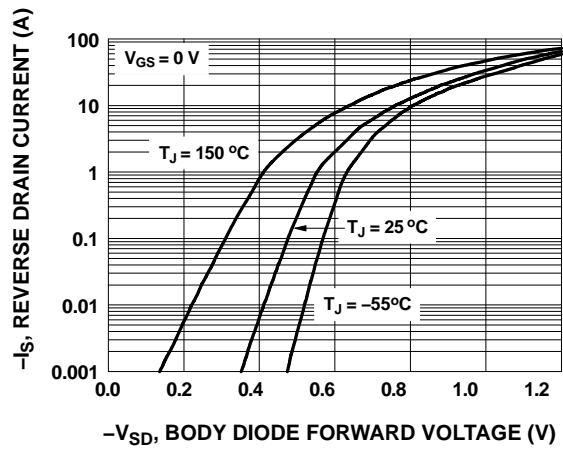


Figure 6. Source to Drain Diode Forward Voltage vs. Source Current

TYPICAL CHARACTERISTICS ( $T_J = 25^\circ\text{C}$  unless otherwise noted) (continued)

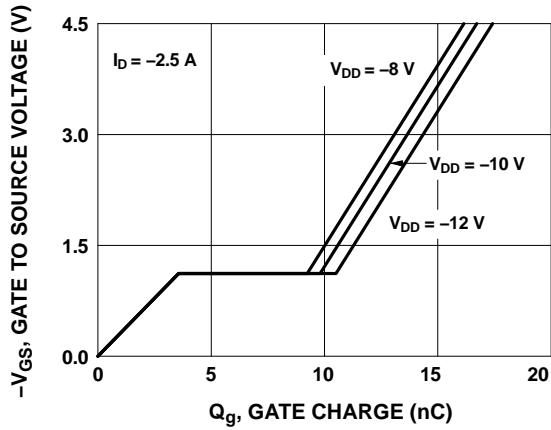


Figure 7. Gate Charge Characteristics

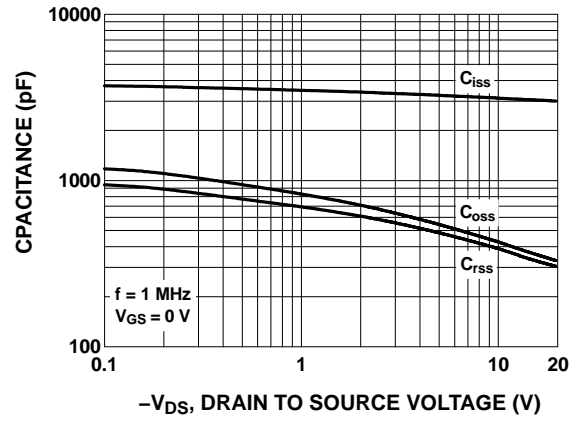


Figure 8. Capacitance vs. Drain to Source Voltage

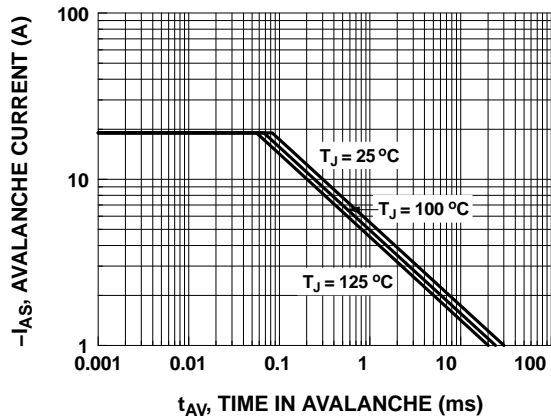


Figure 9. Unclamped Inductive Switching Capability

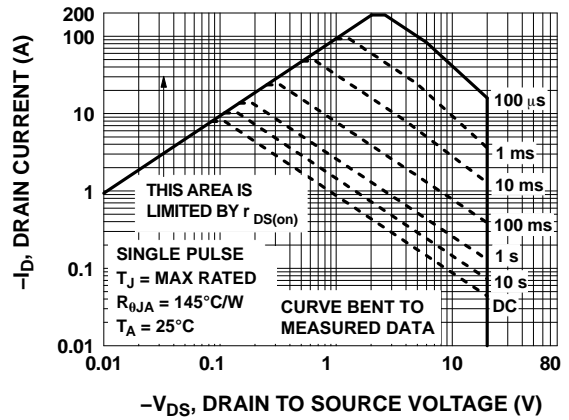


Figure 10. Forward Bias Safe Operating Area

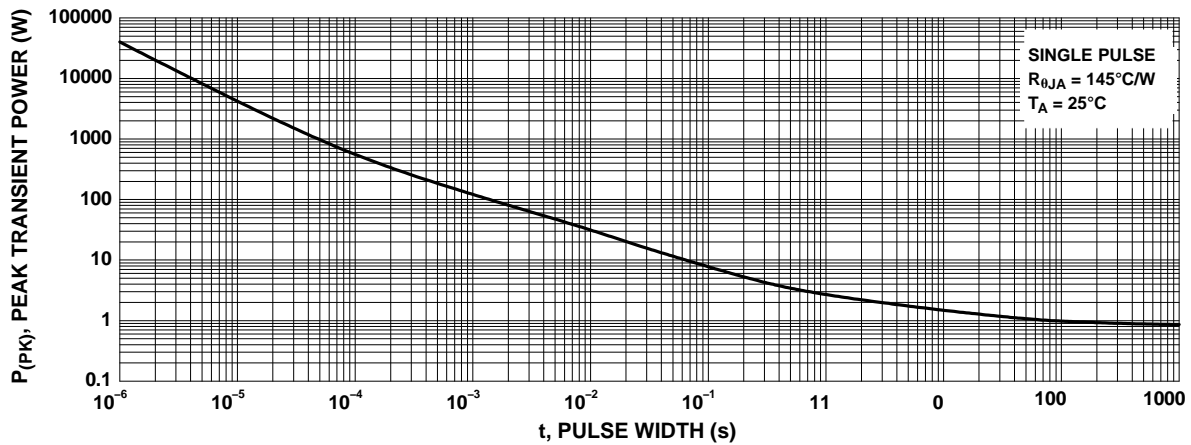
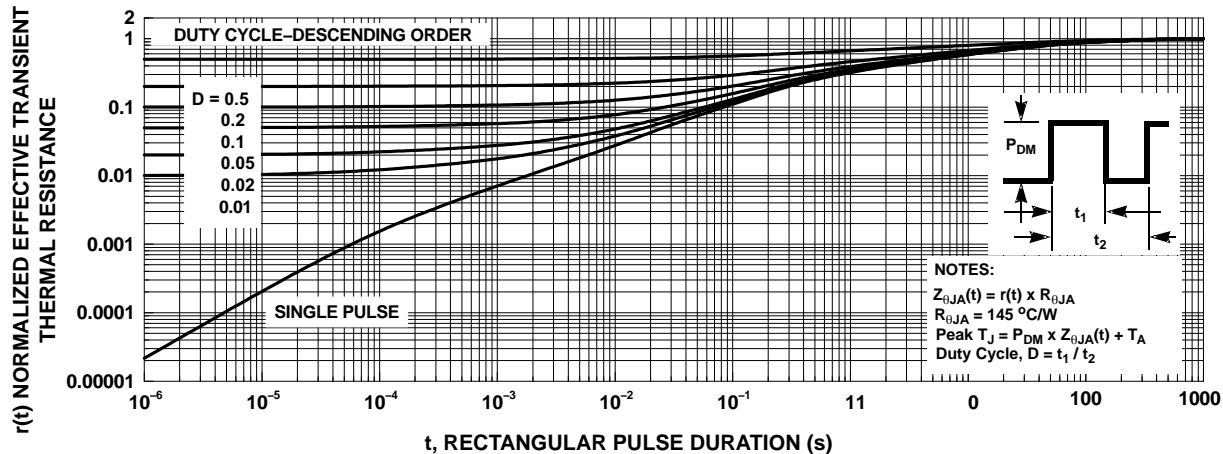


Figure 11. Single Pulse Maximum Power Dissipation

TYPICAL CHARACTERISTICS ( $T_J = 25^\circ\text{C}$  unless otherwise noted) (continued)

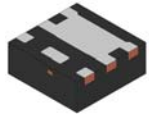


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# MECHANICAL CASE OUTLINE

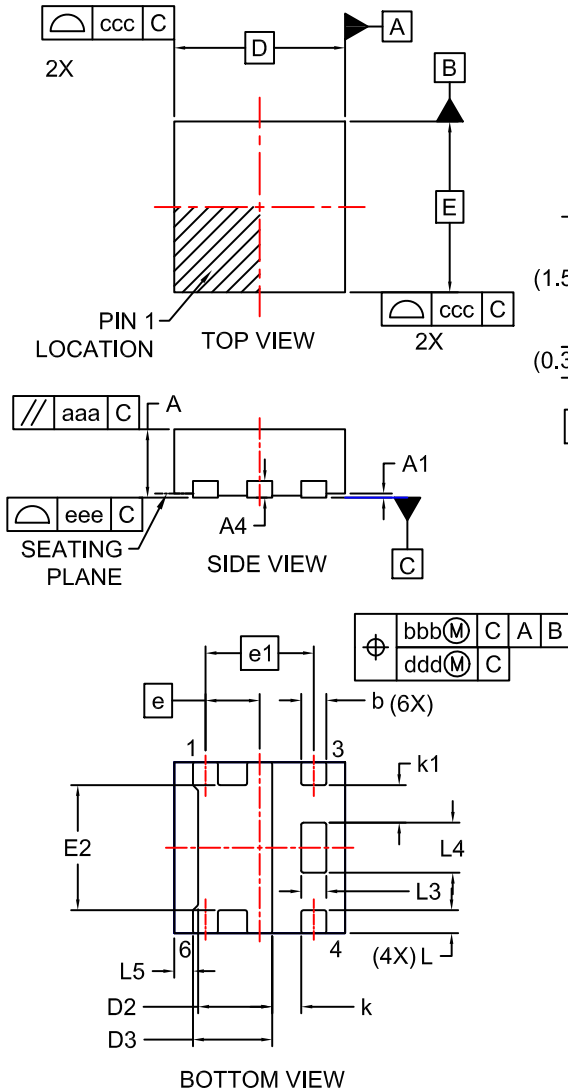
## PACKAGE DIMENSIONS

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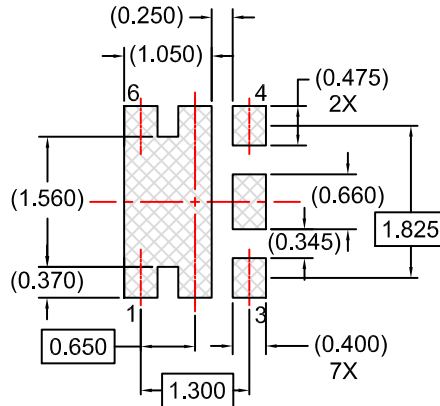


**WDFN6 2.05X2.05, 0.65P**  
CASE 483AV  
ISSUE A

DATE 02 APR 2019



### LAND PATTERN RECOMMENDATION



### NOTES:

1. CONTROLLING DIMENSION: MILLIMETERS.
2. COPLANARITY APPLIES TO THE EXPOSED PADS AS WELL AS THE TERMINALS.
3. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
4. SEATING PLANE IS DEFINED BY THE TERMINALS. "A1" IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT ON THE PACKAGE BODY.

DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	0.60	0.70	0.80
A1	0.00	-	0.05
A4	(0.20)		
b	0.25	0.30	0.35
D	1.95	2.05	2.15
D2	0.84	0.89	0.94
D3	(0.95)		
E	1.95	2.05	2.15
E2	1.45	1.50	1.55
e	0.65 BSC		
e1	1.30 BSC		
k	(0.35)		
k1	(0.45)		
L	0.18	0.28	0.38
L3	0.25	0.30	0.35
L4	0.55	0.60	0.65
L5	(0.23)		
aaa	0.10		
bbb	0.10		
ccc	0.05		
ddd	0.05		
eee	0.05		

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