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# FDMA1430JP

### July 2014

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# Integrated P-Channel PowerTrench® MOSFET and BJT -30 V, -2.9 A, 90 m $\Omega$

#### **Features**

- Max  $r_{DS(on)}$  = 90 m $\Omega$  at  $V_{GS}$  = -4.5 V,  $I_D$  = -2.9 A
- Max  $r_{DS(on)}$  = 130 m $\Omega$  at  $V_{GS}$  = -2.5 V,  $I_D$  = -2.6 A
- Max  $r_{DS(on)} = 170 \text{ m}\Omega$  at  $V_{GS} = -1.8 \text{ V}$ ,  $I_D = -1.7 \text{ A}$
- Max  $r_{DS(on)} = 240 \text{ m}\Omega$  at  $V_{GS} = -1.5 \text{ V}$ ,  $I_D = -1 \text{ A}$
- Low profile 0.8 mm maximum in the new package MicroFET 2x2
- HBM ESD protection level > 2 kV typical (Note 3)
- RoHS Compliant

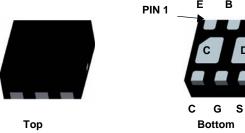
## **General Description**

This device is designed specifically as a single package solution for loadswitching in cellular handset and other ultra-portable applications. It features a 50 V NPN BJT and a 30 V P-ch Trench MOSFET in the space saving MicroFET 2x2 package that offers exceptional thermal performance for it's physical size and is well suited to linear mode applications.

### **Application**

■ Loadswitching

D



MicroFET 2x2



## **Maximum Ratings** $T_A = 25$ °C unless otherwise noted

Symbol	Par	ameter		Ratings	Units
V <sub>DS</sub>	Drain to Source Voltage			-30	V
V <sub>GS</sub>	Gate to Source Voltage			±8	V
1	Drain Current -Continuous	T <sub>A</sub> = 25°C	(Note 1a)	-2.9	Δ.
ID	-Pulsed			-12	A
V <sub>CBO</sub>	Collector-Base Voltage		(Note 4)	50	V
V <sub>CEO</sub>	Collector-Emitter Voltage		(Note 5)	50	V
V <sub>EBO</sub>	Emitter-Base Voltage			10	V
I <sub>C</sub>	Collector Current			100	mA
P <sub>C</sub>	Collector Power Dissipation			200	mW
TJ	Junction Temperature			150	°C
D	Power Dissipation	T <sub>A</sub> = 25°C	(Note 1a)	1.5	W
$P_{D}$		T <sub>A</sub> = 25°C	(Note 1b)	0.7	VV
T <sub>J</sub> , T <sub>STG</sub>	Operating and Storage Junction Temp	perature Range		-55 to +150	°C

#### **Thermal Characteristics**

$R_{\theta JA}$	Thermal Resistance, Junction to Ambient(MOSFET)	(Note 1a)	86	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient(MOSFET)	(Note 1b)	173	C/VV

#### **Package Marking and Ordering Information**

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
143	FDMA1430JP	MicroFET 2x2	7"	8 mm	5000 units

# **Electrical Characteristics** $T_J = 25$ °C unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Тур	Max	Units
Off Chara	ncteristics					
BV <sub>DSS</sub>	Drain to Source Breakdown Voltage	$I_D = -250 \mu A, V_{GS} = 0 V$	-30			V
$\frac{\Delta BV_{DSS}}{\Delta T_{J}}$	Breakdown Voltage Temperature Coefficient	$I_D$ = -250 $\mu$ A, referenced to 25 °C		-23		mV/°C
I <sub>DSS</sub>	Zero Gate Voltage Drain Current	V <sub>DS</sub> = -24 V, V <sub>GS</sub> = 0 V			-1	μΑ
I <sub>GSS</sub>	Gate to Source Leakage Current	$V_{GS} = \pm 8 \text{ V}, V_{DS} = 0 \text{ V}$			±1	μΑ

#### **On Characteristics**

$V_{GS(th)}$	Gate to Source Threshold Voltage	$V_{GS} = V_{DS}, I_D = -250 \mu A$	-0.4	-0.6	-1	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate to Source Threshold Voltage Temperature Coefficient	$I_D$ = -250 $\mu$ A, referenced to 25 °C		2.4		mV/°C
		$V_{GS} = -4.5 \text{ V}, I_D = -2.9 \text{ A}$		67	90	
		$V_{GS} = -2.5 \text{ V},  I_D = -2.6 \text{ A}$		81	130	
rno( )	Static Drain to Source On Resistance	$V_{GS} = -1.8 \text{ V}, I_D = -1.7 \text{ A}$		98	170	mΩ
r <sub>DS(on)</sub>	Static Drain to Source On Resistance	$V_{GS} = -1.5 \text{ V}, I_D = -1 \text{ A}$		114	240	11122
		$V_{GS} = -4.5 \text{ V},  I_{D} = -2.9 \text{ A},$ $T_{J} = 125 \text{ °C}$		102	133	
g <sub>FS</sub>	Forward Transconductance	$V_{DS} = -5 \text{ V}, I_{D} = -2.9 \text{ A}$		11		S

## **Dynamic Characteristics**

C <sub>iss</sub>	Input Capacitance	V 45 V V 0 V	438	580	pF
Coss	Output Capacitance	$V_{DS} = -15 \text{ V}, V_{GS} = 0 \text{ V},$ f = 1  MHz	47	70	pF
C <sub>rss</sub>	Reverse Transfer Capacitance	1 - 1 1/11/12	41	60	pF

## **Switching Characteristics**

t <sub>d(on)</sub>	Turn-On Delay Time		4.8	10	ns
t <sub>r</sub>	Rise Time	$V_{DD}$ = -15 V, $I_{D}$ = -1 A, $V_{GS}$ = -4.5 V, $R_{GEN}$ = 6 Ω	4.4	10	ns
t <sub>d(off)</sub>	Turn-Off Delay Time	V <sub>GS</sub> = -4.5 V, K <sub>GEN</sub> = 612	67	107	ns
t <sub>f</sub>	Fall Time		21	33	ns
$Q_g$	Total Gate Charge	V 45.V.L 20.A	7.2	10	nC
Q <sub>gs</sub>	Gate to Source Charge	$V_{DD} = -15 \text{ V}, I_{D} = -2.9 \text{ A},$ $V_{GS} = -4.5 \text{ V}$	0.7		nC
$Q_{gd}$	Gate to Drain "Miller" Charge	VGS = 4.3 V	1.6		nC

## **Drain-Source Diode Characteristics**

$V_{SD}$	Source to Drain Diode Forward Voltage	$V_{GS} = 0 \text{ V}, I_{S} = -1.1 \text{ A}$ (Note 2)	-0.7	-1.2	V
t <sub>rr</sub>	Reverse Recovery Time	I <sub>E</sub> = -2.9 A, di/dt = 100 A/μs	16	29	ns
Q <sub>rr</sub>	Reverse Recovery Charge	- 1 <sub>F</sub> = -2.9 A, αι/αι = 100 A/μs	5	10	nC

#### **BJT Characteristics**

$I_{CBO}$	Collector Cut-off Current	$V_{CB} = 40 \text{ V}, I_{E} = 0 \text{ A}$			0.1	μΑ
$h_{FE}$	DC Current Gain	$V_{CE} = 5 \text{ V}, I_{C} = 5 \text{ mA}$	68			
V <sub>CE</sub> (sat)	Collector-Emitter Saturation Voltage	$I_C = 10 \text{ mA}, I_B = 0.5 \text{ mA}$			0.3	V
f <sub>T</sub>	Current Gain Bandwidth Product	$V_{CE} = 10 \text{ V}, I_{C} = 5 \text{ mA}$		250		MHz
C <sub>ob</sub>	Output Capacitance	$V_{CB} = 10 \text{ V}, I_{E} = 0 \text{ A}, f = 1 \text{ MHz}$		3.7		pF
V <sub>I</sub> (off)	Input Off Voltage	$V_{CE} = 5 \text{ V}, I_{C} = 100 \mu\text{A}$	0.5			V
V <sub>I</sub> (on)	Input On Voltage	$V_{CE} = 0.2 \text{ V}, I_{C} = 5 \text{ mA}$			1.3	V
R1	Input Resistor			4.7		kΩ
R1/R2	Resistor Ratio			0.1		

## **Electrical Characteristics**

#### Notes:

1.  $R_{\theta JA}$  is determined with the device mounted on a 1 in<sup>2</sup> oz. copper pad on a 1.5 x 1.5 in. board of FR-4 material.  $R_{\theta JC}$  is guaranteed by design while  $R_{\theta JA}$  is determined by the user's board design.



a. 86 °C/W when mounted on a 1 in<sup>2</sup> pad of 2 oz copper



b. 173 °C/W when mounted on a minimum pad of 2 oz copper

- 2. Pulse Test : Pulse Width < 300 us, Duty Cycle < 2.0%
- 3. The diode connected between the gate and source serves only as protection against ESD. No gate overvoltage rating is implied.
- 4. Guaranteed by Icbo
- 5. Guaranteed by Iceo

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### Typical Characteristics T<sub>J</sub> = 25 °C unless otherwise noted

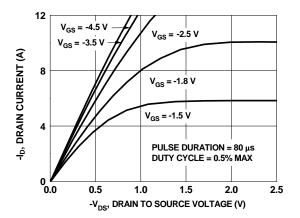


Figure 1. On-Region Characteristics

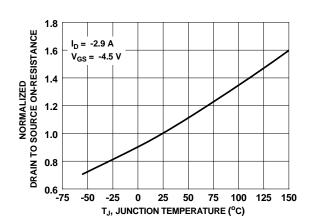


Figure 3. Normalized On-Resistance vs Junction Temperature

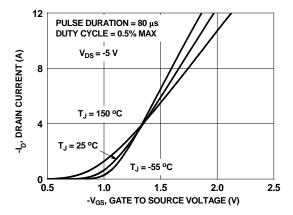


Figure 5. Transfer Characteristics

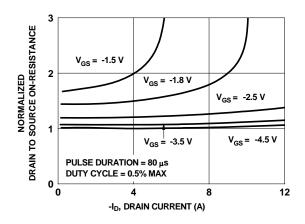


Figure 2. Normalized On-Resistance vs Drain Current and Gate Voltage

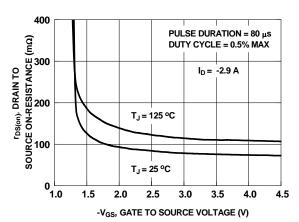


Figure 4. On-Resistance vs Gate to Source Voltage

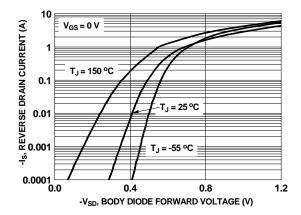


Figure 6. Source to Drain Diode Forward Voltage vs Source Current

## Typical Characteristics T<sub>J</sub> = 25 °C unless otherwise noted

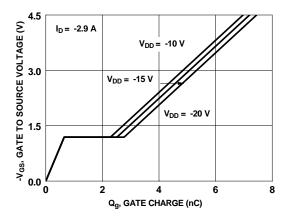


Figure 7. Gate Charge Characteristics

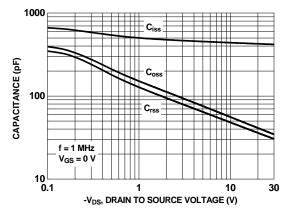


Figure 8. Capacitance vs Drain to Source Voltage

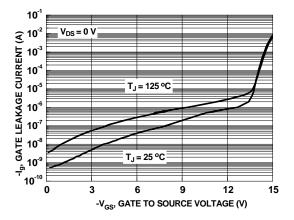


Figure 9. Gate Leakage vs Gate to Source Voltage

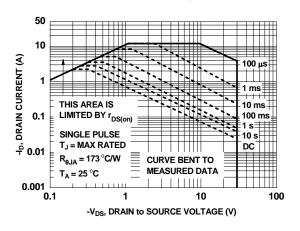


Figure 10. Forward Bias Safe Operating Area

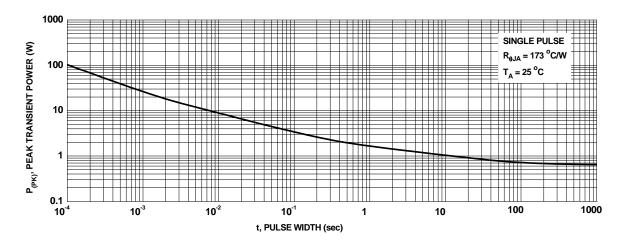


Figure 11. Single Pulse Maximum Power Dissipation



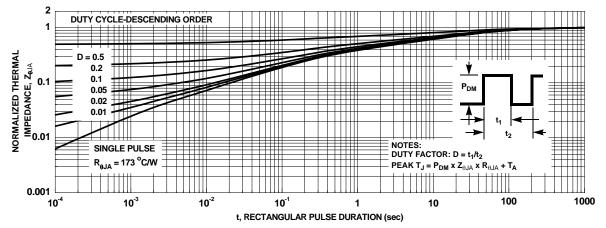
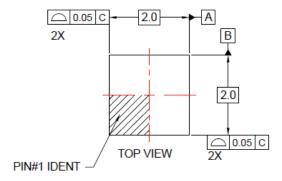
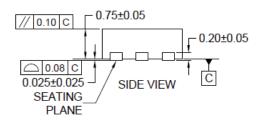
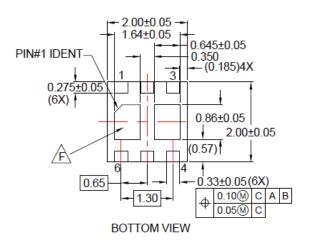


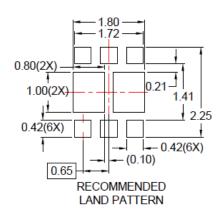
Figure 12. Junction-to-Ambient Transient Thermal Response Curve

## **Dimensional Outline and Pad Layout**









#### NOTES:

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