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May 2010

FDMA507PZ

Single P-Channel PowerTrench® MOSFET

-20 V, -7.8 A, 24 mΩ

Features

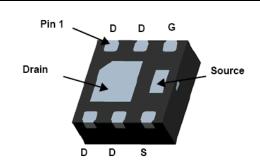
- Max $r_{DS(on)} = 24 \text{ m}\Omega$ at $V_{GS} = -5 \text{ V}$, $I_D = -7.8 \text{ A}$
- Max $r_{DS(on)}$ = 25 m Ω at V_{GS} = -4.5 V, I_D = -7 A
- Max $r_{DS(on)}$ = 35 m Ω at V_{GS} = -2.5 V, I_D = -5.5 A
- Max $r_{DS(on)}$ = 45 m Ω at V_{GS} = -1.8 V, I_D = -4 A
- Low Profile 0.8 mm maximum in the package MicroFET 2X2 mm
- HBM ESD protection level > 3.2K V typical (Note3)
- Free from halogenated compounds and antimony oxides
- RoHS Compliant

General Description

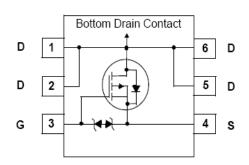
This device is designed specifically for battery charge or load switching in cellular handset and other ultraportable applications. It features a MOSFET with low on-stade resistance.

The MicroFET 2X2 package offers exceptional thermal perforance for its physical size and is well suited to linear mode applications.





MicroFET 2X2 (Bottom View)



MOSFET Maximum Ratings T_A = 25 °C unless otherwise noted

Symbol	Para	Ratings	Units		
V _{DS}	Drain to Source Voltage			-20	V
V _{GS}	Gate to Source Voltage			±8	V
I _D	Drain Current -Continuous	T _A = 25 °C	(Note 1a)	-7.8	٨
	-Pulsed			-24	Α
Б	Power Dissipation	T _A = 25 °C	(Note 1a)	2.4	10/
P_{D}	Power Dissipation $T_A = 25 ^{\circ}\text{C}$ (Note 1b)		(Note 1b)	0.9	W
T _J , T _{STG}	Operating and Storage Junction Temp	perature Range		-55 to +150	°C

Thermal Characteristics

R_{\thetaJA}	Thermal Resistance, Junction to Ambient	(Note 1a)	52	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	(Note 1b)	145	5

Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
507	FDMA507PZ	MicroFET 2X2	7 "	12 mm	3000 units

Electrical Characteristics T_J = 25 °C unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Тур	Max	Units
Off Chara	acteristics					
BV_{DSS}	Drain to Source Breakdown Voltage	$I_D = -250 \mu\text{A}, V_{GS} = 0 \text{V}$	-20			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	I_D = -250 μ A, referenced to 25 °C		-12		mV/°C
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} = -16 V, V _{GS} = 0 V			-1	μΑ
I _{GSS}	Gate to Source Leakage Current	$V_{GS} = \pm 8 \text{ V}, V_{DS} = 0 \text{ V}$			±10	μА

On Characteristics

$V_{GS(th)}$	Gate to Source Threshold Voltage	$V_{GS} = V_{DS}, I_{D} = -250 \mu A$	-0.4	-0.5	-1.5	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate to Source Threshold Voltage Temperature Coefficient	I_D = -250 μ A, referenced to 25 °C		3		mV/°C
	$V_{GS} = -5 \text{ V}, I_D = -7.8 \text{ A}$		19	24		
		$V_{GS} = -4.5 \text{ V}, I_D = -7 \text{ A}$		20	25	
r _{DS(on)}	Drain to Source On Resistance	$V_{GS} = -2.5 \text{ V}, I_D = -5.5 \text{ A}$		24	35	mΩ
		$V_{GS} = -1.8 \text{ V}, I_D = -4 \text{ A}$		29	45	
		$V_{GS} = -5 \text{ V}, I_D = -7.8 \text{ A}, T_J = 125 \text{ °C}$		26	34	
9 _{FS}	Forward Transconductance	$V_{DS} = -5 \text{ V}, I_{D} = -7.8 \text{ A}$		33		S

Dynamic Characteristics

C _{iss}	Input Capacitance	V 40.V V 0.V	1515	2015	pF
C _{oss}	Output Capacitance	$V_{DS} = -10 \text{ V}, V_{GS} = 0 \text{ V},$ f = 1 MHz	265	355	pF
C _{rss}	Reverse Transfer Capacitance	1 - 1 1011 12	240	360	pF

Switching Characteristics

t _{d(on)}	Turn-On Delay Time	.,	6.4	13	ns
t _r	Rise Time	V_{DD} = -10 V, I_{D} = -7.8 A V_{GS} = -5 V, R_{GEN} = 6 Ω	14	25	ns
t _{d(off)}	Turn-Off Delay Time	V _{GS} = -5 V, K _{GEN} = 0 12	192	307	ns
t _f	Fall Time		96	154	ns
$Q_{g(TOT)}$	Total Gate Charge	V 40.V I 70.A	30	42	nC
Q _{gs}	Gate to Source Gate Charge	$V_{DD} = -10 \text{ V}, I_D = -7.8 \text{ A}$ $V_{GS} = -5 \text{ V}$	2		nC
Q_{gd}	Gate to Drain "Miller" Charge	v GS = 30 v	7.5		nC

Drain-Source Diode Characteristics

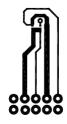
V_{SD}	Source to Drain Diode Forward Voltage	$V_{GS} = 0 \text{ V}, I_{S} = -2.0 \text{ A}$ (Note 2)		-0.6	-1.2	V
t _{rr}	Reverse Recovery Time	-I _E = -7.8 A. di/dt = 100 A/μs		66	106	ns
Q_{rr}	Reverse Recovery Charge	I _F = -7.8 A, di/dt = 100 A/μs		44	70	nC

Notes

^{1.} R_{0JA} is determined with the device mounted on a 1 in² pad 2 oz copper pad on a 1.5 x 1.5 in. board of FR-4 material. R_{0JC} is guaranteed by design while R_{0CA} is determined by the user's board design.



 a. 52 °C/W when mounted on a 1 in² pad of 2 oz copper.



 b. 145 °C/W when mounted on a minimum pad of 2 oz copper.

^{2.} Pulse Test: Pulse Width < $300\mu\text{s},$ Duty cycle < 2.0%.

^{3.} The diode connected between the gate and source serves only as protection against ESD. No gate overvoltage rating is implied.

Typical Characteristics T_J = 25 °C unless otherwise noted

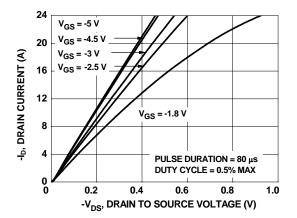


Figure 1. On Region Characteristics

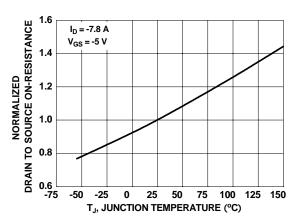


Figure 3. Normalized On Resistance vs Junction Temperature

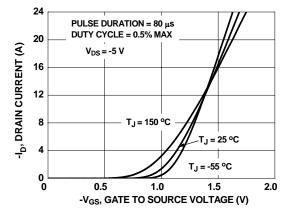


Figure 5. Transfer Characteristics

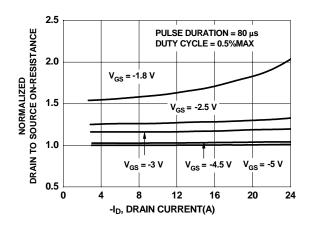


Figure 2. Normalized On-Resistance vs Drain Current and Gate Voltage

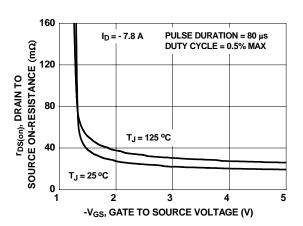


Figure 4. On-Resistance vs Gate to Source Voltage

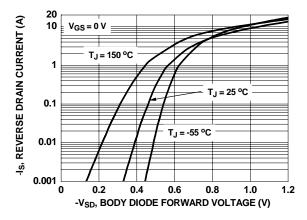


Figure 6. Source to Drain Diode Forward Voltage vs Source Current

Typical Characteristics T_J = 25 °C unless otherwise noted

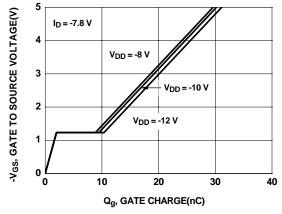


Figure 7. Gate Charge Characteristics

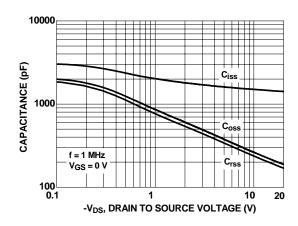


Figure 8. Capacitance vs Drain to Source Voltage

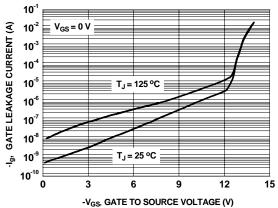


Figure 9. Gate Leakage Current vs Gate to Source Voltage

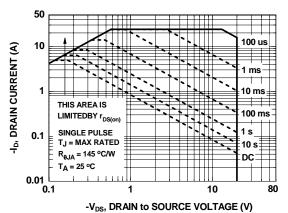


Figure 10. Forward Bias Safe
Operating Area

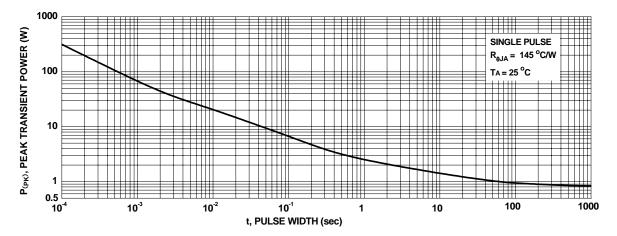


Figure 11. Single Pulse Maximum Power Dissipation

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Typical Characteristics T_J = 25 °C unless otherwise noted

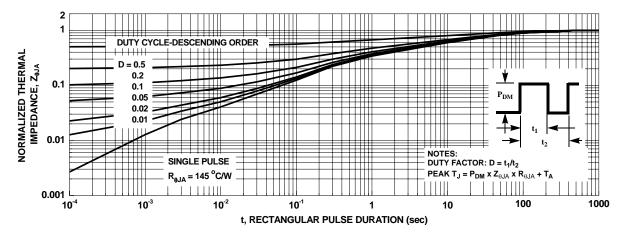
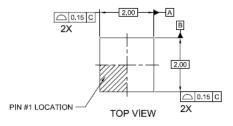
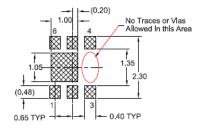


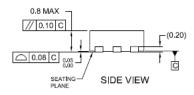
Figure 12. Junction-to-Ambient Transient Thermal Response Curve

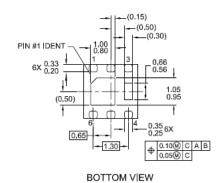
Dimensional Outline and Pad Layout

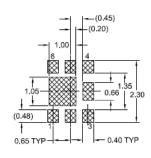




RECOMMENDED LAND PATTERN OPT 1







RECOMMENDED LAND PATTERN OPT 2

NOTES:

- A, DOES NOT FULLY CONFORM TO JEDEC REGISTRATION MO-229 DATED AUG/2003
 B. DIMENSIONS ARE IN MILLIMETERS.
- C. DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994





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