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Please note: As part of the Fairchild Semiconductor integration, some of the Fairchild orderable part numbers will need to change in order to meet ON Semiconductor's system requirements. Since the ON Semiconductor product management systems do not have the ability to manage part nomenclature that utilizes an underscore (_), the underscore (_) in the Fairchild part numbers will be changed to a dash (-). This document may contain device numbers with an underscore (_). Please check the ON Semiconductor website to verify the updated device numbers. The most current and up-to-date ordering information can be found at www.onsemi.com. Please email any questions regarding the system integration to Fairchild_questions@onsemi.com.

April 2015

FDMC2523P
P-Channel QFET®
-150V, -3A, 1.5Ω

Features

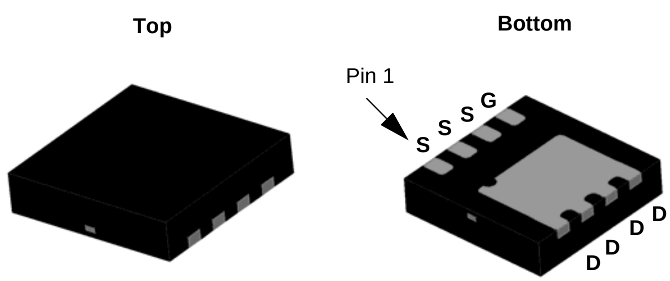
- Max $r_{DS(on)}$ = 1.5Ω at V_{GS} = -10V, I_D = -1.5A
- Low Crss (typical 10pF)
- Fast Switching
- Low gate charge (typical 6.2 nC)
- Improved dv / dt capability
- RoHS Compliant

General Description

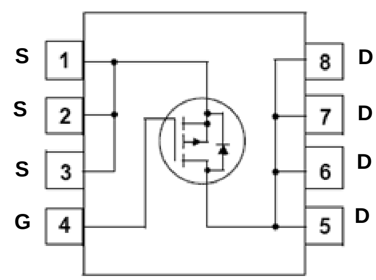
These P-Channel MOSFET enhancement mode power field effect transistors are produced using Fairchild's proprietary, planar stripe, DMOS technology. This advanced technology has been especially tailored to minimize on-state resistance, provide superior switching performance, and withstand high energy pulse in the avalanche and commutation mode. These devices are well suited for low voltage applications such as audio amplifier, high efficiency switching DC/DC converters, and DC motor control.

Application

- Active Clamp Switch



MLP 3.3x3.3



MOSFET Maximum Ratings T_A = 25°C unless otherwise noted

Symbol	Parameter	Ratings	Units
V_{DS}	Drain to Source Voltage	-150	V
V_{GS}	Gate to Source Voltage	±30	V
I_D	Drain Current -Continuous T_C = 25°C	-3	A
	-Continuous T_C = 100°C	-1.8	
	-Pulsed	-12	
P_D	Power Dissipation (Steady State) T_C = 25°C	42	W
E_{AS}	Single Pulse Avalanche Energy (Note 5)	3.3	mJ
T_J, T_{STG}	Operating and Storage Junction Temperature Range	-55 to +150	°C
T_L	Maximum lead temperature for soldering purposes, 1/8" from case for 5 seconds	300	°C
dv/dt	Peak Diode Recovery dv/dt (Note 2)	-5	V/ns

Thermal Characteristics

$R_{\theta JC}$	Thermal Resistance, Junction to Case (Note 1)	3.0	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1a)	60	

Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
2523P	FDMC2523P	MLP 3.3x3.3	13 "	12 mm	3000 units

Electrical Characteristics T_J = 25°C unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units

Off Characteristics

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
BV_{DSS}	Drain to Source Breakdown Voltage	I_D = -250µA, V_{GS} = 0V	-150			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	I_D = -250µA, referenced to 25°C		-138		mV/°C
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = -150V, V_{GS} = 0V			-1	µA
		T_J = 125°C			-10	
I_{GSS}	Gate to Source Leakage Current	V_{GS} = ±30V, V_{DS} = 0V			±100	nA

On Characteristics

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
$V_{GS(th)}$	Gate to Source Threshold Voltage	V_{GS} = V_{DS}, I_D = -250µA	-3	-3.8	-5	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate to Source Threshold Voltage Temperature Coefficient	I_D = -250µA, referenced to 25°C		6		mV/°C
$r_{DS(on)}$	Static Drain to Source On Resistance	V_{GS} = -10V, I_D = -1.5A		1.1	1.5	Ω
		V_{GS} = -10V, I_D = -1.5A , T_J = 125°C		2.0	3.6	
g_{FS}	Forward Transconductance	V_{DS} = -40V, I_D = -1.5A (Note 4)		1.4		S

Dynamic Characteristics

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
C_{iss}	Input Capacitance	V_{DS} = -25V, V_{GS} = 0V, f = 1MHz		200	270	pF
C_{oss}	Output Capacitance			60	80	pF
C_{rss}	Reverse Transfer Capacitance			10	15	pF
R_g	Gate Resistance	f = 1MHz	0.1	7.5	15	Ω

Switching Characteristics

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
$t_{d(on)}$	Turn-On Delay Time	V_{DD} = -75V, I_D = -3A V_{GS} = -10V, R_{GEN} = 25Ω (Note 3,4)		15	27	ns
t_r	Rise Time			11	20	ns
$t_{d(off)}$	Turn-Off Delay Time			19	35	ns
t_f	Fall Time			13	24	ns
Q_g	Total Gate Charge	V_{GS} = -10V V_{DD} = -75V I_D = -3A (Note 3,4)		6.2	9	nC
Q_{gs}	Gate to Source Gate Charge			1.4		nC
Q_{gd}	Gate to Drain "Miller" Charge			3.3		nC

Drain-Source Diode Characteristics

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
I_S	Maximum continuous Drain - Source Diode Forward Current				-3	A
I_{SM}	Maximum Pulse Drain - Source Doide Forward Current				-12	A
V_{SD}	Source to Drain Diode Forward Voltage	V_{GS} = 0V, I_S = -3.0A		-1.8	-5	V
t_{rr}	Reverse Recovery Time	I_F = -3.0A, di/dt = 100A/µs (Note 3)		93		ns
Q_{rr}	Reverse Recovery Charge			0.27		µC

Notes:

1: $R_{\theta JA}$ is the sum of the junction-to-case and case-to- ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.

a. 60°C/W when mounted on a 1 in^2 pad of 2 oz copper

b.135°C/W when mounted on a minimum pad of 2 oz copper

2: $I_{SD} \leq$ -3A, dI/dt $\leq$ 300A/us, $V_{DD} \leq B_{VDSS}$, Starting T_J = 25°C
3: Pulse Test: Pulse Width < 300µs, Duty cycle < 2.0%.
4: Essentially independent of operating temperature.
5: E_{AS} of 3.3 mJ is based on starting T_J = 25 °C; P-ch: L = 3 mH, I_{AS} = -1.5 A, V_{DD} = -150 V, V_{GS} = -10 V.

Typical Characteristics T_J = 25°C unless otherwise noted

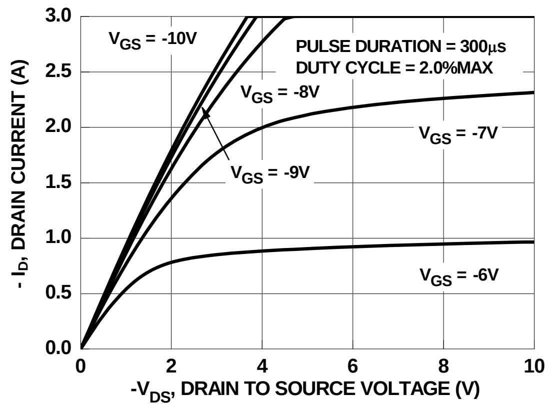


Figure 1. On-Region Characteristics

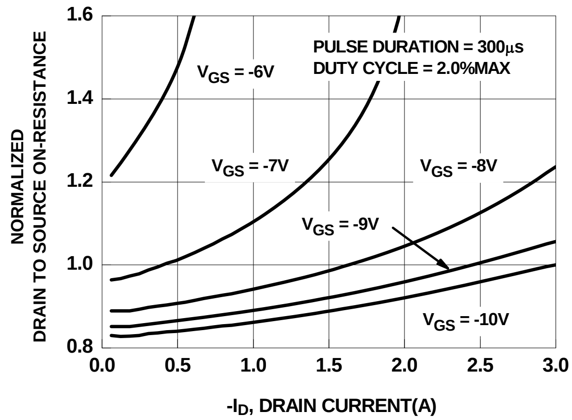


Figure 2. Normalized On-Resistance vs Drain Current and Gate Voltage

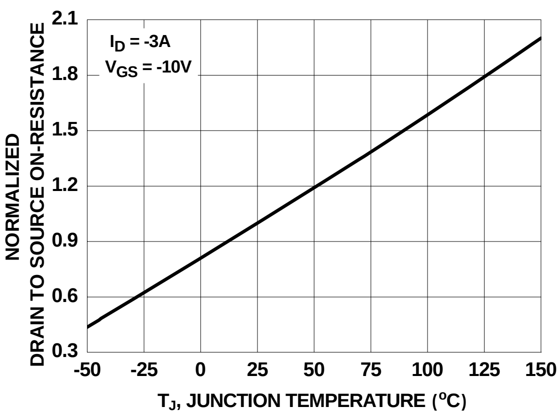


Figure 3. Normalized On-Resistance vs Junction Temperature

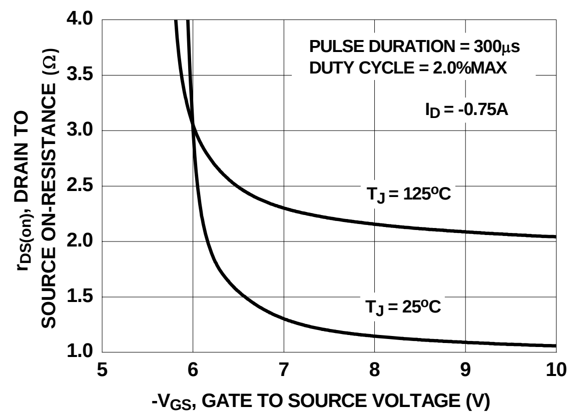


Figure 4. On-Resistance vs Gate to Source Voltage

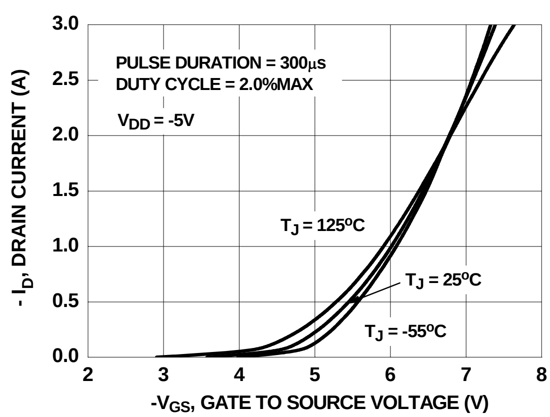


Figure 5. Transfer Characteristics

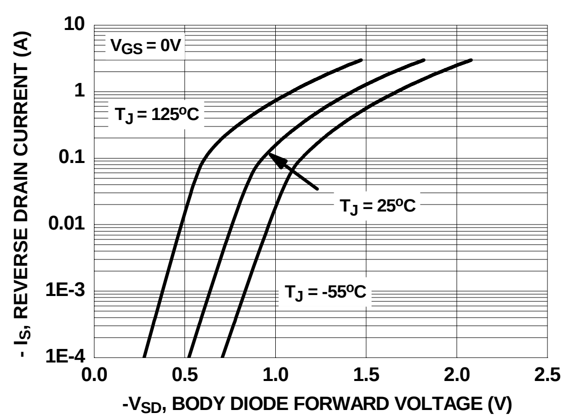


Figure 6. Source to Drain Diode Forward Voltage vs Source Current

Typical Characteristics T_J = 25°C unless otherwise noted

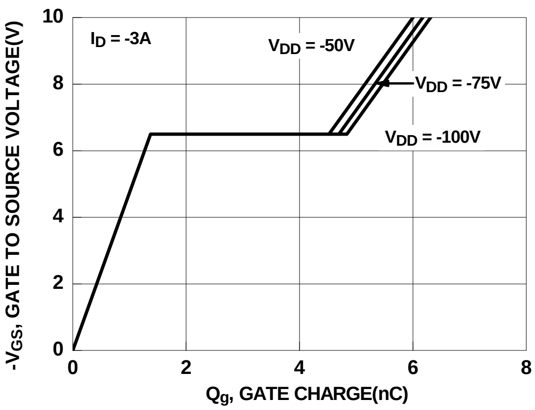


Figure 7. Gate Charge Characteristics

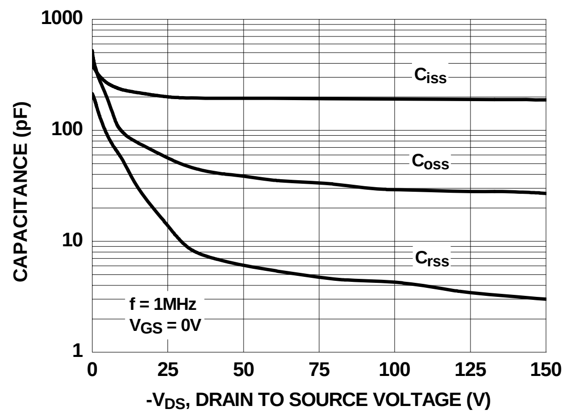


Figure 8. Capacitance vs Drain to Source Voltage

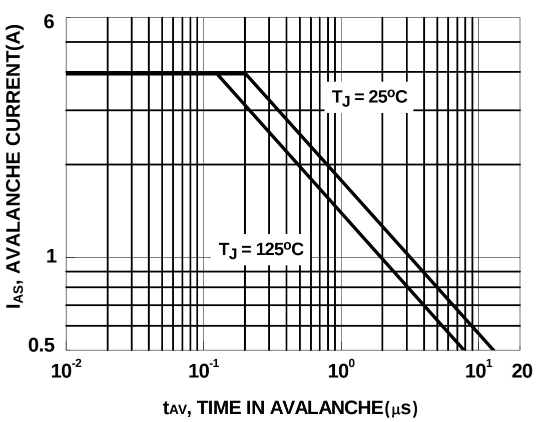


Figure 9. Unclamped Inductive Switching Capability

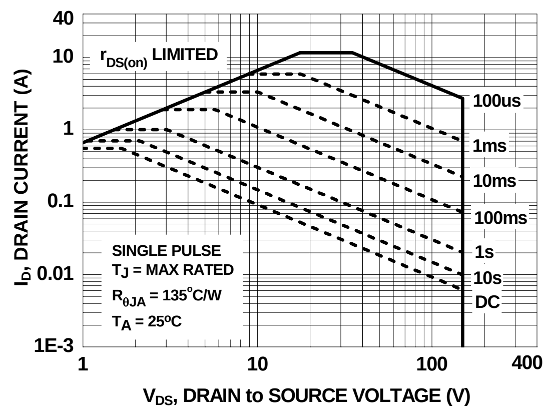


Figure 10. Forward Bias Safe Operating Area

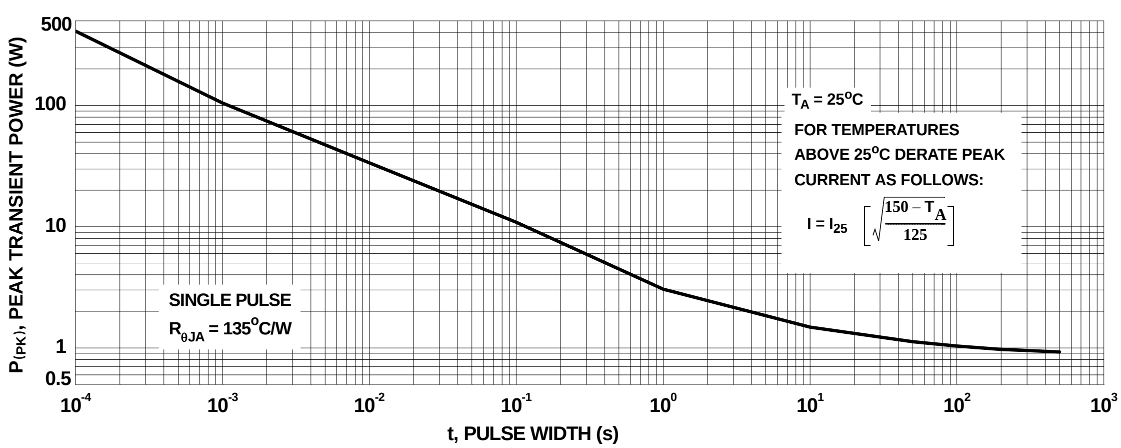


Figure 11. Single Pulse Maximum Power Dissipation

Typical Characteristics T_J = 25°C unless otherwise noted

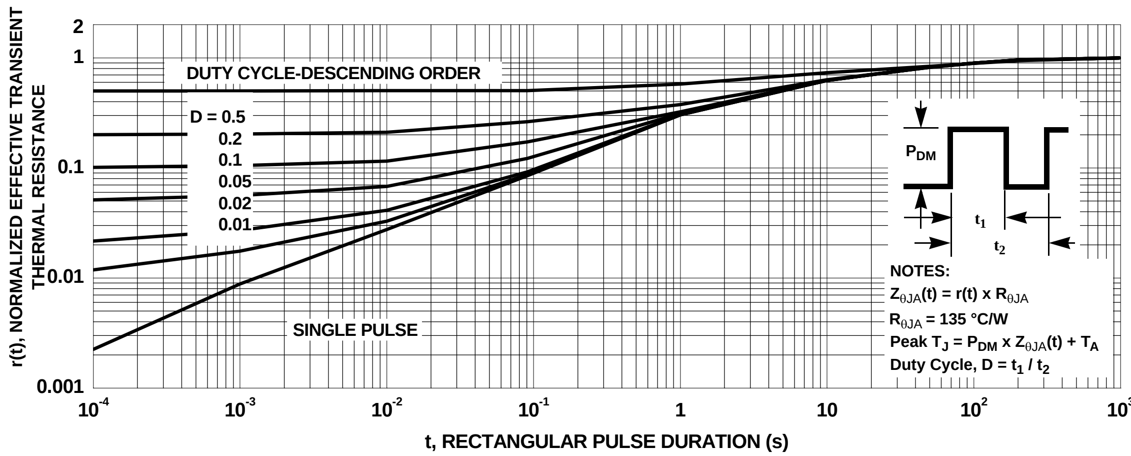
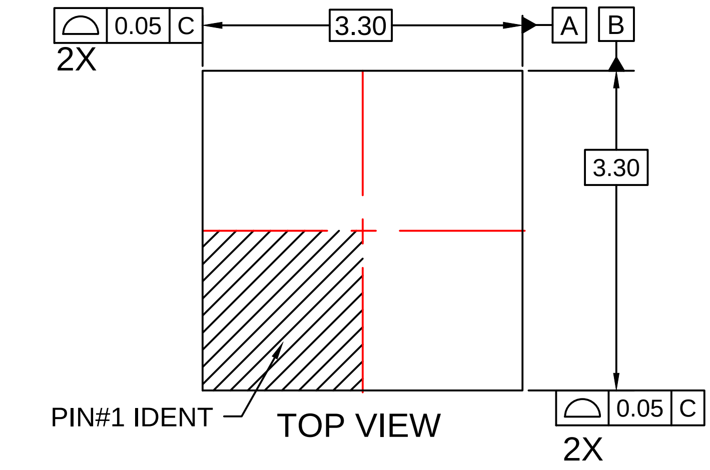
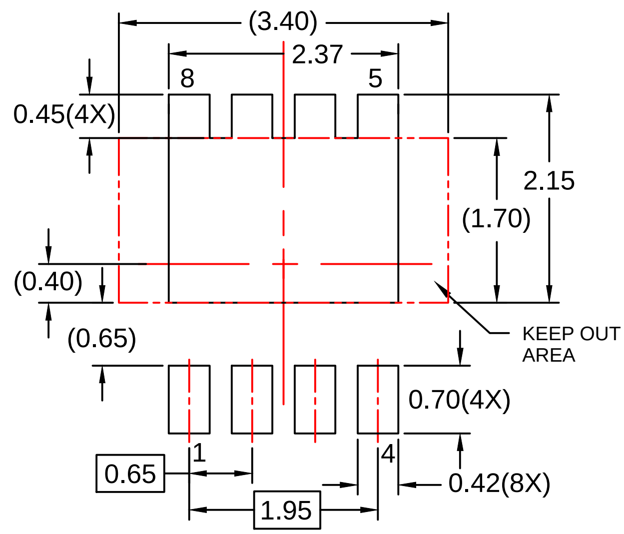
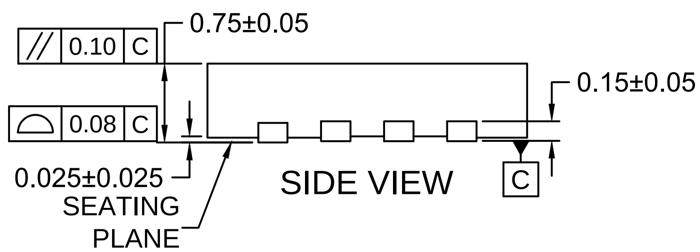


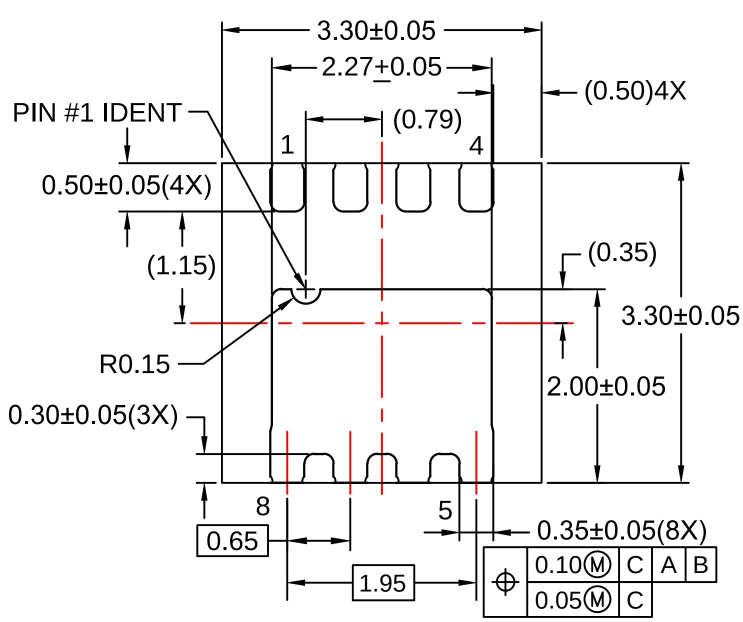
Figure 12. Transient Thermal Response Curve





RECOMMENDED LAND PATTERN





BOTTOM VIEW

NOTES:

A. DOES NOT CONFORM TO JEDEC REGISTRATION MO-229

B. DIMENSIONS ARE IN MILLIMETERS.

C. DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 2009.

D. LAND PATTERN RECOMMENDATION IS EXISTING INDUSTRY LAND PATTERN.

E. DRAWING FILENAME: MKT-MLP08Srev3.

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