

FDMC86106LZ

N-Channel Shielded Gate PowerTrench® MOSFET

100 V, 7.5 A, 103 mΩ

Features

- Shielded Gate MOSFET Technology
- Max $r_{DS(on)}$ = 103 mΩ at $V_{GS} = 10$ V, $I_D = 3.3$ A
- Max $r_{DS(on)}$ = 153 mΩ at $V_{GS} = 4.5$ V, $I_D = 2.7$ A
- HBM ESD protection level > 3 kV typical (Note 4)
- 100% UIL Tested
- RoHS Compliant

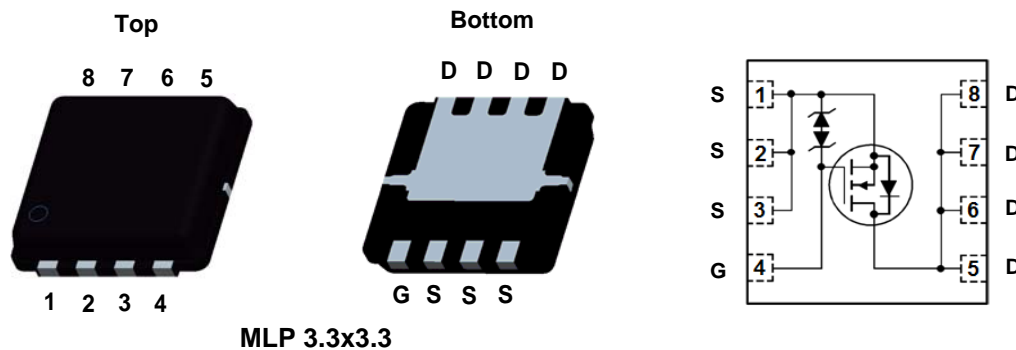


General Description

This N-Channel logic Level MOSFETs are produced using Fairchild Semiconductor's advanced PowerTrench® process that incorporates Shielded Gate technology. This process has been optimized for the on-state resistance and yet maintain superior switching performance. G-S zener has been added to enhance ESD voltage level.

Application

- DC - DC Conversion



MOSFET Maximum Ratings $T_A = 25$ °C unless otherwise noted

Symbol	Parameter	Rated	Units
V_{DS}	Drain to Source Voltage	100	V
V_{GS}	Gate to Source Voltage	±20	V
I_D	Drain Current -Continuous (Package limited) $T_C = 25$ °C	7.5	A
	-Continuous (Silicon limited) $T_C = 25$ °C	9.6	
	-Continuous $T_A = 25$ °C (Note 1a)	3.3	
	-Pulsed	15	
E_{AS}	Single Pulse Avalanche Energy (Note 3)	12	mJ
P_D	Power Dissipation $T_C = 25$ °C	19	W
	Power Dissipation $T_A = 25$ °C (Note 1a)	2.3	
T_J, T_{STG}	Operating and Storage Junction Temperature Range	-55 to +150	°C

Thermal Characteristics

$R_{\theta JC}$	Thermal Resistance, Junction to Case	6.5	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1a)	53	

Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
FDMC86106Z	FDMC86106LZ	Power 33	13 "	12 mm	3000 units

Electrical Characteristics $T_J = 25\text{ }^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
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Off Characteristics

BV_{DSS}	Drain to Source Breakdown Voltage	$I_D = 250\text{ }\mu\text{A}$, $V_{GS} = 0\text{ V}$	100			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	$I_D = 250\text{ }\mu\text{A}$, referenced to $25\text{ }^\circ\text{C}$		73		mV/ $^\circ\text{C}$
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = 80\text{ V}$, $V_{GS} = 0\text{ V}$			1	μA
I_{GSS}	Gate to Source Leakage Current	$V_{GS} = \pm 20\text{ V}$, $V_{DS} = 0\text{ V}$			± 10	μA

On Characteristics

$V_{GS(th)}$	Gate to Source Threshold Voltage	$V_{GS} = V_{DS}$, $I_D = 250\text{ }\mu\text{A}$	1.0	1.8	2.2	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate to Source Threshold Voltage Temperature Coefficient	$I_D = 250\text{ }\mu\text{A}$, referenced to $25\text{ }^\circ\text{C}$		-6		mV/ $^\circ\text{C}$
$r_{DS(on)}$	Static Drain to Source On Resistance	$V_{GS} = 10\text{ V}$, $I_D = 3.3\text{ A}$		79	103	m Ω
		$V_{GS} = 4.5\text{ V}$, $I_D = 2.7\text{ A}$		105	153	
		$V_{GS} = 10\text{ V}$, $I_D = 3.3\text{ A}$, $T_J = 125\text{ }^\circ\text{C}$		136	178	
g_{FS}	Forward Transconductance	$V_{DS} = 5\text{ V}$, $I_D = 3.3\text{ A}$		11		S

Dynamic Characteristics

C_{iss}	Input Capacitance	$V_{DS} = 50\text{ V}$, $V_{GS} = 0\text{ V}$, $f = 1\text{ MHz}$		232	310	pF
C_{oss}	Output Capacitance			45	60	pF
C_{rss}	Reverse Transfer Capacitance			2.4	5	pF
R_g	Gate Resistance			0.7		Ω

Switching Characteristics

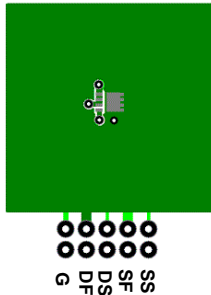
$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = 50\text{ V}$, $I_D = 3.3\text{ A}$, $V_{GS} = 10\text{ V}$, $R_{GEN} = 6\text{ }\Omega$		4.5	10	ns	
t_r	Rise Time			1.3	10	ns	
$t_{d(off)}$	Turn-Off Delay Time			10	20	ns	
t_f	Fall Time			1.4	10	ns	
$Q_{g(TOT)}$	Total Gate Charge		$V_{GS} = 0\text{ V to } 10\text{ V}$		4	6	nC
$Q_{g(TOT)}$	Total Gate Charge	$V_{GS} = 0\text{ V to } 4.5\text{ V}$	$V_{DD} = 50\text{ V}$, $I_D = 3.3\text{ A}$		2	3	nC
Q_{gs}	Total Gate Charge				0.8		nC
Q_{gd}	Gate to Drain "Miller" Charge				0.7		nC

Drain-Source Diode Characteristics

V_{SD}	Source to Drain Diode Forward Voltage	$V_{GS} = 0\text{ V}$, $I_S = 3.3\text{ A}$ (Note 2)		0.85	1.3	V
		$V_{GS} = 0\text{ V}$, $I_S = 2\text{ A}$ (Note 2)		0.82	1.2	
t_{rr}	Reverse Recovery Time	$I_F = 3.3\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$		33	54	ns
Q_{rr}	Reverse Recovery Charge			23	38	nC

NOTES:

1. $R_{\theta JA}$ is determined with the device mounted on a 1 in^2 pad 2 oz copper pad on a $1.5 \times 1.5\text{ in.}$ board of FR-4 material. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.



a. $53\text{ }^\circ\text{C/W}$ when mounted on a 1 in^2 pad of 2 oz copper



b. $125\text{ }^\circ\text{C/W}$ when mounted on a minimum pad of 2 oz copper

2. Pulse Test: Pulse Width < $300\text{ }\mu\text{s}$, Duty cycle < 2.0%.

3. Starting $T_J = 25\text{ }^\circ\text{C}$; N-ch: $L = 1.0\text{ mH}$, $I_{AS} = 5.0\text{ A}$, $V_{DD} = 90\text{ V}$, $V_{GS} = 10\text{ V}$.

4. The diode connected between gate and source serves only as protection against ESD. No gate overvoltage rating is implied.

Typical Characteristics $T_J = 25\text{ }^\circ\text{C}$ unless otherwise noted

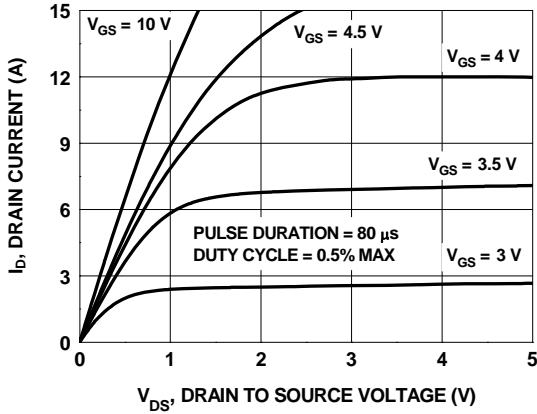


Figure 1. On Region Characteristics

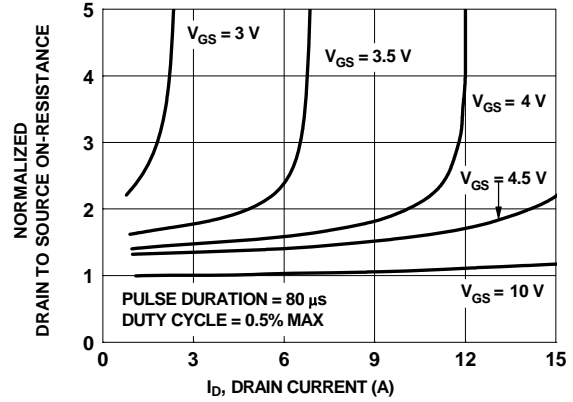


Figure 2. Normalized On-Resistance vs Drain Current and Gate Voltage

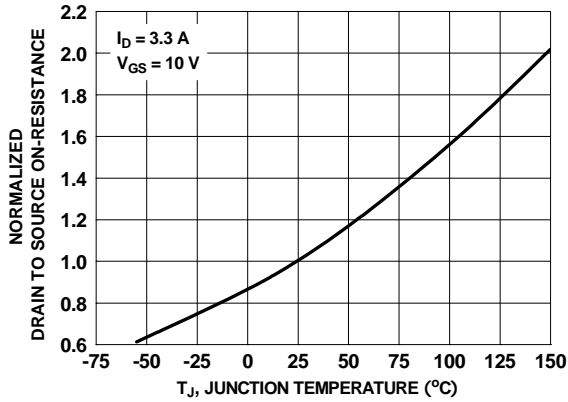


Figure 3. Normalized On Resistance vs Junction Temperature

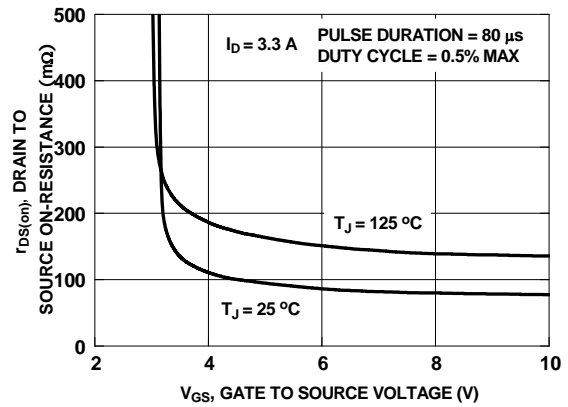


Figure 4. On-Resistance vs Gate to Source Voltage

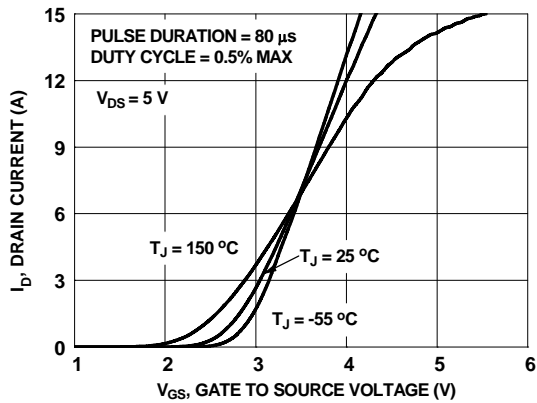


Figure 5. Transfer Characteristics

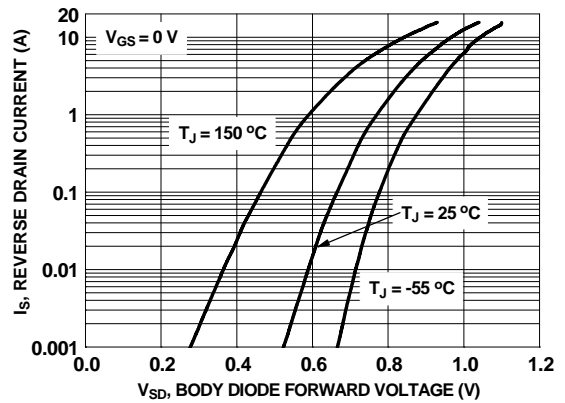


Figure 6. Source to Drain Diode Forward Voltage vs Source Current

Typical Characteristics $T_J = 25\text{ }^\circ\text{C}$ unless otherwise noted

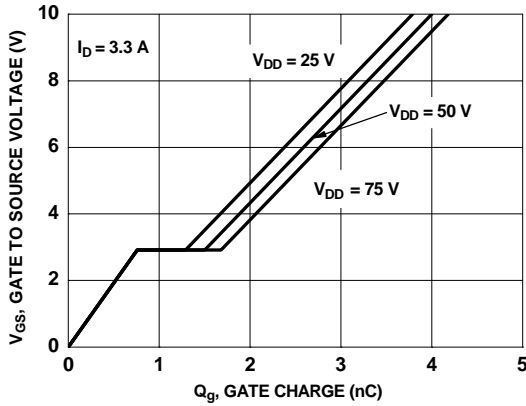


Figure 7. Gate Charge Characteristics

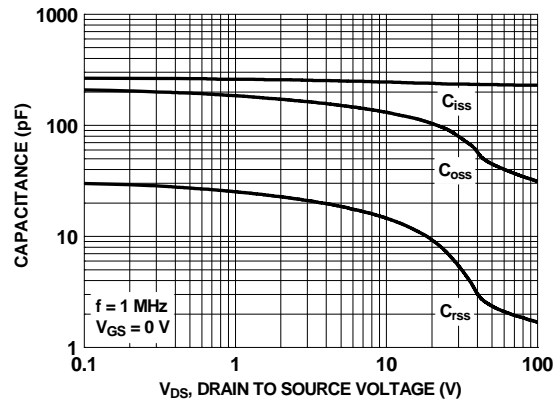


Figure 8. Capacitance vs Drain to Source Voltage

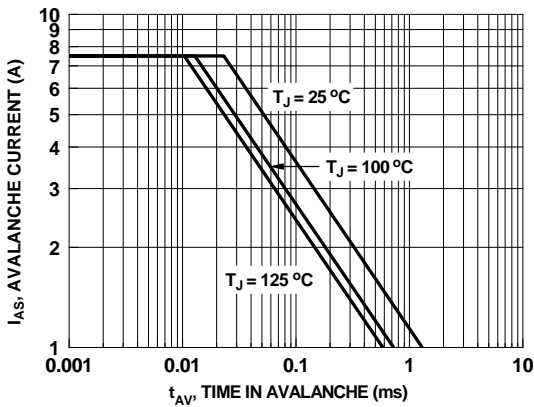


Figure 9. Unclamped Inductive Switching Capability

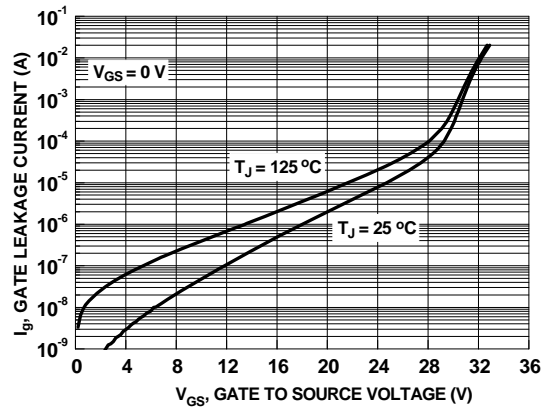


Figure 10. Gate Leakage Current vs Gate to Source Voltage

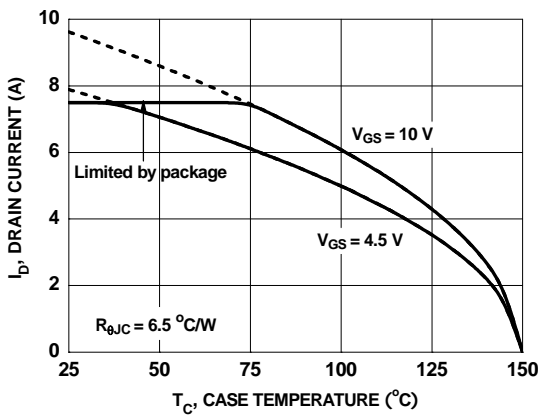


Figure 11. Maximum Continuous Drain Current vs Case Temperature

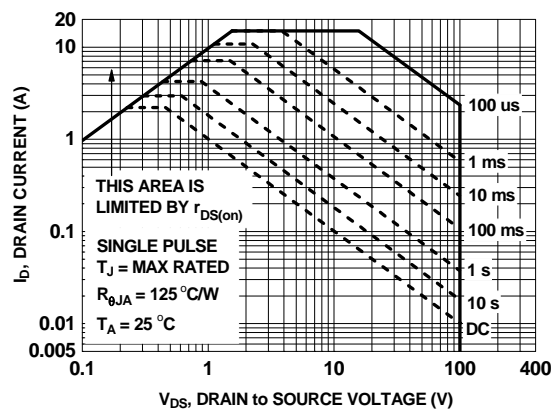


Figure 12. Forward Bias Safe Operating Area

Typical Characteristics $T_J = 25\text{ }^\circ\text{C}$ unless otherwise noted

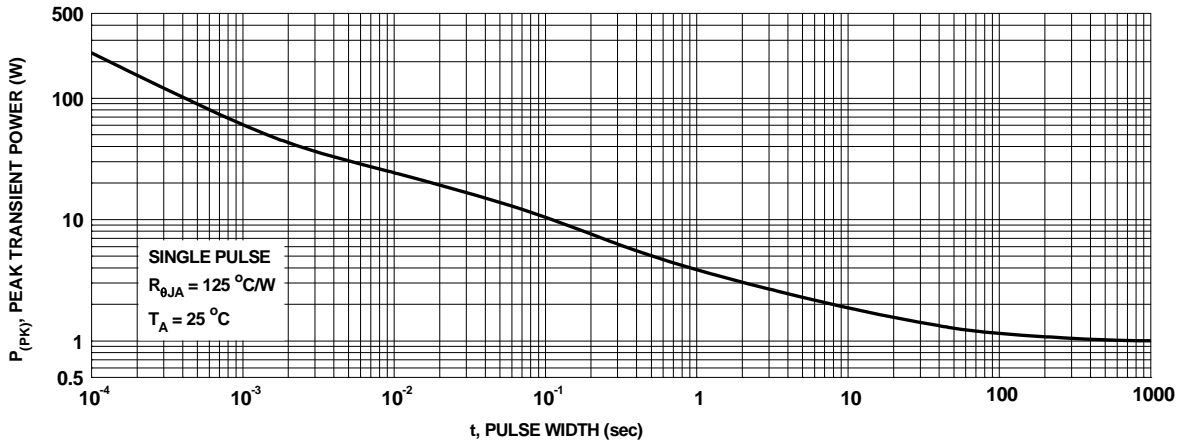


Figure 13. Single Pulse Maximum Power Dissipation

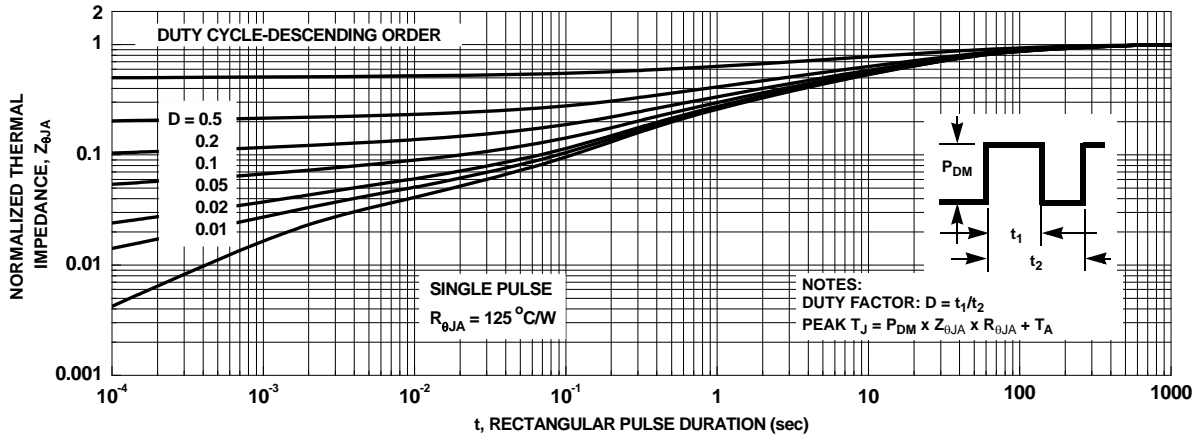
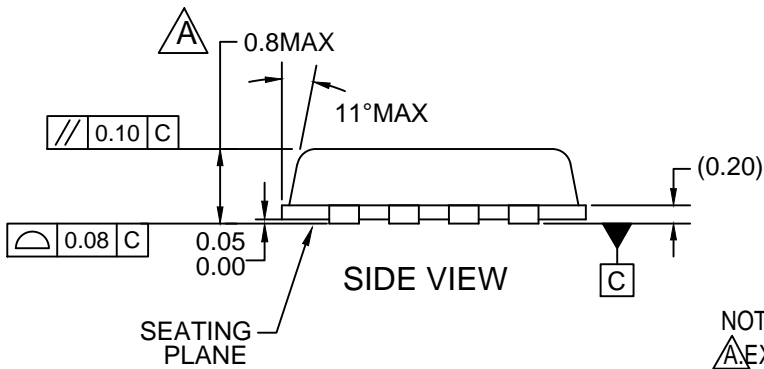
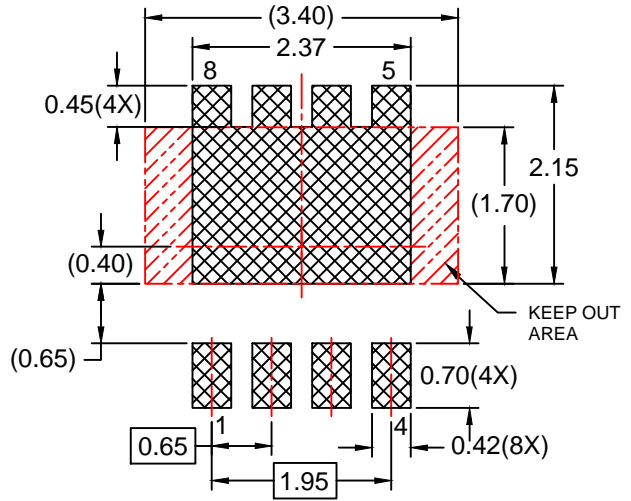
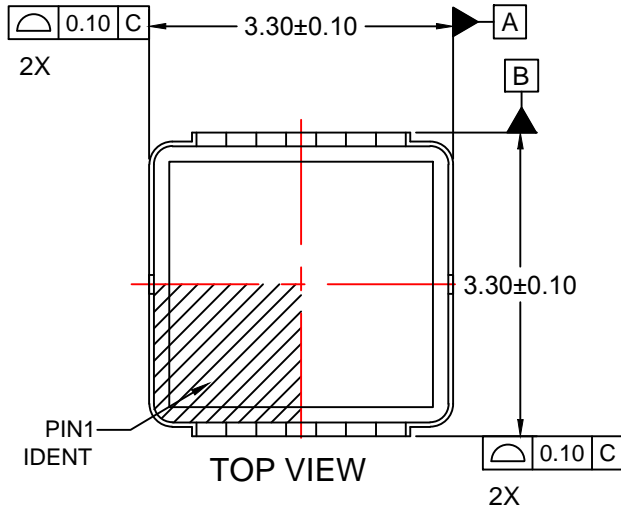


Figure 14. Junction-to-Ambient Transient Thermal Response Curve

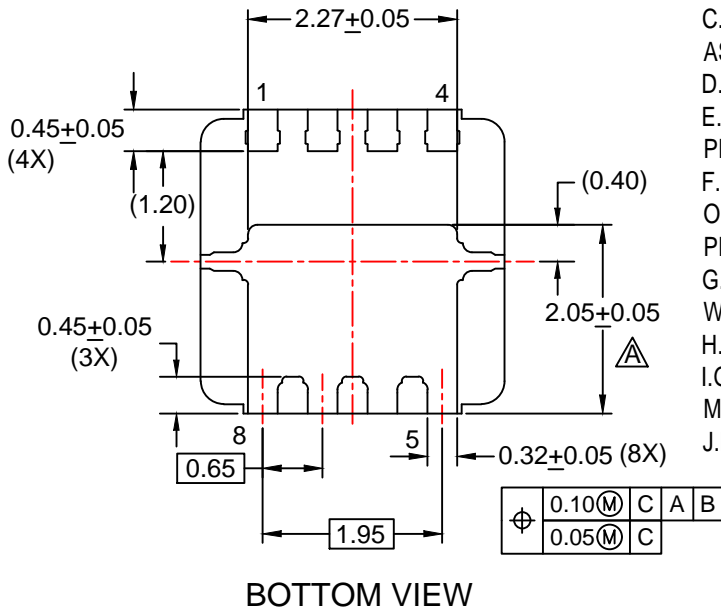
Dimensional Outline and Pad Layout



RECOMMENDED LAND PATTERN

NOTES:

- A. EXCEPT AS NOTED, PACKAGE CONFORMS TO JEDEC REGISTRATION MO-240 VARIATION BA..
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- C. DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994.
- D. SEATING PLANE IS DEFINED BY TERMINAL TIPS ONLY
- E. BODY DIMENSIONS DO NOT INCLUDE MOLD FLASH PROTRUSIONS NOR GATEBURRS.
- F. FLANGE DIMENSIONS INCLUDE INTERTERMINAL FLASH OR PROTRUSION. INTERTERMINAL FLASH OR PROTRUSION SHALL NOT EXCEED 0.25MM PER SIDE.
- G. IT IS RECOMMENDED TO HAVE NO TRACES OR VIA WITHIN THE KEEP OUT AREA.
- H. DRAWING FILENAME: MKT-MLP08Trev3.
- I. GENERAL RADII FOR ALL CORNERS SHALL BE 0.20MM MAX.
- J. FAIRCHILD SEMICONDUCTOR.




⊕	0.10(M)	C	A	B
	0.05(M)	C		



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Definition of Terms

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Preliminary	First Production	Datasheet contains preliminary data; supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve design.
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