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September 2016

FDMC86260

N-Channel Shielded Gate PowerTrench® MOSFET 150 V, 25 A, 34 m Ω

Features

- Shielded Gate MOSFET Technology
- Max $r_{DS(on)}$ = 34 m Ω at V_{GS} = 10 V, I_D = 5.4 A
- Max $r_{DS(on)}$ = 44 m Ω at V_{GS} = 6 V, I_D = 4.8 A
- High Performance Technology for Extremely Low r_{DS(on)}
- 100% UIL Tested
- Termination is Lead-free
- RoHS Compliant

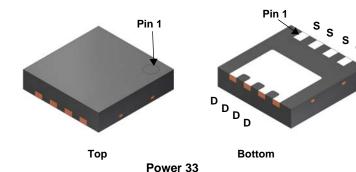


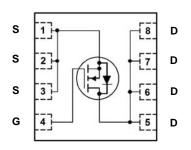
General Description

This N-Channel MOSFET is produced using Fairchild Semiconductor's advanced PowerTrench® process that incorporates Shielded Gate technology. This process has been optimized for the on-state resistance and yet maintain superior switching performance.

Application

■ DC-DC Conversion





MOSFET Maximum Ratings T_A = 25 °C unless otherwise noted.

Symbol	Parameter				Ratings	Units
V _{DS}	Drain to Source	Voltage			150	V
V _{GS}	Gate to Source \	/oltage			±20	V
	Drain Current	-Continuous	T _C = 25 °C	(Note 5)	25	
		-Continuous	T _C = 100°C	(Note 5)	16	A
ID		-Continuous	T _A = 25 °C	(Note 1a)	5.4	A
		-Pulsed		(Note 4)	135	
E _{AS}	Single Pulse Ava	lanche Energy		(Note 3)	121	mJ
D	Power Dissipatio	n	T _C = 25 °C		54	W
P_{D}	Power Dissipatio	n	T _A = 25 °C	(Note 1a)	2.3	VV
T _J , T _{STG}	Operating and St	torage Junction Temperat	ure Range		-55 to +150	°C

Thermal Characteristics

$R_{\theta JC}$	Thermal Resistance, Junction to Case	(Note 1)	2.3	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	(Note 1a)	53	C/VV

Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
FDMC86260	FDMC86260	Power33	13 "	12 mm	3000 units

Electrical Characteristics $T_J = 25$ °C unless otherwise noted.

Symbol	Parameter	Test Conditions	Min.	Тур.	Max.	Units
Off Chara	cteristics					
BV _{DSS}	Drain to Source Breakdown Voltage	$I_D = 250 \mu A, V_{GS} = 0 V$	150			V
$\Delta BV_{DSS} \over \Delta T_{J}$	Breakdown Voltage Temperature Coefficient	I_D = 250 μ A, referenced to 25 °C		110		mV/°C
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} = 120 V, V _{GS} = 0 V			1	μΑ
I _{GSS}	Gate to Source Leakage Current	$V_{GS} = \pm 20 \text{ V}, V_{DS} = 0 \text{ V}$			±100	nA

On Characteristics

V _{GS(th)}	Gate to Source Threshold Voltage	$V_{GS} = V_{DS}, I_{D} = 250 \mu A$	2	2.7	4	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate to Source Threshold Voltage Temperature Coefficient	I_D = 250 μ A, referenced to 25 °C		-9		mV/°C
		$V_{GS} = 10 \text{ V}, I_D = 5.4 \text{ A}$		27	34	
r _{DS(on)}	Static Drain to Source On Resistance	$V_{GS} = 6 \text{ V}, I_D = 4.8 \text{ A}$		31	44	mΩ
, ,		$V_{GS} = 10 \text{ V}, I_D = 5.4 \text{ A}, T_J = 125 ^{\circ}\text{C}$		55	69	
g _{FS}	Forward Transconductance	$V_{DD} = 10 \text{ V}, I_D = 5.4 \text{ A}$		19		S

Dynamic Characteristics

C _{iss}	Input Capacitance	V 75.V.V 0.V		1000	1330	pF
Coss	Output Capacitance	$V_{DS} = 75 \text{ V}, V_{GS} = 0 \text{ V},$ f = 1 MHz		105	140	pF
C _{rss}	Reverse Transfer Capacitance	1 - 1 1/11/12		4.8	10	pF
R_{q}	Gate Resistance		0.1	0.6	1.8	Ω

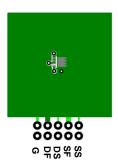
Switching Characteristics

t _{d(on)}	Turn-On Delay Time			9.5	19	ns
t _r	Rise Time	V _{DD} = 75 V, I _D = 5.4	4 A,	2	10	ns
t _{d(off)}	Turn-Off Delay Time	V _{GS} = 10 V, R _{GEN} =	= 6 Ω	17	30	ns
t _f	Fall Time			3.3	10	ns
$Q_{g(TOT)}$	Total Gate Charge	$V_{GS} = 0 \text{ V to } 10 \text{ V}$		15	21	nC
$Q_{g(TOT)}$	Total Gate Charge	$V_{GS} = 0 V to 6 V$	V _{DD} = 75 V,	9.7	14	nC
Q_{gs}	Total Gate Charge		$I_D = 5.4 \text{ A}$	4.0		nC
Q_{gd}	Gate to Drain "Miller" Charge			3.1		nC

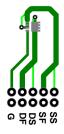
Drain-Source Diode Characteristics

V	V _{SD} Source to Drain Diode Forward Voltage	$V_{GS} = 0 \text{ V}, I_S = 5.4 \text{ A}$ (Note 2)		0.77	1.3	V	
VSC)	Source to Drain Diode 1 of ward voltage	$V_{GS} = 0 \text{ V}, I_S = 1.9 \text{ A}$ (Note 2)		0.72	1.2	V
t _{rr}		Reverse Recovery Time	L = 5.4 A di/dt = 100 A/us		64	102	ns
Q_{rr}		Reverse Recovery Charge	I _F = 5.4 A, di/dt = 100 A/μs		85	137	nC

^{1.} R_{0,JA} is determined with the device mounted on a 1 in² pad 2 oz copper pad on a 1.5 x 1.5 in. board of FR-4 material. R_{0,JC} is guaranteed by design while R_{0,CA} is determined by the user's board design.



a. 53 °C/W when mounted on a 1 in² pad of 2 oz copper



b. 125 °C/W when mounted on a minimum pad of 2 oz copper

- 2. Pulse Test: Pulse Width < 300 μ s, Duty cycle < 2.0%. 3. E_{AS} of 121 mJ is based on starting T_J = 25 °C, L = 3 mH, I_{AS} = 9 A, V_{DD} = 150 V, V_{GS} = 10 V. 100% test at L = 0.1 mH, I_{AS} = 22 A. 4. Pulsed Id please refer to Fig 11 SOA graph for more details.
- 5. Computed continuous current limited to Max Junction Temperature only, actual continuous current will be limited by thermal & electro-mechanical application board design.

Typical Characteristics $T_J = 25$ °C unless otherwise noted.

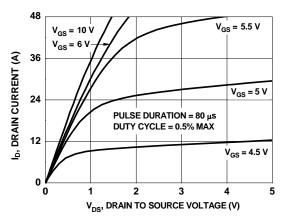


Figure 1. On-Region Characteristics

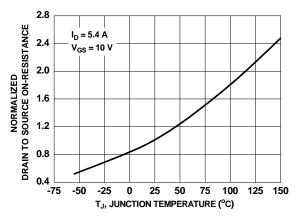


Figure 3. Normalized On-Resistance vs. Junction Temperature

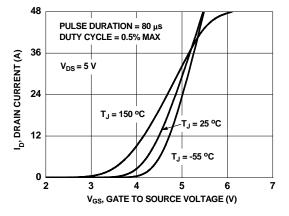


Figure 5. Transfer Characteristics

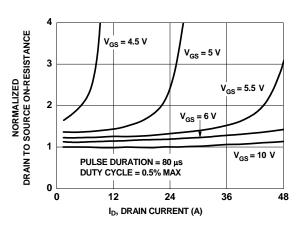


Figure 2. Normalized On-Resistance vs. Drain Current and Gate Voltage

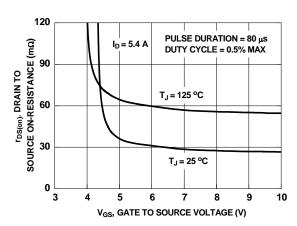


Figure 4. On-Resistance vs. Gate to Source Voltage

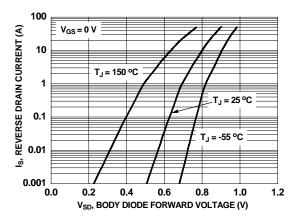


Figure 6. Source to Drain Diode Forward Voltage vs. Source Current

Typical Characteristics $T_J = 25 \, ^{\circ}\text{C}$ unless otherwise noted.

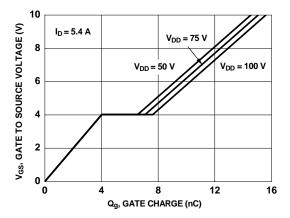


Figure 7. Gate Charge Characteristics

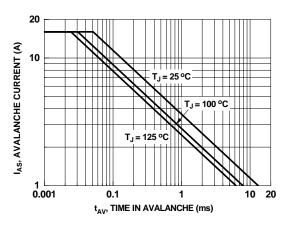


Figure 9. Unclamped Inductive Switching Capability

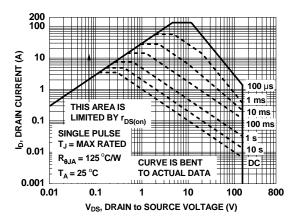


Figure 11. Forward Bias Safe Operating Area

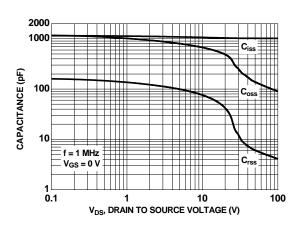


Figure 8. Capacitance vs. Drain to Source Voltage

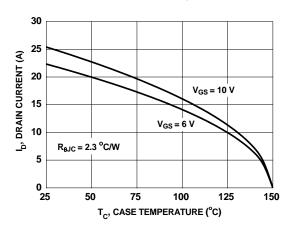


Figure 10. Maximum Continuous Drain Current vs. Case Temperature

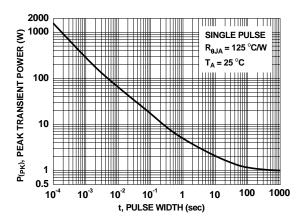


Figure 12. Single Pulse Maximum Power Dissipation

Typical Characteristics $T_J = 25 \, ^{\circ}\text{C}$ unless otherwise noted.

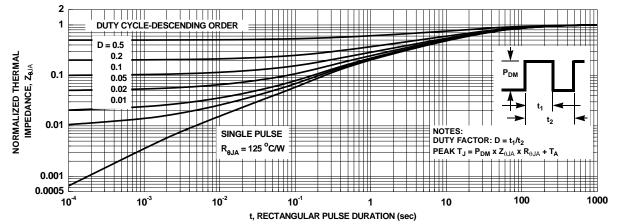
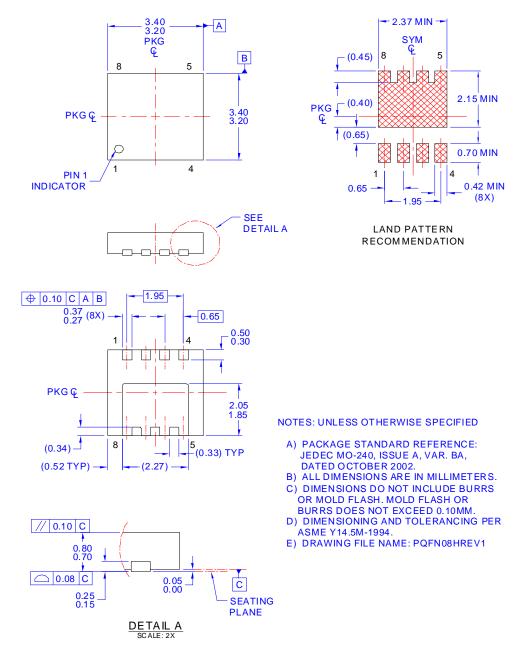


Figure 13. Junction-to-Ambient Transient Thermal Response Curve

Dimensional Outline and Pad Layout



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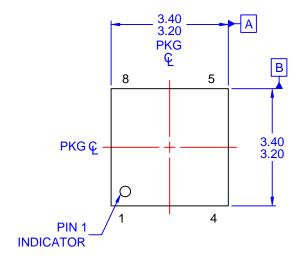
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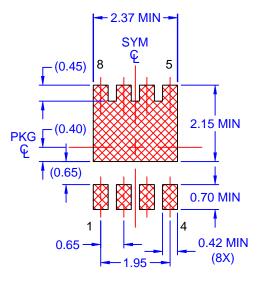
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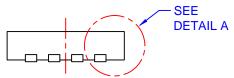
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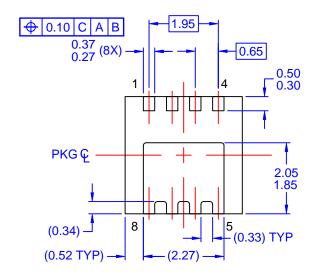
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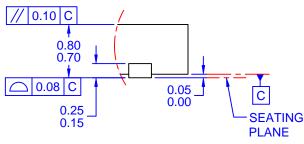


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