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FDMC8884

### June 2014

# N-Channel PowerTrench<sup>®</sup> MOSFET 30 V, 15 A, 19 m $\Omega$

#### **Features**

- Max  $r_{DS(on)} = 19 \text{ m}\Omega$  at  $V_{GS} = 10 \text{ V}$ ,  $I_D = 9.0 \text{ A}$
- Max  $r_{DS(on)}$  = 30 m $\Omega$  at  $V_{GS}$  = 4.5 V,  $I_D$  = 7.2 A
- High performance technology for extremely low r<sub>DS(on)</sub>
- Termination is Lead-free and RoHS Compliant

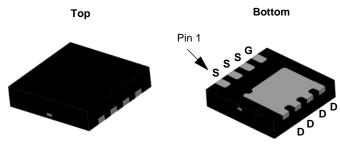


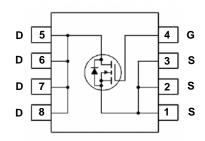
#### **General Description**

This N-Channel MOSFET is produced using Fairchild Semiconductor's advanced PowerTrench<sup>®</sup> process that has been especially tailored to minimize the on-state resistance. This device is well suited for Power Management and load switching applications common in Notebook Computers and Portable Battery Packs.

#### **Application**

- High side in DC DC Buck Converters
- Notebook battery power management
- Load switch in Notebook





MLP 3.3x3.3

## **MOSFET Maximum Ratings** $T_A = 25 \, ^{\circ}\text{C}$ unless otherwise noted

Symbol	Parame		Ratings	Units	
$V_{DS}$	Drain to Source Voltage			30	V
$V_{GS}$	Gate to Source Voltage			±20	V
	Drain Current -Continuous	T <sub>C</sub> = 25 °C		15	
$I_D$	-Continuous	T <sub>A</sub> = 25 °C	(Note 1a)	9.0	Α
	-Pulsed			40	
E <sub>AS</sub>	Single Pulse Avalanche Energy		(Note 3)	24	mJ
D	Power Dissipation	T <sub>C</sub> = 25 °C		18	W
$P_{D}$	Power Dissipation	T <sub>A</sub> = 25 °C	(Note 1a)	2.3	VV
T <sub>J</sub> , T <sub>STG</sub>	Operating and Storage Junction Temperat	Operating and Storage Junction Temperature Range			°C

#### **Thermal Characteristics**

$R_{\theta JC}$	Thermal Resistance, Junction to Case	6.6	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1a)	53	C/VV

#### **Package Marking and Ordering Information**

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
FDMC8884	FDMC8884	MLP 3.3x3.3	13 "	12 mm	3000 units

## Electrical Characteristics T<sub>J</sub> = 25 °C unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Тур	Max	Units
Off Chara	acteristics					
BV <sub>DSS</sub>	Drain to Source Breakdown Voltage	$I_D = 250 \mu A, V_{GS} = 0 V$	30			V
ΔBV <sub>DSS</sub> _ΔT <sub>J</sub>	Breakdown Voltage Temperature Coefficient	$I_D$ = 250 $\mu$ A, referenced to 25 °C		22		mV/°C
laco	Zero Gate Voltage Drain Current	V <sub>DS</sub> = 24 V, V <sub>GS</sub> = 0 V			1	μА
IDSS	Zero Gate Voltage Drain Guirent	T <sub>J</sub> = 125 °C			250	μΛ
I <sub>GSS</sub>	Gate to Source Leakage Current	V <sub>GS</sub> = ±20 V, V <sub>DS</sub> = 0 V			±100	nA

#### **On Characteristics**

V <sub>GS(th)</sub>	Gate to Source Threshold Voltage	$V_{GS} = V_{DS}, I_D = 250 \mu A$	1.4	1.9	2.5	V
$\Delta V_{GS(th)}$ $\Delta T_J$	Gate to Source Threshold Voltage Temperature Coefficient	$I_D$ = 250 $\mu$ A, referenced to 25 °C		-6		mV/°C
		$V_{GS} = 10 \text{ V}, I_D = 9.0 \text{ A}$		16	19	
r <sub>DS(on)</sub>	Static Drain to Source On Resistance	$V_{GS} = 4.5 \text{ V}, I_D = 7.2 \text{ A}$		22	30	mΩ
, ,		$V_{GS} = 10 \text{ V}, I_D = 9.0 \text{ A}, T_J = 125 ^{\circ}\text{C}$		22	30	
9 <sub>FS</sub>	Forward Transconductance	$V_{DD} = 5 \text{ V}, I_{D} = 9.0 \text{ A}$		24		S

#### **Dynamic Characteristics**

C <sub>iss</sub>	Input Capacitance	V 45 V V 0 V	513	685	pF
Coss	Output Capacitance	$V_{DS} = 15 \text{ V}, V_{GS} = 0 \text{ V},$ f = 1  MHz	110	150	pF
C <sub>rss</sub>	Reverse Transfer Capacitance	1 - 1 101112	76	115	pF
R <sub>a</sub>	Gate Resistance		1.4	2.1	Ω

#### **Switching Characteristics**

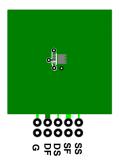
t <sub>d(on)</sub>	Turn-On Delay Time		6	12	ns
t <sub>r</sub>	Rise Time	V <sub>DD</sub> = 15 V, I <sub>D</sub> = 9.0 A,	2	10	ns
t <sub>d(off)</sub>	Turn-Off Delay Time	$V_{GS}$ = 10 V, $R_{GEN}$ = 6 $\Omega$	15	27	ns
t <sub>f</sub>	Fall Time		2	10	ns
Q <sub>g(TOT)</sub>	Total Gate Charge	V <sub>GS</sub> = 0 V to 10 V	10	14	nC
	Total Gate Charge	$V_{GS} = 0 \text{ V to } 4.5 \text{ V} V_{DD} = 15 \text{ V}$	5.0	7.0	nC
$Q_{gs}$	Total Gate Charge	I <sub>D</sub> = 9.0 A	1.8		nC
$Q_{gd}$	Gate to Drain "Miller" Charge		2.2		nC

#### **Drain-Source Diode Characteristics**

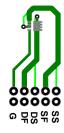
V <sub>SD</sub>	150Urce to Drain Diode Forward Voltage	$V_{GS} = 0 \text{ V}, I_{S} = 9.0 \text{ A}$ (Note 2)	0.86	1.2	V
		$V_{GS} = 0 \text{ V}, I_{S} = 1.6 \text{ A}$ (Note 2)	0.76	1.2	
t <sub>rr</sub>	Reverse Recovery Time	-I <sub>E</sub> = 9.0 A, di/dt = 100 A/μs	13	18	ns
Q <sub>rr</sub>	Reverse Recovery Charge	T <sub>F</sub> = 9.0 A, αναι = 100 Ανμs	3	10	nC

#### NOTES

<sup>1.</sup> R<sub>0,1A</sub> is determined with the device mounted on a 1 in<sup>2</sup> pad 2 oz copper pad on a 1.5 x 1.5 in. board of FR-4 material. R<sub>0,1C</sub> is guaranteed by design while R<sub>0,1C</sub> is determined by the user's board design.



a. 53 °C/W when mounted on a 1 in² pad of 2 oz copper



b.125 °C/W when mounted on a minimum pad of 2 oz copper

<sup>2.</sup> Pulse Test: Pulse Width < 300  $\mu s,$  Duty cycle < 2.0 %.

<sup>3.</sup>  $E_{AS}$  of 24 mJ is based on starting  $T_J$  = 25  $^{\circ}C$ , L = 1 mH,  $I_{AS}$  = 7 A,  $V_{DD}$  = 30 V,  $V_{GS}$  = 10 V. 100% test at L = 3 mH,  $I_{AS}$  = 4 A .

### Typical Characteristics T<sub>J</sub> = 25 °C unless otherwise noted

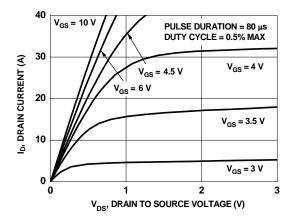
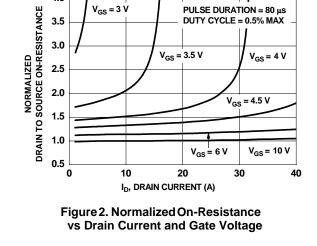


Figure 1. On-Region Characteristics



4.0

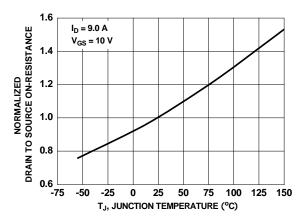


Figure 3. Normalized On-Resistance vs Junction Temperature

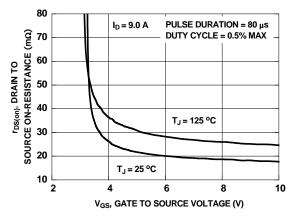


Figure 4. On-Resistance vs Gate to Source Voltage

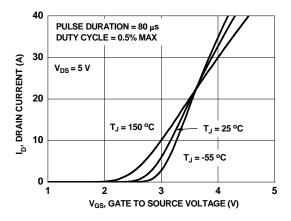


Figure 5. Transfer Characteristics

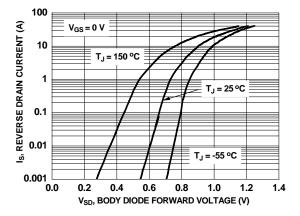


Figure 6. Source to Drain Diode Forward Voltage vs Source Current

## **Typical Characteristics** $T_J = 25$ °C unless otherwise noted

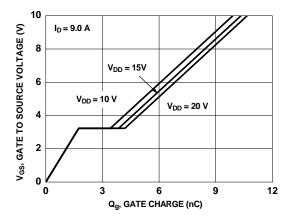


Figure 7. Gate Charge Characteristics

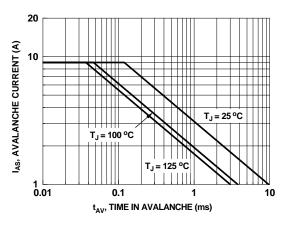


Figure 9. Unclamped Inductive Switching Capability

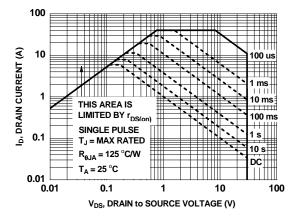


Figure 11. Forward Bias Safe Operating Area

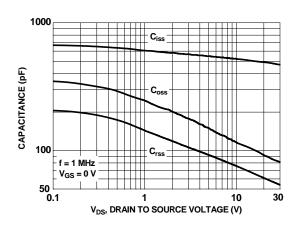


Figure 8. Capacitance vs Drain to Source Voltage

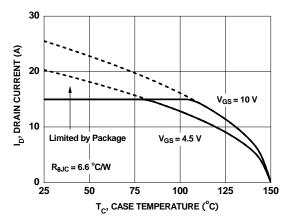


Figure 10. Maximum Continuous Drain Current vs Case Temperature

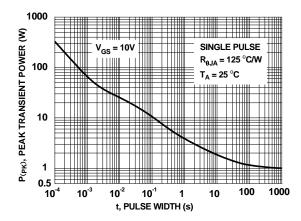


Figure 12. Single Pulse Maximum Power Dissipation

## **Typical Characteristics** $T_J = 25$ °C unless otherwise noted

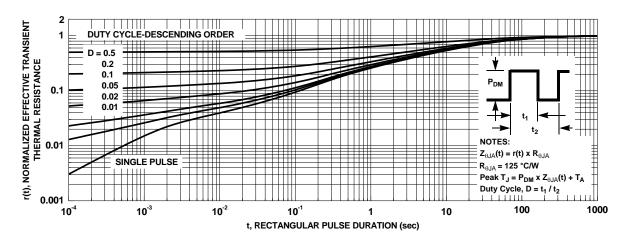
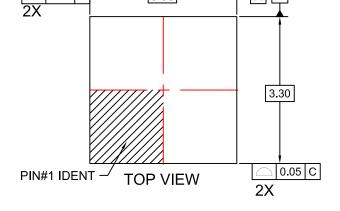
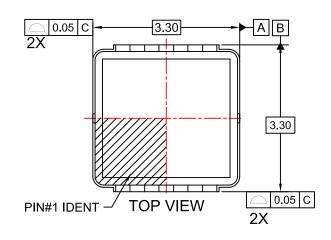
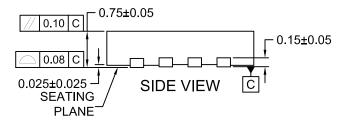
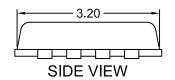


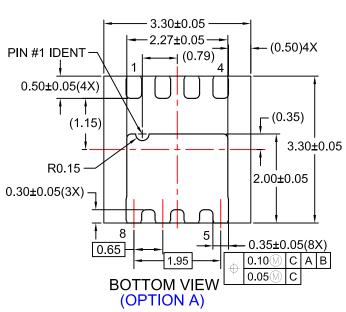
Figure 13. Transient Thermal Response Curve

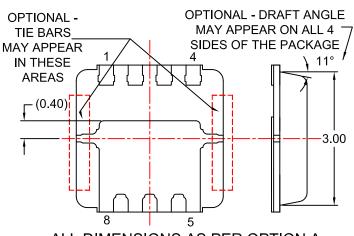


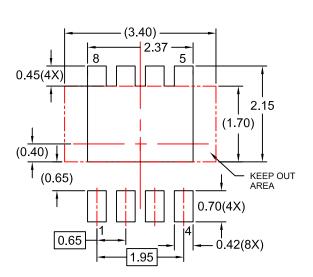








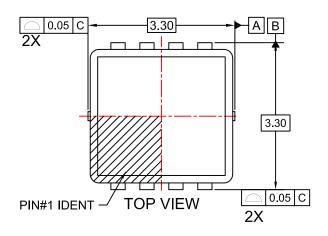


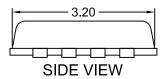


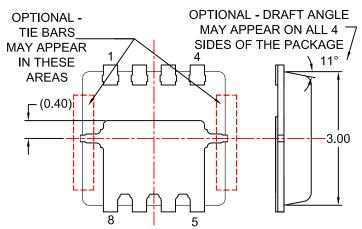
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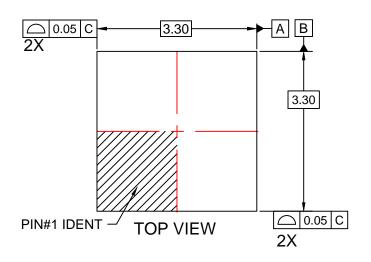


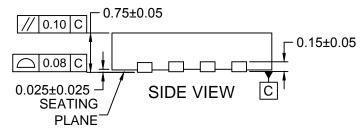
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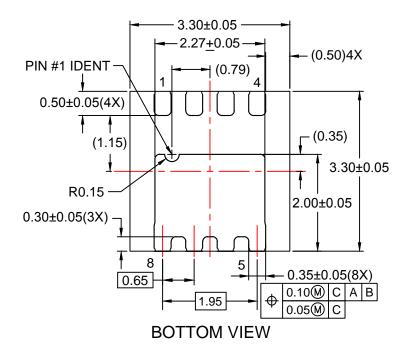
#### **NOTES:**

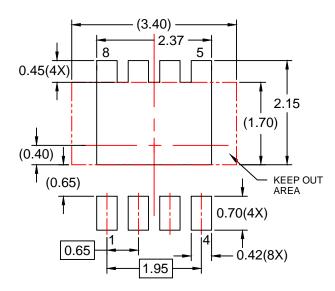
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