

# FDMS2510SDC

## N-Channel Dual Cool™ PowerTrench® SyncFET™ 25 V, 49 A, 2.9 mΩ

### Features

- Dual Cool™ Top Side Cooling PQFN package
- Max  $r_{DS(on)}$  = 2.9 mΩ at  $V_{GS} = 10$  V,  $I_D = 23$  A
- Max  $r_{DS(on)}$  = 4.2 mΩ at  $V_{GS} = 4.5$  V,  $I_D = 18$  A
- High performance technology for extremely low  $r_{DS(on)}$
- SyncFET Schottky Body Diode
- RoHS Compliant

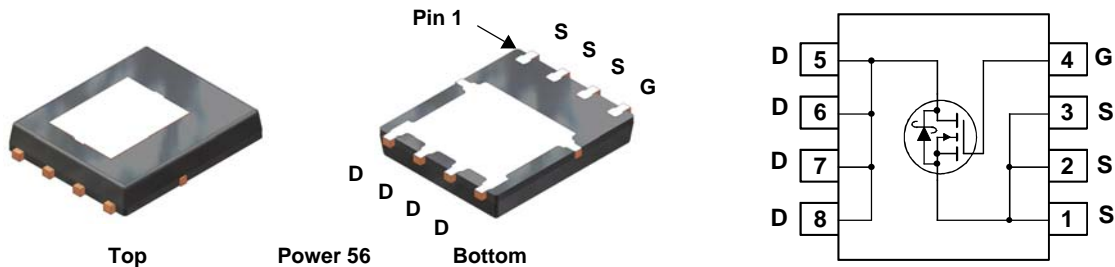


### General Description

This N-Channel MOSFET is produced using Fairchild Semiconductor's advanced PowerTrench® process. Advancements in both silicon and Dual Cool™ package technologies have been combined to offer the lowest  $r_{DS(on)}$  while maintaining excellent switching performance by extremely low Junction-to-Ambient thermal resistance. This device has the added benefit of an efficient monolithic Schottky body diode.

### Applications

- Synchronous Rectifier for DC/DC Converters
- Telecom Secondary Side Rectification
- High End Server/Workstation Vcore Low Side



### MOSFET Maximum Ratings $T_A = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Rated	Units
$V_{DS}$	Drain to Source Voltage	25	V
$V_{GS}$	Gate to Source Voltage (Note 4)	$\pm 20$	V
$I_D$	Drain Current -Continuous (Package limited) $T_C = 25^\circ\text{C}$	49	A
	-Continuous (Silicon limited) $T_C = 25^\circ\text{C}$	117	
	-Continuous $T_A = 25^\circ\text{C}$ (Note 1a)	28	
	-Pulsed	200	
$E_{AS}$	Single Pulse Avalanche Energy (Note 3)	84	mJ
$dv/dt$	Peak Diode Recovery $dv/dt$ (Note 5)	2.5	V/ns
$P_D$	Power Dissipation $T_C = 25^\circ\text{C}$	60	W
	Power Dissipation $T_A = 25^\circ\text{C}$ (Note 1a)	3.3	
$T_J, T_{STG}$	Operating and Storage Junction Temperature Range	-55 to +150	$^\circ\text{C}$

### Thermal Characteristics

Symbol	Parameter	Rated	Units
$R_{\theta JC}$	Thermal Resistance, Junction to Case (Top Source)	4.4	$^\circ\text{C/W}$
$R_{\theta JC}$	Thermal Resistance, Junction to Case (Bottom Drain)	2.1	
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1a)	38	
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1b)	81	
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1i)	16	
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1j)	23	
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1k)	11	

### Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
2510S	FDMS2510SDC	Dual Cool™ Power 56	13"	12 mm	3000 units

**Electrical Characteristics**  $T_J = 25\text{ }^\circ\text{C}$  unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
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**Off Characteristics**

$BV_{DSS}$	Drain to Source Breakdown Voltage	$I_D = 1\text{ mA}, V_{GS} = 0\text{ V}$	25			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	$I_D = 10\text{ mA}$ , referenced to $25\text{ }^\circ\text{C}$		19		mV/°C
$I_{DSS}$	Zero Gate Voltage Drain Current	$V_{DS} = 20\text{ V}, V_{GS} = 0\text{ V}$			500	$\mu\text{A}$
$I_{GSS}$	Gate to Source Leakage Current, Forward	$V_{GS} = 20\text{ V}, V_{DS} = 0\text{ V}$			100	nA

**On Characteristics**

$V_{GS(th)}$	Gate to Source Threshold Voltage	$V_{GS} = V_{DS}, I_D = 1\text{ mA}$	1.2	1.7	3.0	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate to Source Threshold Voltage Temperature Coefficient	$I_D = 10\text{ mA}$ , referenced to $25\text{ }^\circ\text{C}$		-5		mV/°C
$r_{DS(on)}$	Static Drain to Source On Resistance	$V_{GS} = 10\text{ V}, I_D = 23\text{ A}$		2.4	2.9	m $\Omega$
		$V_{GS} = 4.5\text{ V}, I_D = 18\text{ A}$		3.4	4.2	
		$V_{GS} = 10\text{ V}, I_D = 23\text{ A}, T_J = 125\text{ }^\circ\text{C}$		3.5	4.3	
$g_{FS}$	Forward Transconductance	$V_{DS} = 5\text{ V}, I_D = 23\text{ A}$		159		S

**Dynamic Characteristics**

$C_{iss}$	Input Capacitance	$V_{DS} = 13\text{ V}, V_{GS} = 0\text{ V},$ $f = 1\text{ MHz}$		2090	2780	pF
$C_{oss}$	Output Capacitance			577	770	pF
$C_{rss}$	Reverse Transfer Capacitance			128	195	pF
$R_g$	Gate Resistance			1.1	2.4	$\Omega$

**Switching Characteristics**

$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = 13\text{ V}, I_D = 23\text{ A},$ $V_{GS} = 10\text{ V}, R_{GEN} = 6\text{ }\Omega$		10	20	ns	
$t_r$	Rise Time			4	10	ns	
$t_{d(off)}$	Turn-Off Delay Time			27	43	ns	
$t_f$	Fall Time			3	10	ns	
$Q_g$	Total Gate Charge		$V_{GS} = 0\text{ V to }10\text{ V}$		32	45	nC
$Q_g$	Total Gate Charge		$V_{GS} = 0\text{ V to }4.5\text{ V}$		15	21	nC
$Q_{gs}$	Gate to Source Gate Charge	$V_{DD} = 13\text{ V},$ $I_D = 23\text{ A}$		6.3		nC	
$Q_{gd}$	Gate to Drain "Miller" Charge			4.0		nC	

**Drain-Source Diode Characteristics**

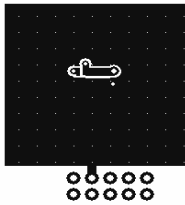
$V_{SD}$	Source to Drain Diode Forward Voltage	$V_{GS} = 0\text{ V}, I_S = 2\text{ A}$ (Note 2)		0.48	0.8	V
		$V_{GS} = 0\text{ V}, I_S = 23\text{ A}$ (Note 2)		0.79	1.2	
$t_{rr}$	Reverse Recovery Time	$I_F = 23\text{ A}, di/dt = 300\text{ A}/\mu\text{s}$		23	36	ns
$Q_{rr}$	Reverse Recovery Charge			17	31	nC

## Thermal Characteristics

$R_{\theta JC}$	Thermal Resistance, Junction to Case (Top Source)	4.4	$^{\circ}\text{C}/\text{W}$
$R_{\theta JC}$	Thermal Resistance, Junction to Case (Bottom Drain)	2.1	
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1a)	38	
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1b)	81	
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1c)	27	
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1d)	34	
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1e)	16	
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1f)	19	
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1g)	26	
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1h)	61	
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1i)	16	
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1j)	23	
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1k)	11	
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1l)	13	

### NOTES:

1.  $R_{\theta JA}$  is determined with the device mounted on specified pad 2 oz copper pad on board of FR-4 material.  $R_{\theta JC}$  is guaranteed by design while  $R_{\theta CA}$  is determined by the user's board design.



a. 38  $^{\circ}\text{C}/\text{W}$  when mounted on a 1 in<sup>2</sup> pad of 2 oz copper



b. 81  $^{\circ}\text{C}/\text{W}$  when mounted on a minimum pad of 2 oz copper

- c. Still air, 20.9x10.4x12.7mm Aluminum Heat Sink, 1 in<sup>2</sup> pad of 2 oz copper
- d. Still air, 20.9x10.4x12.7mm Aluminum Heat Sink, minimum pad of 2 oz copper
- e. Still air, 45.2x41.4x11.7mm Aavid Thermalloy Part # 10-L41B-11 Heat Sink, 1 in<sup>2</sup> pad of 2 oz copper
- f. Still air, 45.2x41.4x11.7mm Aavid Thermalloy Part # 10-L41B-11 Heat Sink, minimum pad of 2 oz copper
- g. 200FPM Airflow, No Heat Sink, 1 in<sup>2</sup> pad of 2 oz copper
- h. 200FPM Airflow, No Heat Sink, minimum pad of 2 oz copper
- i. 200FPM Airflow, 20.9x10.4x12.7mm Aluminum Heat Sink, 1 in<sup>2</sup> pad of 2 oz copper
- j. 200FPM Airflow, 20.9x10.4x12.7mm Aluminum Heat Sink, minimum pad of 2 oz copper
- k. 200FPM Airflow, 45.2x41.4x11.7mm Aavid Thermalloy Part # 10-L41B-11 Heat Sink, 1 in<sup>2</sup> pad of 2 oz copper
- l. 200FPM Airflow, 45.2x41.4x11.7mm Aavid Thermalloy Part # 10-L41B-11 Heat Sink, minimum pad of 2 oz copper

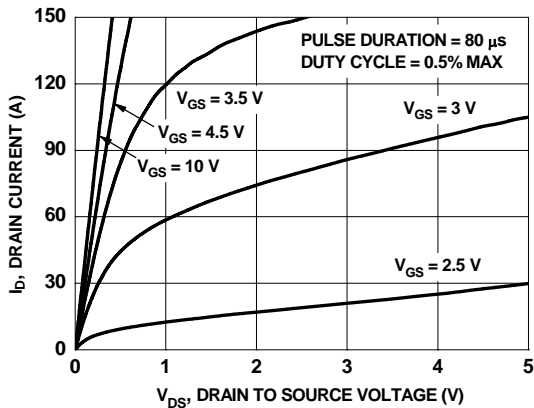
2. Pulse Test: Pulse Width < 300  $\mu\text{s}$ , Duty cycle < 2.0%.

3.  $E_{AS}$  of 84 mJ is based on starting  $T_J = 25^{\circ}\text{C}$ ,  $L = 1$  mH,  $I_{AS} = 13$  A,  $V_{DD} = 23$  V,  $V_{GS} = 10$  V. 100% test at  $L = 0.3$  mH,  $I_{AS} = 20$  A.

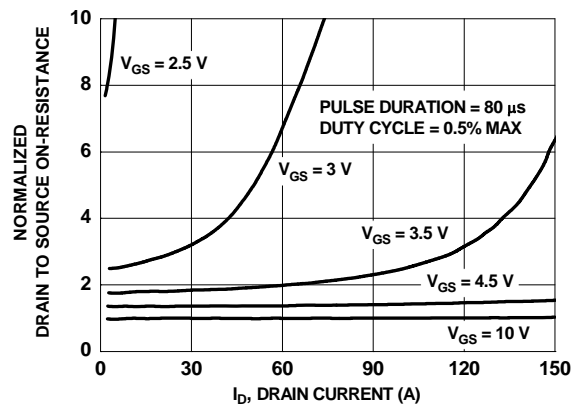
4. As an N-ch device, the negative  $V_{GS}$  rating is for low duty cycle pulse occurrence only. No continuous rating is implied.

5.  $I_{SD} \leq 23$  A,  $di/dt \leq 200$  A/ $\mu\text{s}$ ,  $V_{DD} \leq BV_{DSS}$ , Starting  $T_J = 25^{\circ}\text{C}$ .

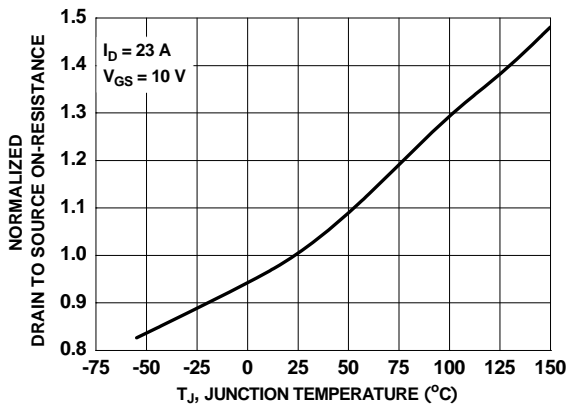
**Typical Characteristics**  $T_J = 25\text{ }^\circ\text{C}$  unless otherwise noted



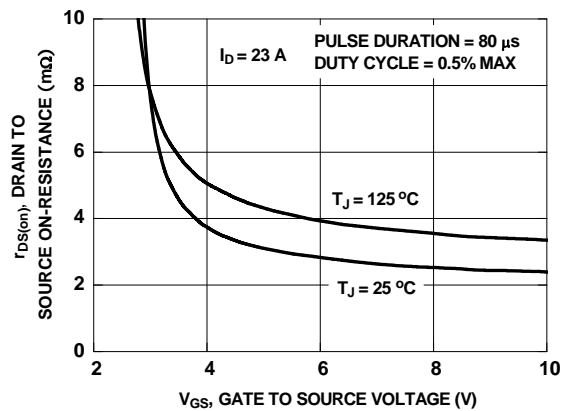
**Figure 1. On Region Characteristics**



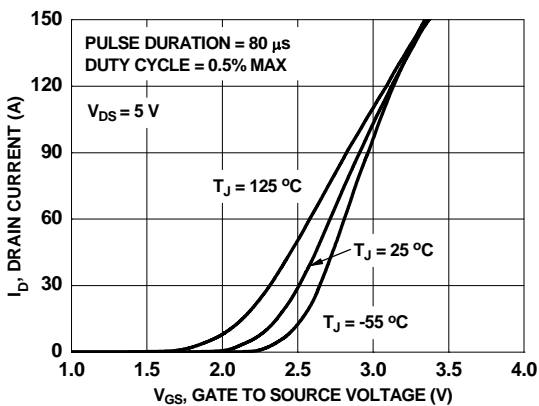
**Figure 2. Normalized On-Resistance vs Drain Current and Gate Voltage**



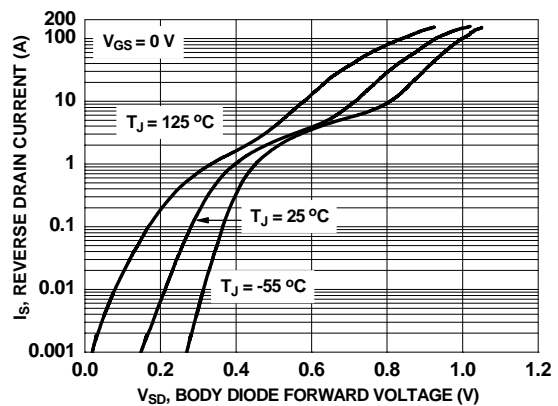
**Figure 3. Normalized On Resistance vs Junction Temperature**



**Figure 4. On-Resistance vs Gate to Source Voltage**

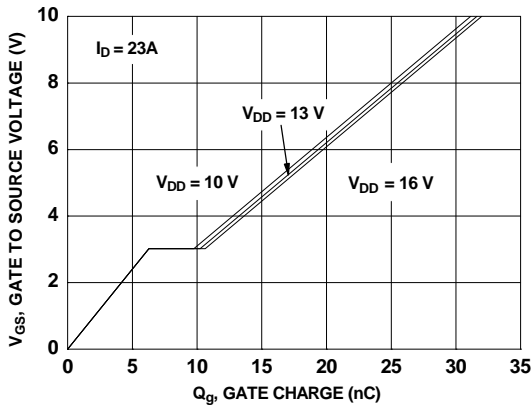


**Figure 5. Transfer Characteristics**

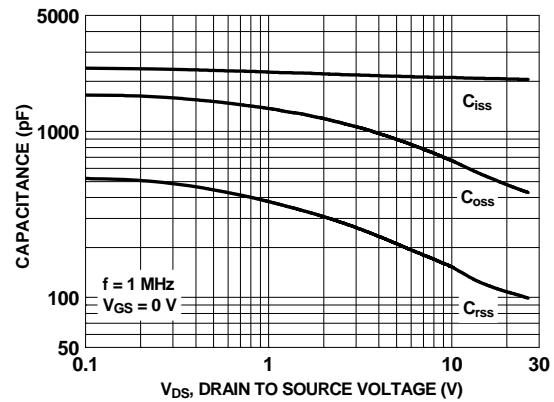


**Figure 6. Source to Drain Diode Forward Voltage vs Source Current**

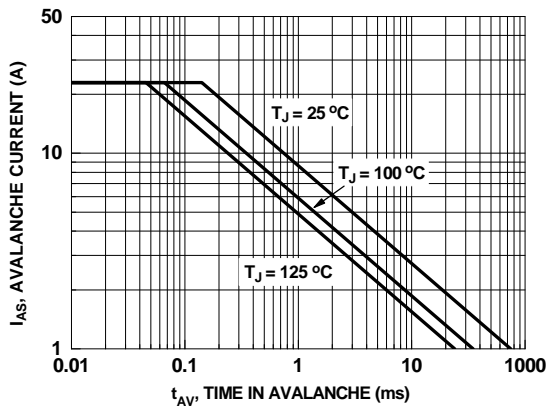
**Typical Characteristics**  $T_J = 25\text{ }^\circ\text{C}$  unless otherwise noted



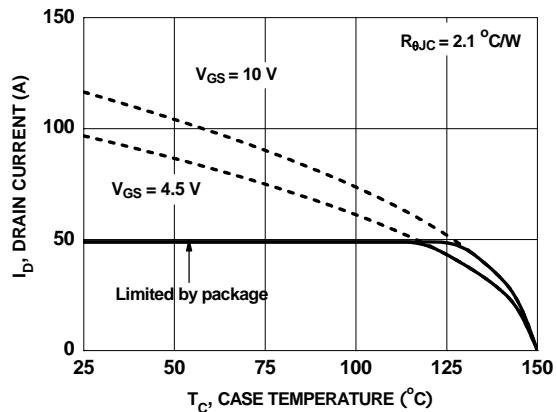
**Figure 7. Gate Charge Characteristics**



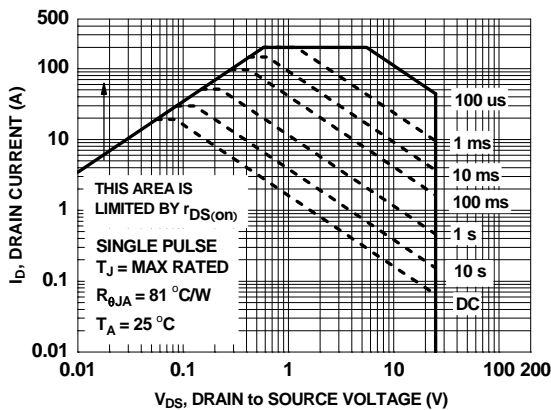
**Figure 8. Capacitance vs Drain to Source Voltage**



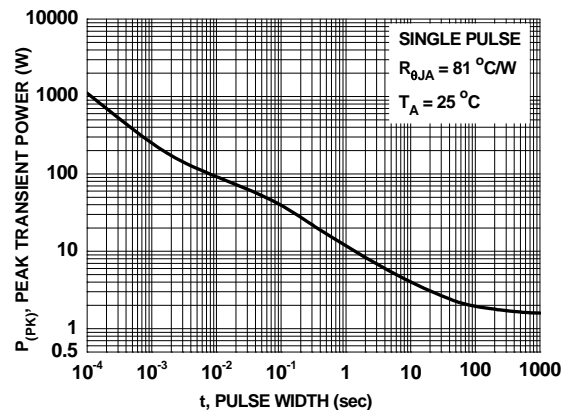
**Figure 9. Unclamped Inductive Switching Capability**



**Figure 10. Maximum Continuous Drain Current vs Case Temperature**

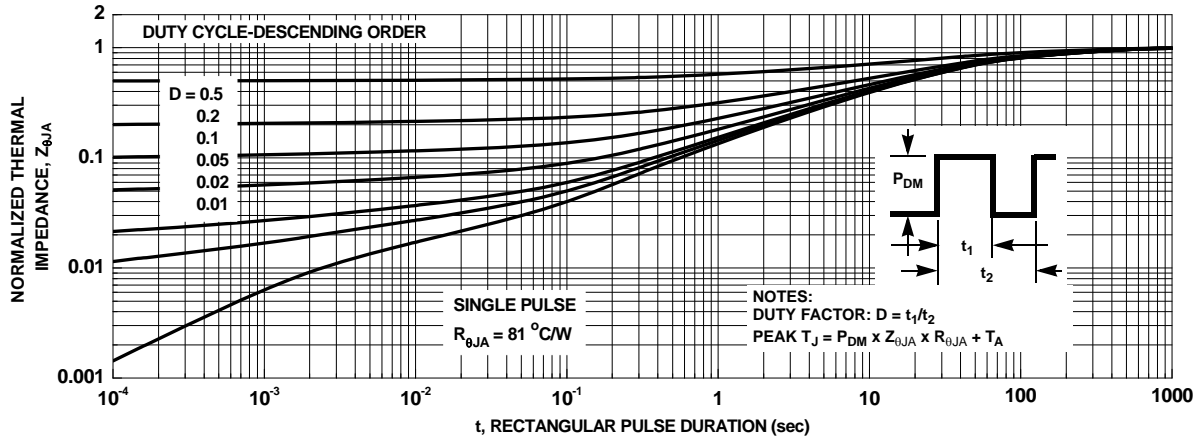


**Figure 11. Forward Bias Safe Operating Area**



**Figure 12. Single Pulse Maximum Power Dissipation**

**Typical Characteristics**  $T_J = 25\text{ }^\circ\text{C}$  unless otherwise noted



**Figure 13. Junction-to-Ambient Transient Thermal Response Curve**

## Typical Characteristics (continued)

### SyncFET Schottky body diode Characteristics

Fairchild's SyncFET process embeds a Schottky diode in parallel with PowerTrench MOSFET. This diode exhibits similar characteristics to a discrete external Schottky diode in parallel with a MOSFET. Figure 14 shows the reverse recovery characteristic of the FDMS2510SDC.

Schottky barrier diodes exhibit significant leakage at high temperature and high reverse voltage. This will increase the power in the device.

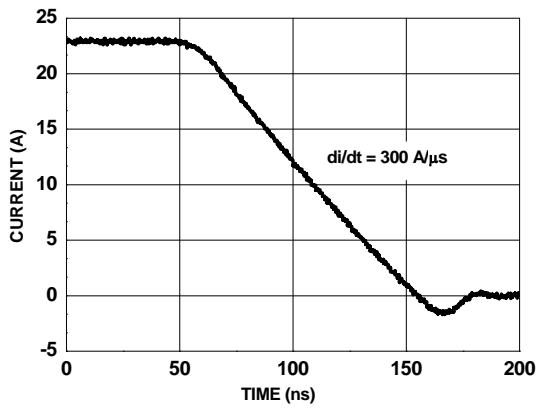


Figure 14. FDMS2510SDC SyncFET body diode reverse recovery characteristic

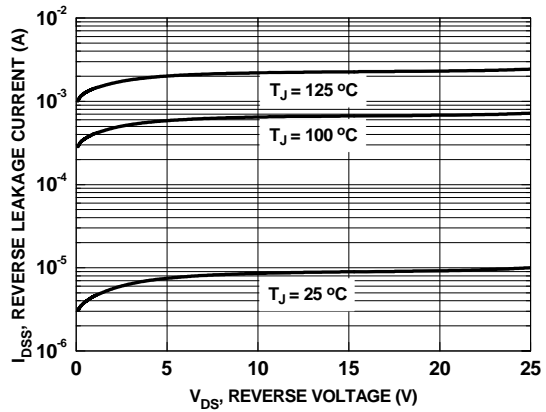
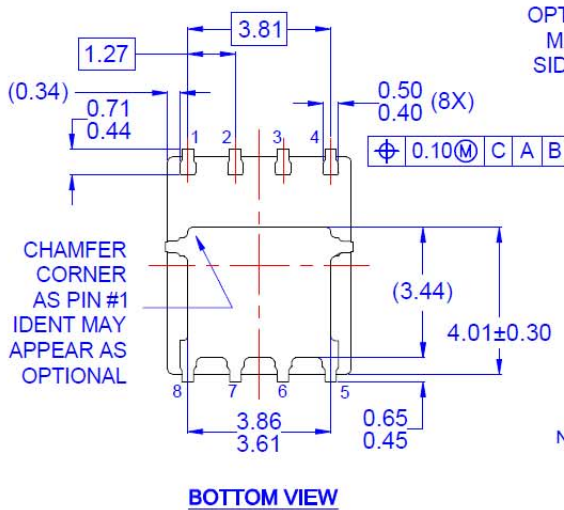
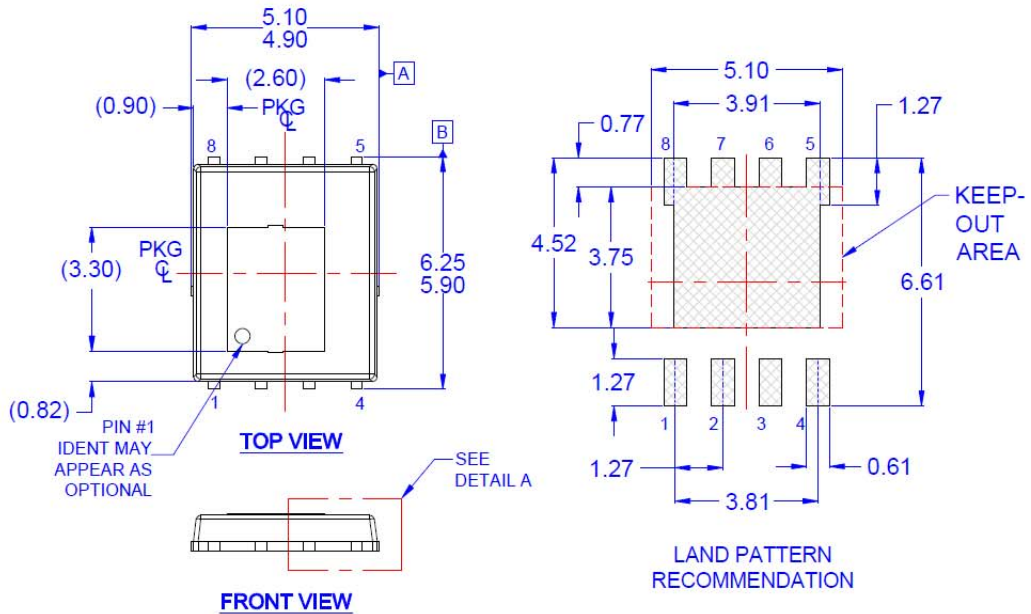
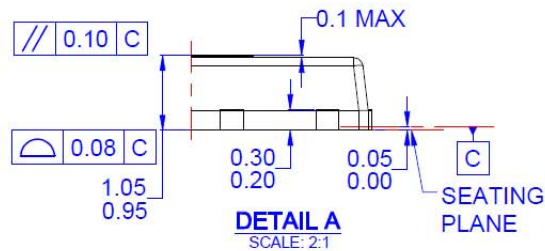
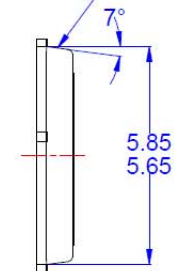


Figure 15. SyncFET body diode reverse leakage versus drain-source voltage

## Dimensional Outline and Pad Layout



OPTIONAL DRAFT ANGLE MAY APPEAR ON FOUR SIDES OF THE PACKAGE



- NOTES: UNLESS OTHERWISE SPECIFIED
- PACKAGE STANDARD REFERENCE: JEDEC MO-240, ISSUE A, VAR. AA, DATED OCTOBER 2002.
  - ALL DIMENSIONS ARE IN MILLIMETERS.
  - DIMENSIONS DO NOT INCLUDE BURRS OR MOLD FLASH. MOLD FLASH OR BURRS DOES NOT EXCEED 0.10MM.
  - DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994.
  - IT IS RECOMMENDED TO HAVE NO TRACES OR VIAS WITHIN THE KEEP OUT AREA.





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| BitSiC™                  | Global Power Resource <sup>SM</sup>             | QFET®                                 | TinyBoost™       |
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| <b>F</b> ®               | MicroPak™                                       | SuperSOT™-3                           | <b>SarDes</b> ™  |
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| FACT Quiet Series™       | MotionMax™                                      | SupreMOS®                             | UniFET™          |
| FACT®                    | mWSaver™  | SyncFET™                              | VCX™             |
| FAST®                    | OptoHiT™  |                                       | VisualMax™       |
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**Definition of Terms**

Datasheet Identification	Product Status	Definition
Advance Information	Formative / In Design	Datasheet contains the design specifications for product development. Specifications may change in any manner without notice.
Preliminary	First Production	Datasheet contains preliminary data; supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve design.
No Identification Needed	Full Production	Datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve the design.
Obsolete	Not In Production	Datasheet contains specifications on a product that is discontinued by Fairchild Semiconductor. The datasheet is for reference information only.

Rev. I64

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