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February 2007

## **FDMS3572**

## N-Channel UltraFET Trench® MOSFET

**80V**, **22A**, **16.5m** $\Omega$ 

#### **Features**

- Max  $r_{DS(on)}$  = 16.5m $\Omega$  at  $V_{GS}$  = 10V,  $I_D$  = 8.8A
- Max  $r_{DS(on)}$  = 24m $\Omega$  at  $V_{GS}$  = 6V,  $I_D$  = 8.4A
- Typ Qg = 28nC at V<sub>GS</sub> = 10V
- Low Miller Charge
- Optimized efficiency at high frequencies
- RoHS Compliant

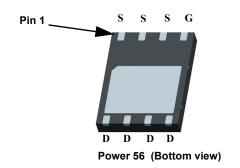


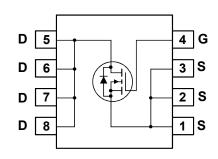
## **General Description**

UltraFET devices combine characteristics that enable benchmark efficiency in power conversion applications. Optimized for  $r_{DS(on)}$ , low ESR, low total and Miller gate charge, these devices are ideal for high frequency DC to DC converters.

## **Application**

■ DC - DC Conversion





## MOSFET Maximum Ratings T<sub>A</sub> = 25°C unless otherwise noted

Symbol	Parameter	Parameter			Units
V <sub>DS</sub>	Drain to Source Voltage			80	V
V <sub>GS</sub>	Gate to Source Voltage			±20	V
I <sub>D</sub>	Drain Current -Continuous (Package limited)	T <sub>C</sub> = 25°C		22	
	-Continuous (Silicon limited)	T <sub>C</sub> = 25°C		48	_
	-Continuous	T <sub>A</sub> = 25°C	(Note 1a)	8.8	Α
	-Pulsed			50	
D	Power Dissipation	T <sub>C</sub> = 25°C		78	W
$P_D$	Power Dissipation	T <sub>A</sub> = 25°C	(Note 1a)	2.5	VV
T <sub>J</sub> , T <sub>STG</sub>	Operating and Storage Junction Temperature R	lange		-55 to +150	°C

#### **Thermal Characteristics**

$R_{\theta JC}$	Thermal Resistance, Junction to Case	1.6	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1a)	50	C/VV

### **Package Marking and Ordering Information**

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
FDMS3572	FDMS3572	Power 56	13"	12mm	3000 units

## **Electrical Characteristics** $T_J = 25$ °C unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Тур	Max	Units	
Off Characteristics							
$BV_{DSS}$	Drain to Source Breakdown Voltage	$I_D = 250 \mu A, V_{GS} = 0 V$	80			V	
$\frac{\Delta BV_{DSS}}{\Delta T_{J}}$	Breakdown Voltage Temperature Coefficient	I <sub>D</sub> = 250μA, referenced to 25°C		76		mV/°C	
I <sub>DSS</sub>	Zero Gate Voltage Drain Current	$V_{DS} = 64V, V_{GS} = 0V$			1	μΑ	
I <sub>GSS</sub>	Gate to Source Leakage Current	$V_{GS} = \pm 20V, V_{DS} = 0V$			±100	nA	

#### On Characteristics

V <sub>GS(th)</sub>	Gate to Source Threshold Voltage	$V_{GS} = V_{DS}, I_{D} = 250 \mu A$	2	3.2	4	V	
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate to Source Threshold Voltage Temperature Coefficient	I <sub>D</sub> = 250μA, referenced to 25°C		-11		mV/°C	
	Drain to Source On Resistance	V <sub>GS</sub> = 10V, I <sub>D</sub> = 8.8A		13.5	16.5	16.5	
r <sub>DS(on)</sub>		$V_{GS} = 6V, I_D = 8.4A$		18.3	24	mΩ	
		$V_{GS} = 10V$ , $I_D = 8.8A$ , $T_J = 125$ °C		22.2	29		
g <sub>FS</sub>	Forward Transconductance	$V_{DS} = 10V, I_{D} = 8.8A$		23		S	

## **Dynamic Characteristics**

C <sub>iss</sub>	Input Capacitance	\\ - 40\\ \\ - 0\\	1870	2490	pF
C <sub>oss</sub>	Output Capacitance	V <sub>DS</sub> = 40V, V <sub>GS</sub> = 0V, f = 1MHz	275	365	pF
C <sub>rss</sub>	Reverse Transfer Capacitance	1 - 1141112	78	120	pF
$R_g$	Gate Resistance	f = 1MHz	1.3		Ω

## **Switching Characteristics**

t <sub>d(on)</sub>	Turn-On Delay Time		11	20	ns
t <sub>r</sub>	Rise Time	$V_{DD} = 40V, I_{D} = 8.8A$ $V_{GS} = 10V, R_{GEN} = 6\Omega$	13	24	ns
t <sub>d(off)</sub>	Turn-Off Delay Time	V <sub>GS</sub> - 10V, K <sub>GEN</sub> - 012	24	39	ns
t <sub>f</sub>	Fall Time		12	22	ns
$Q_{g(TOT)}$	Total Gate Charge at 10V	$V_{GS} = 0V \text{ to } 10V$ $V_{DD} = 40V$	28	40	nC
$Q_{gs}$	Gate to Source Gate Charge	I <sub>D</sub> = 8.8A	9		nC
$Q_{gd}$	Gate to Drain "Miller" Charge		8		nC

## **Drain-Source Diode Characteristics**

$V_{SD}$	Source to Drain Diode Forward Voltage	$V_{GS} = 0V, I_S = 8.8A$ (Note 2)		8.0	1.2	V
t <sub>rr</sub>	Reverse Recovery Time	1 - 9 9 A di/dt - 100 A/v.o		43	65	ns
Q <sub>rr</sub>	Reverse Recovery Charge	F = 8.8A, di/dt = 100A/μs		71	107	nC

#### Notes

R<sub>θJA</sub> is determined with the device mounted on a 1in<sup>2</sup> pad 2 oz copper pad on a 1.5 x 1.5 in. board of FR-4 material. R<sub>θJC</sub> is guaranteed by design while R<sub>θCA</sub> is determined by the user's board design.



a.  $50^{\circ}$ C/W when mounted on a 1 in<sup>2</sup> pad of 2 oz copper



b. 125°C/W when mounted on a minimum pad of 2 oz copper

2: Pulse Test: Pulse Width <  $300\mu$ s, Duty cycle < 2.0%.

## Typical Characteristics T<sub>J</sub> = 25°C unless otherwise noted

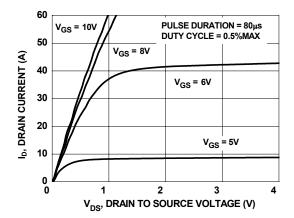


Figure 1. On Region Characteristics

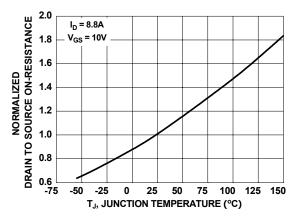


Figure 3. Normalized On Resistance vs Junction Temperature

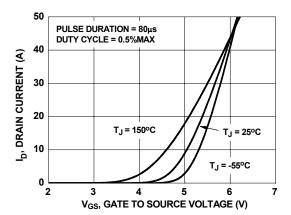


Figure 5. Transfer Characteristics

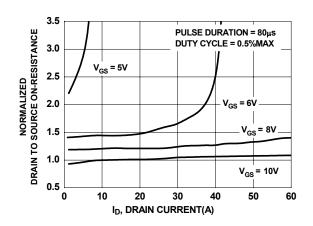


Figure 2. Normalized On-Resistance vs Drain Current and Gate Voltage

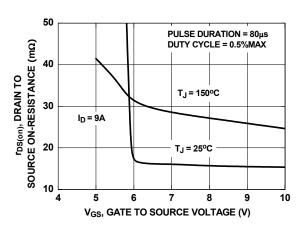


Figure 4. On-Resistance vs Gate to Source Voltage

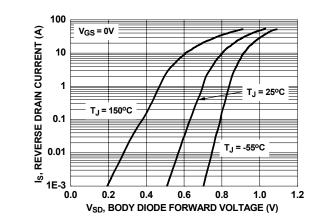


Figure 6. Source to Drain Diode Forward Voltage vs Source Current

## **Typical Characteristics** $T_J = 25^{\circ}C$ unless otherwise noted

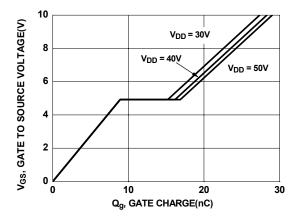


Figure 7. Gate Charge Characteristics

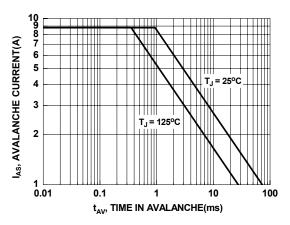


Figure 9. Unclamped Inductive Switching Capability

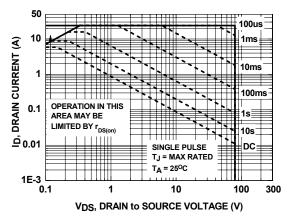


Figure 11. Forward Bias Safe Operating Area

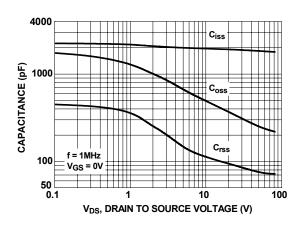


Figure 8. Capacitance vs Drain to Source Voltage

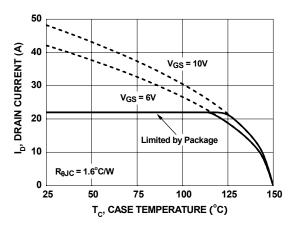


Figure 10. Maximum Continuous Drain Current vs Case Temperature

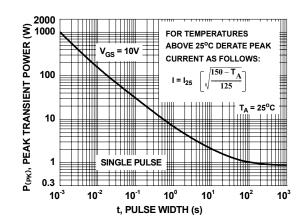


Figure 12. Single Pulse Maximum Power Dissipation

## Typical Characteristics T<sub>J</sub> = 25°C unless otherwise noted

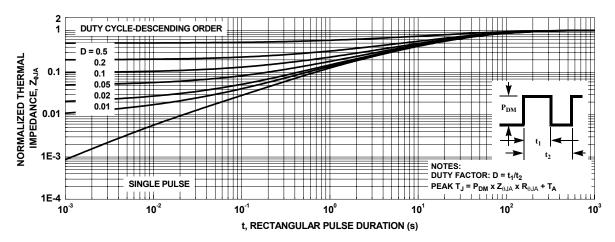
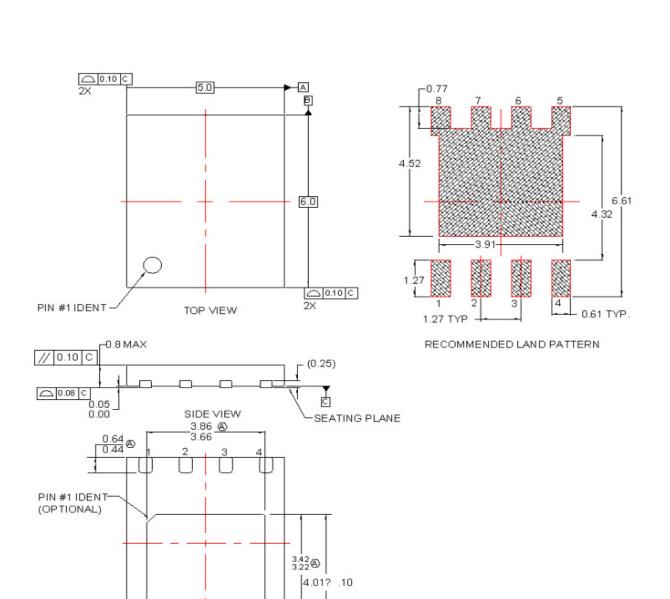


Figure 13. Transient Thermal Response Curve



#### NOTES:

(A) DOES NOT FULLY CONFORM TO JEDEC REGISTRATION, MO-229. DATED 11/2001.

3.81

BOTTOM VIEW

1.27

- B. DIMENSIONS ARE IN MILLIMETERS.
- C. DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994
- D. TERMINALS 5,6,7 AND 8 ARE TIED TO THE EXPOSED PADDLE

## MLP08GrevD

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