MOSFET – N-Channel, DUAL COOL® 56, POWERTRENCH®

30 V, 100 A, 0.99 mΩ

FDMS7650DC

ON Semiconductor®

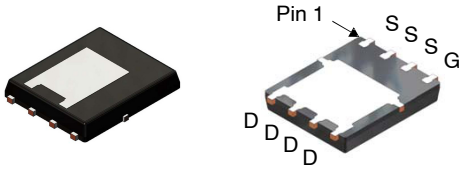
www.onsemi.com

General Description

This N−Channel MOSFET is produced using ON Semiconductor's advanced POWERTRENCH process. Advancements in both silicon and DUAL COOL package technologies have been combined to offer the lowest $r_{DS(on)}$ while maintaining excellent switching performance by extremely low Junction−to−Ambient thermal resistance.

Features

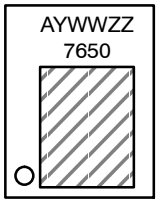
- DUAL COOL Top Side Cooling PQFN package
- Max $r_{DS(on)}$ = 0.99 mΩ at V_{GS} = 10 V, I_D = 36 A
- Max $r_{DS(on)}$ = 1.55 mΩ at V_{GS} = 4.5 V, I_D = 32 A
- High performance technology for extremely low $r_{DS(on)}$
- This Device is Pb−Free and is RoHS Compliant



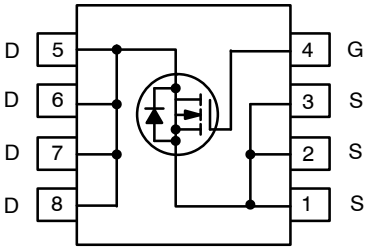
Top Bottom

DFN8 5x6.15, 1.27P,
DUAL COOL 56
CASE 506EG

MARKING DIAGRAM



7650 = Specific Device Code
A = Assembly Location
Y = Year
WW = Work Week
ZZ = Assembly Lot Code



N−Channel MOSFET

ORDERING INFORMATION

See detailed ordering and shipping information on page 7 of this data sheet.

MOSFET MAXIMUM RATINGS (T_A = 25°C unless otherwise specified)

Symbol	Parameter		Rating	Unit
V_{DS}	Drain to Source Voltage		30	V
V_{GS}	Gate to Source Voltage (Note 4)		+20	V
I_D	Drain Current – Continuous (Package limited)	T_C = 25°C	100	A
	– Continuous (Silicon limited)	T_C = 25°C	289	
	– Continuous	T_A = 25 °C (Note 1a)	47	
	– Pulsed		200	
E_{AS}	Single Pulse Avalanche Energy (Note 3)		578	mJ
dv/dt	Peak Diode Recovery dv/dt (Note 5)		0.5	V/ns
P_D	Power Dissipation	T_C = 25°C	125	W
	Power Dissipation	T_A = 25°C (Note 1a)	3.3	
T_J, T_{STG}	Operating and Storage Junction Temperature Range		–55 to +150	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

THERMAL CHARACTERISTICS

Symbol	Parameter	Rating	Unit
$R_{\theta JC}$	Thermal Resistance, Junction to Case (Top Source)	2.3	°C/W
$R_{\theta JC}$	Thermal Resistance, Junction to Case (Bottom Drain)	1	
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1a)	38	
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1b)	81	
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1i)	16	
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1j)	23	
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1k)	11	

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
ON CHARACTERISTICS						
BV_{DSS}	Drain to Source Breakdown Voltage	I_D = 250 μA, V_{GS} = 0 V	30	–	–	V
$\frac{\Delta BV_{DSS}}{\Delta T_j}$	Breakdown Voltage Temperature Coefficient	I_D = 250 μA, referenced to 25°C	–	12	–	mV/°C
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 24 V, V_{GS} = 0 V	–	–	1	μA
I_{GSS}	Gate to Source Leakage Current, Forward	V_{GS} = 20 V, V_{DS} = 0 V	–	–	100	nA
ON CHARACTERISTICS						
$V_{GS(th)}$	Gate to Source Threshold Voltage	V_{GS} = V_{DS}, I_D = 250 μA	1.1	1.9	2.7	V
$\frac{\Delta V_{GS(th)}}{\Delta T_j}$	Gate to Source Threshold Voltage Temperature Coefficient	I_D = 250 μA, referenced to 25°C	–	–7	–	mV/°C
$r_{DS(on)}$	Static Drain to Source On Resistance	V_{GS} = 10 V, I_D = 36 A	–	0.6	0.99	mΩ
		V_{GS} = 4.5 V, I_D = 32 A	–	1	1.55	
		V_{GS} = 10 V, I_D = 36 A, T_J = 125°C	–	0.9	1.5	
g_{FS}	Forward Transconductance	V_{DS} = 5 V, I_D = 36 A	–	225	–	S
DYNAMIC CHARACTERISTICS						
C_{iss}	Input Capacitance	V_{DS} = 15 V, V_{GS} = 0 V, f = 1 MHz	–	11100	14765	pF
C_{oss}	Output Capacitance		–	3440	4575	pF
C_{rss}	Reverse Transfer Capacitance		–	205	310	pF
R_g	Gate Resistance		–	1.3	–	Ω
SWITCHING CHARACTERISTICS						
$t_{d(on)}$	Turn–On Delay Time	V_{DD} = 15 V, I_D = 36 A, V_{GS} = 10 V, R_{GEN} = 6 Ω	–	29	46	ns
t_r	Rise Time		–	28	45	ns
$t_{d(off)}$	Turn–Off Delay Time		–	81	130	ns
t_f	Fall Time		–	20	32	ns
Q_g	Total Gate Charge	V_{GS} = 0 V to 10 V; V_{DD} = 15 V, I_D = 36 A	–	147	206	nC
Q_g	Total Gate Charge	V_{GS} = 0 V to 4.5 V; V_{DD} = 15 V, I_D = 36 A	–	62	87	nC
Q_{gs}	Gate to Source Charge	V_{DD} = 15 V, I_D = 36 A	–	38	–	nC
Q_{gd}	Gate to Drain “Miller” Charge		–	9.7	–	nC
DRAIN–SOURCE DIODE CHARACTERISTICS						
V_{SD}	Source to Drain Diode Forward Voltage	V_{GS} = 0 V, I_S = 2.1 A (Note 2)	–	0.7	1.2	V
		V_{GS} = 0 V, I_S = 36 A (Note 2)	–	0.8	1.3	
t_{rr}	Reverse Recovery Time	I_F = 36 A, di/dt = 100 A/μs	–	75	120	ns
Q_{rr}	Reverse Recovery Charge		–	61	98	nC

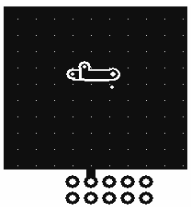
Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

THERMAL CHARACTERISTICS

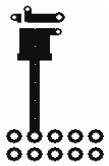
Symbol	Parameter	Rating	Unit
$R_{\theta JC}$	Thermal Resistance, Junction to Case (Top Source)	2.3	°C/W
$R_{\theta JC}$	Thermal Resistance, Junction to Case (Bottom Drain)	1	
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1a)	38	
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1b)	81	
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1c)	27	
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1d)	34	
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1e)	16	
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1f)	19	
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1g)	26	
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1h)	61	
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1i)	16	
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1j)	23	
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1k)	11	
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1l)	13	

NOTES:

1. $R_{\theta JA}$ is determined with the device mounted on a FR−4 board using a specified pad of 2 oz copper as shown below. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.



a. 38°C/W when mounted on a 1 in^2 pad of 2 oz copper



b. 0°C/W when mounted on a minimum pad of 2 oz copper

c. Still air, 20.9 x 10.4 x 12.7 mm Aluminum Heat Sink, 1 in^2 pad of 2 oz copper
d. Still air, 20.9 x 10.4 x 12.7 mm Aluminum Heat Sink, minimum pad of 2 oz copper
e. Still air, 45.2 x 41.4 x 11.7 mm Aavid Thermalloy Part # 10−L41B−11 Heat Sink, 1 in^2 pad of 2 oz copper
f. Still air, 45.2 x 41.4 x 11.7 mm Aavid Thermalloy Part # 10−L41B−11 Heat Sink, minimum pad of 2 oz copper
g. 200FPM Airflow, No Heat Sink,1 in^2 pad of 2 oz copper
h. 200FPM Airflow, No Heat Sink, minimum pad of 2 oz copper
i. 200FPM Airflow, 20.9 x 10.4 x 12.7 mm Aluminum Heat Sink, 1 in^2 pad of 2 oz copper
j. 200FPM Airflow, 20.9 x 10.4 x 12.7 mm Aluminum Heat Sink, minimum pad of 2 oz copper
k. 200FPM Airflow, 45.2 x 41.4 x 11.7 mm Aavid Thermalloy Part # 10−L41B−11 Heat Sink, 1 in^2 pad of 2 oz copper
l. 200FPM Airflow, 45.2 x 41.4 x 11.7 mm Aavid Thermalloy Part # 10−L41B−11 Heat Sink, minimum pad of 2 oz copper

2. Pulse Test: Pulse Width < 300 μs, Duty cycle < 2.0%.
3. E_{AS} of 578 mJ is based on starting T_J = 25°C; N−ch: L = 1 mH, I_{AS} = 34 A, V_{DD} = 27 V, V_{GS} = 10 V.
4. As an N−ch device, the negative Vgs rating is for low duty cycle pulse ocurrence only. No continuous rating is implied.
5. $I_{SD} \leq$ 3 36 A, di/dt 3 100 A/μs, $V_{DD} \leq BV_{DSS}$, Starting T_J = 25°C.

TYPICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

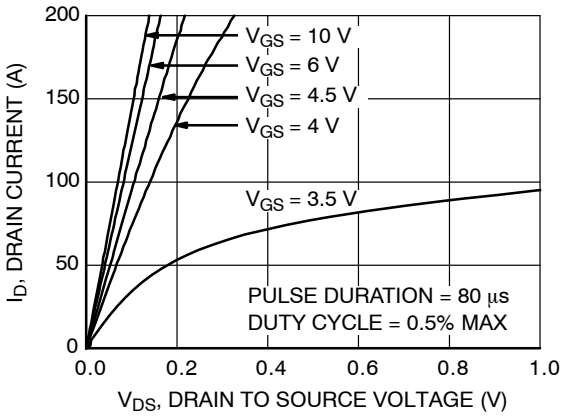


Figure 1. On Region Characteristics

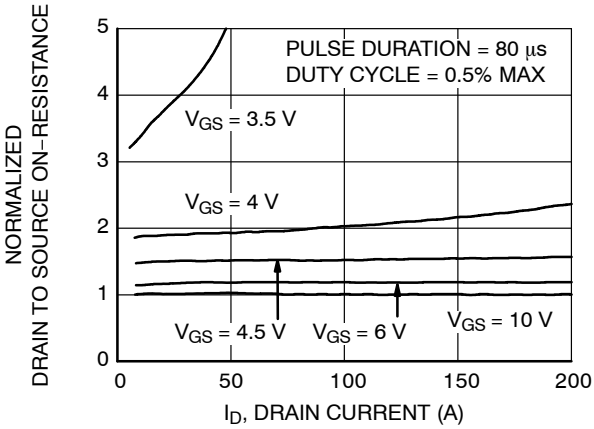


Figure 2. Normalized On−Resistance vs. Drain Current and Gate Voltage

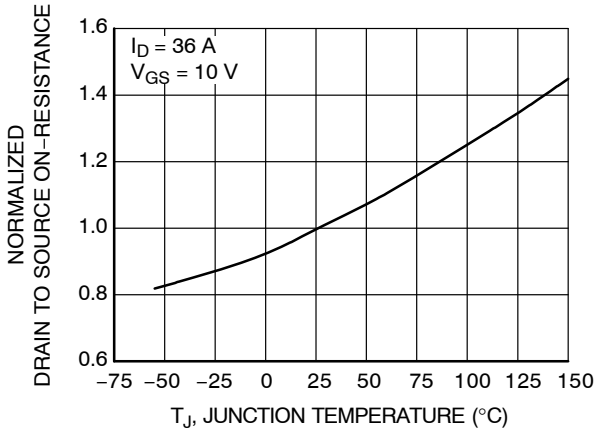


Figure 3. Normalized On Resistance vs. Junction Temperature

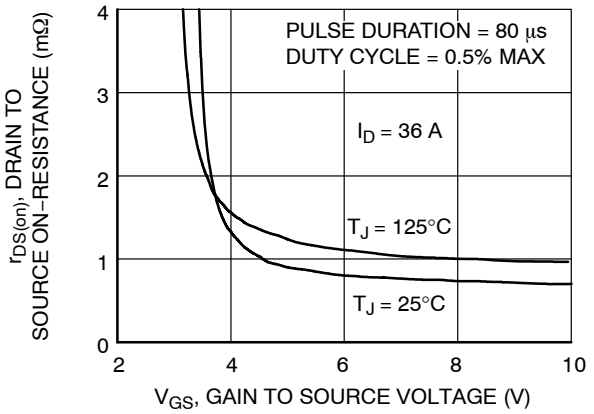


Figure 4. On−Resistance vs. Gate to Source Voltage

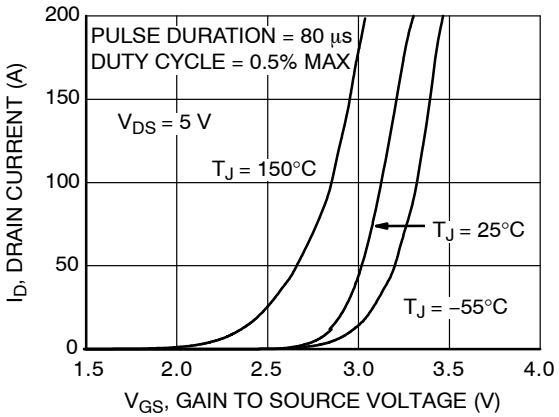


Figure 5. Transfer Characteristics

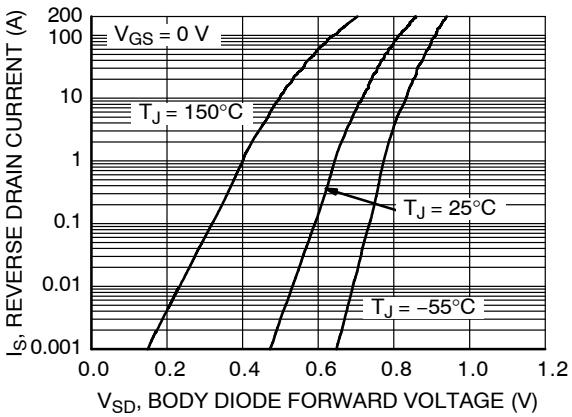


Figure 6. Source to Drain Diode Voltage vs. Source Current

TYPICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

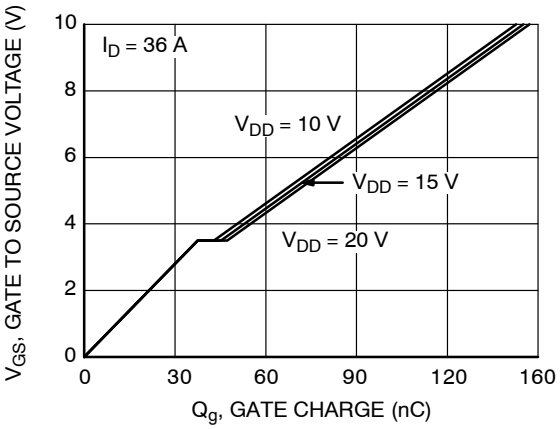


Figure 7. Gate Charge Characteristics

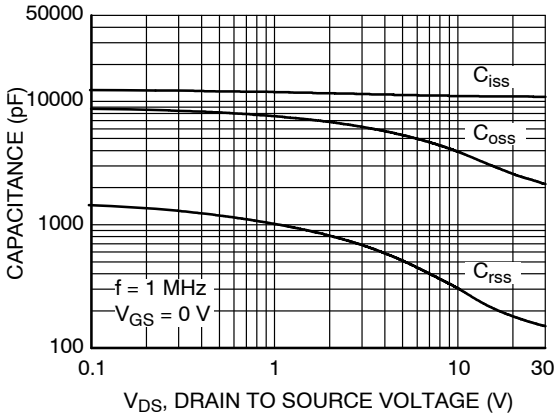


Figure 8. Capacitance vs. Drain to Source Voltage

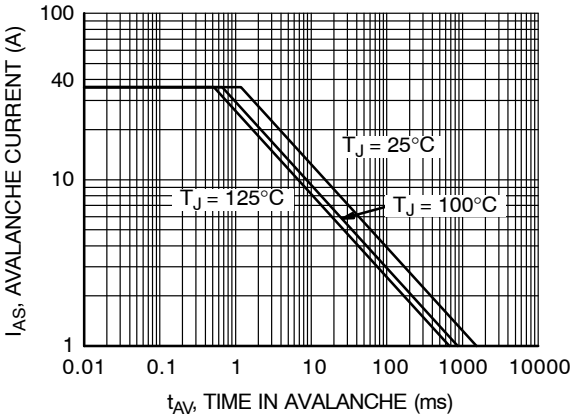


Figure 9. Unclamped Inductive Switching Capability

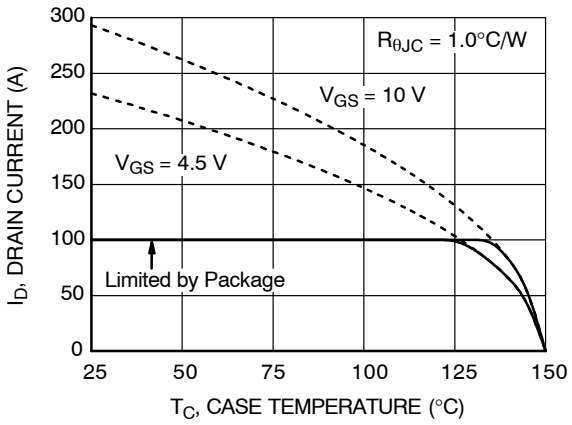


Figure 10. Maximum Continuous Drain Current vs. Case Temperature

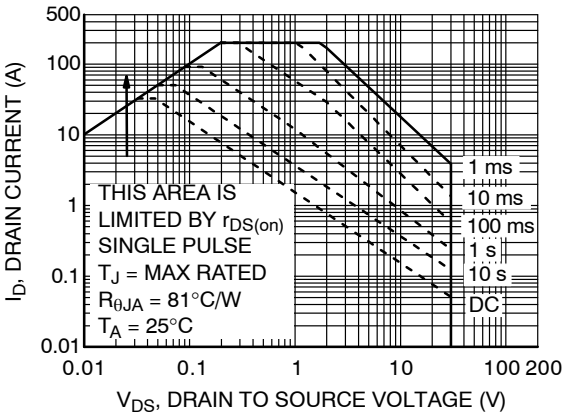


Figure 11. Forward Bias Safe Operating Area

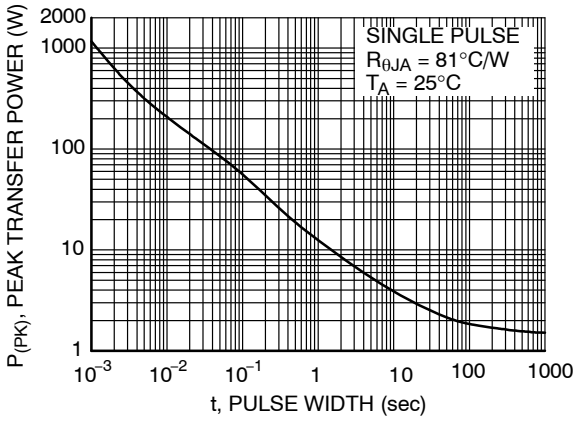


Figure 12. Single Pulse Maximum Power Dissipation

TYPICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

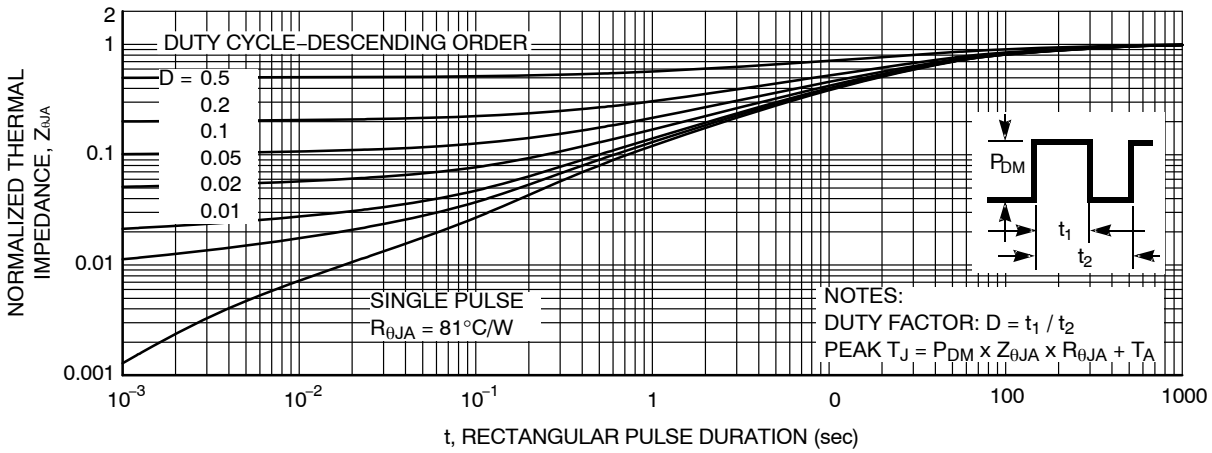


Figure 13. Junction−to−Ambient Transient Thermal Response Curve

ORDERING INFORMATION

Device	Device Marking	Package	Reel Size	Tape Width	Shipping†
FDMS7650DC	7650	DFN8 5x6.15, 1.27P, DUAL COOL 56 (Pb−Free)	13”	12 mm	3000 / Tape & Reel

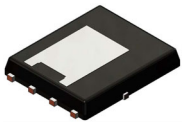
†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

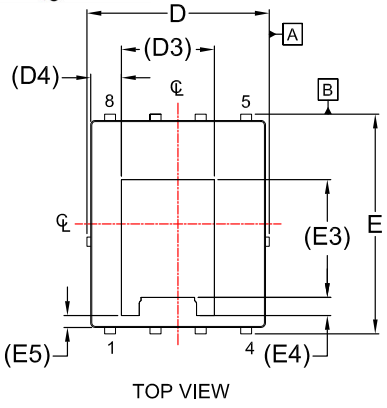
MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

ON Semiconductor®

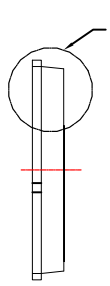
DFN8 5x6.15, 1.27P, DUAL COOL
CASE 506EG
ISSUE D

DATE 25 AUG 2020

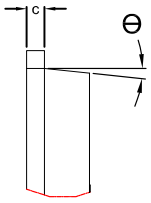




TOP VIEW



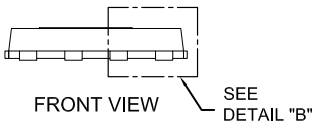
SIDE VIEW



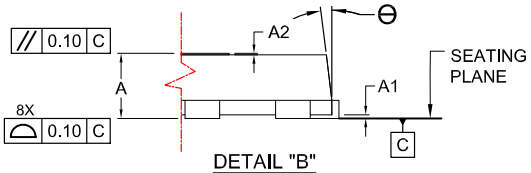
DETAIL "A"
SCALE: 2:1

NOTES:

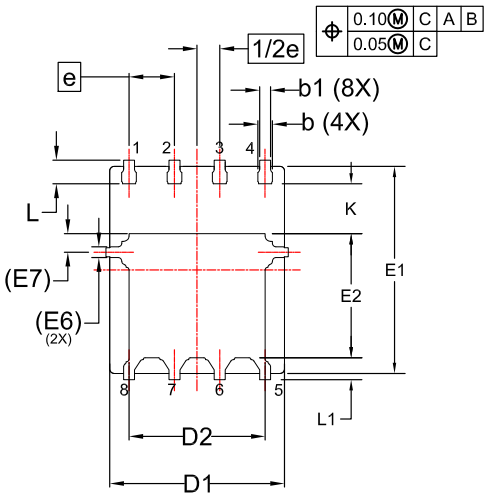
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2009.
2. CONTROLLING DIMENSION: MILLIMETERS
3. COPLANARITY APPLIES TO THE EXPOSED PADS AS WELL AS THE TERMINALS.
4. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.
5. SEATING PLANE IS DEFINED BY THE TERMINALS. "A1" IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT ON THE PACKAGE BODY.



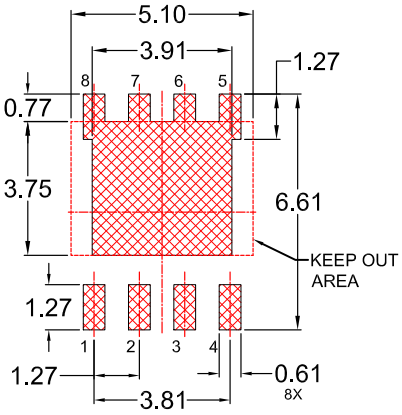
FRONT VIEW



DETAIL "B"
SCALE: 2:1



BOTTOM VIEW

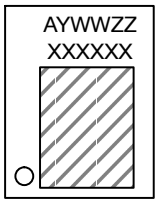


LAND PATTERN
RECOMMENDATION

*FOR ADDITIONAL INFORMATION ON OUR PB-FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ON SEMICONDUCTOR SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERRM/D.

DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	0.85	0.90	0.95
A1	-	-	0.05
A2	-	-	0.05
b	0.31	0.41	0.51
b1	0.21	0.31	0.41
c	0.20	0.25	0.30
D	4.90	5.00	5.10
D1	4.80	4.90	5.00
D2	3.67	3.82	3.97
D3	2.60 REF		
D4	0.86 REF		
E	6.05	6.15	6.25
E1	5.70	5.80	5.90
E2	3.38	3.48	3.58
E3	3.30 REF		
E4	0.50 REF		
E5	0.34 REF		
E6	0.30 REF		
E7	0.52 REF		
e	1.27 BSC		
1/2e	0.635 BSC		
K	1.30	1.40	1.50
L	0.56	0.66	0.76
L1	0.52	0.62	0.72
Θ	0°	---	12°

GENERIC MARKING DIAGRAM*



XXXX = Specific Device Code
A = Assembly Location
Y = Year
WW = Work Week
ZZ = Assembly Lot Code

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

DOCUMENT NUMBER:	**98AON84257G**	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.
DESCRIPTION:	**DFN8 5x6.15, 1.27P, DUAL COOL**	**PAGE 1 OF 1**

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:
Email Requests to: orderlit@onsemi.com

onsemi Website: www.onsemi.com

TECHNICAL SUPPORT
North American Technical Support:
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Phone: 011 421 33 790 2910

Europe, Middle East and Africa Technical Support:
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