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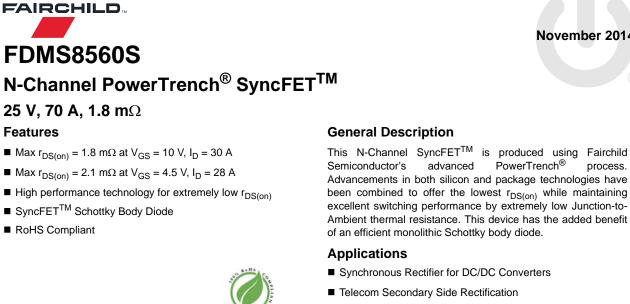


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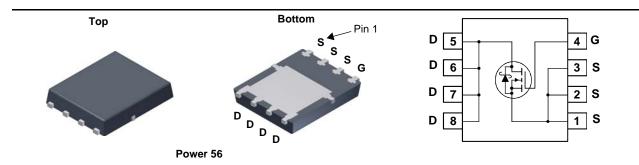
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■ High End Server/Workstation Vcore Low Side



# **MOSFET Maximum Ratings** $T_A = 25^{\circ}C$ unless otherwise noted

Symbol	Parameter			Ratings	Units	
V <sub>DS</sub>	Drain to Source Voltage		25	V		
V <sub>GS</sub>	Gate to Source Voltage			12	V	
	Drain Current -Continuous (Package limited)	T <sub>C</sub> = 25 °C		70		
I <sub>D</sub>	-Continuous	T <sub>A</sub> = 25 °C	(Note 1a)	30	Α	
	-Pulsed			150		
E <sub>AS</sub>	Single Pulse Avalanche Energy		(Note 3)	79	mJ	
D	Power Dissipation	T <sub>C</sub> = 25 °C		65	14/	
PD	Power Dissipation	T <sub>A</sub> = 25 °C	(Note 1a)	2.5	W	
T <sub>J</sub> , T <sub>STG</sub>	Operating and Storage Junction Temperature Range			-55 to +150	°C	

### **Thermal Characteristics**

Features

$R_{ ext{ heta}JC}$	Thermal Resistance, Junction to Case	T <sub>C</sub> = 25 °C		1.9	°C/W
$R_{\thetaJA}$	Thermal Resistance, Junction to Ambient	T <sub>A</sub> = 25 °C	(Note 1a)	50	0/11

### Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
05OD	FDMS8560S	Power 56	13"	12 mm	3000 units

November 2014

process.

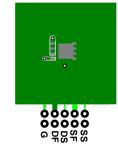
Symbol	Parameter	Test Conditions	Min	Тур	Max	Units	
Off Chara	octeristics						
BV <sub>DSS</sub>	Drain to Source Breakdown Voltage	I <sub>D</sub> = 1 mA, V <sub>GS</sub> = 0 V	25			V	
ΔBV <sub>DSS</sub> 	Breakdown Voltage Temperature Coefficient	$I_D = 10$ mA, referenced to 25 °C		20		mV/°C	
I <sub>DSS</sub>	Zero Gate Voltage Drain Current	V <sub>DS</sub> = 20 V, V <sub>GS</sub> = 0 V			500	μΑ	
I <sub>GSS</sub>	Gate to Source Leakage Current	$V_{GS}$ = +12 V/-8 V, $V_{DS}$ = 0 V			±100	nA	
On Chara	cteristics						
V <sub>GS(th)</sub>	Gate to Source Threshold Voltage	$V_{GS} = V_{DS}, I_D = 1 \text{ mA}$	1.1	1.4	2.2	V	
$\Delta V_{GS(th)}$ $\Delta T_J$	Gate to Source Threshold Voltage Temperature Coefficient	I <sub>D</sub> = 10 mA, referenced to 25 °C		-3		mV/°C	
	Static Drain to Source On Resistance	V <sub>GS</sub> = 10 V, I <sub>D</sub> = 30 A		1.4	1.8	mΩ	
r <sub>DS(on)</sub>		$V_{GS} = 4.5 \text{ V}, \text{ I}_{D} = 28 \text{ A}$		1.6	2.1		
		$V_{GS}$ = 10 V, $I_{D}$ = 30 A, $T_{J}$ = 125 °C		2.1	2.8		
9 <sub>FS</sub>	Forward Transconductance	V <sub>DS</sub> = 5 V, I <sub>D</sub> = 30 A		304		S	
C <sub>iss</sub>	Characteristics Input Capacitance	V <sub>DS</sub> = 13 V, V <sub>GS</sub> = 0 V,		4350		pF	
C <sub>oss</sub>	Output Capacitance	$v_{DS} = 13 v, v_{GS} = 0 v,$ 		1270		pF	
C <sub>rss</sub>	Reverse Transfer Capacitance			138		pF	
R <sub>g</sub>	Gate Resistance			0.8		Ω	
Switching	g Characteristics						
Switching t <sub>d(on)</sub>	Turn-On Delay Time			13		ns	
		V <sub>DD</sub> = 13 V, I <sub>D</sub> = 30 A,		13 6		ns ns	
t <sub>d(on)</sub>	Turn-On Delay Time	V <sub>DD</sub> = 13 V, I <sub>D</sub> = 30 A, V <sub>GS</sub> = 10 V, R <sub>GEN</sub> = 6 Ω					
t <sub>d(on)</sub> t <sub>r</sub>	Turn-On Delay Time Rise Time			6		ns	
t <sub>d(on)</sub> t <sub>r</sub> t <sub>d(off)</sub>	Turn-On Delay Time Rise Time Turn-Off Delay Time	$V_{GS} = 10 \text{ V}, \text{ R}_{GEN} = 6 \Omega$ $V_{GS} = 0 \text{ V to } 10 \text{ V}$		6 45		ns ns	
t <sub>d(on)</sub> t <sub>r</sub> t <sub>d(off)</sub> t <sub>f</sub>	Turn-On Delay Time Rise Time Turn-Off Delay Time Fall Time	$V_{GS} = 10 \text{ V}, \text{ R}_{GEN} = 6 \Omega$ $V_{GS} = 0 \text{ V to } 10 \text{ V}$ $V_{GS} = 0 \text{ V to } 4.5 \text{ V} \text{ V}_{DD} = 13 \text{ V},$		6 45 5		ns ns ns	
t <sub>d(on)</sub> t <sub>r</sub> t <sub>d(off)</sub> t <sub>f</sub> Q <sub>g</sub>	Turn-On Delay Time         Rise Time         Turn-Off Delay Time         Fall Time         Total Gate Charge	$V_{GS} = 10 \text{ V}, \text{ R}_{GEN} = 6 \Omega$		6 45 5 68		ns ns ns nC	
t <sub>d(on)</sub> t <sub>r</sub> t <sub>d(off)</sub> t <sub>f</sub> Q <sub>g</sub> Q <sub>g</sub> Q <sub>gs</sub>	Turn-On Delay Time         Rise Time         Turn-Off Delay Time         Fall Time         Total Gate Charge         Total Gate Charge	$V_{GS} = 10 \text{ V}, \text{ R}_{GEN} = 6 \Omega$ $V_{GS} = 0 \text{ V to } 10 \text{ V}$ $V_{GS} = 0 \text{ V to } 4.5 \text{ V} \text{ V}_{DD} = 13 \text{ V},$		6 45 5 68 32		ns ns ns nC nC	
t <sub>d(on)</sub> t <sub>r</sub> t <sub>d(off)</sub> t <sub>f</sub> Q <sub>g</sub> Q <sub>g</sub> Q <sub>gs</sub> Q <sub>gd</sub>	Turn-On Delay Time         Rise Time         Turn-Off Delay Time         Fall Time         Total Gate Charge         Total Gate Charge         Gate to Source Gate Charge	$V_{GS} = 10 \text{ V}, \text{ R}_{GEN} = 6 \Omega$ $V_{GS} = 0 \text{ V to } 10 \text{ V}$ $V_{GS} = 0 \text{ V to } 4.5 \text{ V} \text{ V}_{DD} = 13 \text{ V},$		6 45 5 68 32 8.2		ns ns nC nC nC	
t <sub>d(on)</sub> t <sub>r</sub> t <sub>d(off)</sub> t <sub>f</sub> Q <sub>g</sub> Q <sub>g</sub> Q <sub>gs</sub> Q <sub>gd</sub>	Turn-On Delay Time         Rise Time         Turn-Off Delay Time         Fall Time         Total Gate Charge         Total Gate Charge         Gate to Source Gate Charge         Gate to Drain "Miller" Charge	$V_{GS} = 10 \text{ V}, \text{ R}_{GEN} = 6 \Omega$ $V_{GS} = 0 \text{ V to } 10 \text{ V}$ $V_{GS} = 0 \text{ V to } 4.5 \text{ V} \text{ V}_{DD} = 13 \text{ V},$		6 45 5 68 32 8.2	0.8	ns ns nC nC nC	

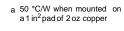
ain-Source Diode Characteristics							
SD	Source to Drain Diode Forward Voltage	$V_{GS} = 0 V, I_S = 2 A$ (Note 2)	0.6	0.8	V		
		$V_{GS} = 0 V, I_S = 30 A$ (Note 2)	0.8	1.2			
	Reverse Recovery Time	I <sub>E</sub> = 30 A, di/dt = 300 A/μs	32		ns		
<b>r</b>	Reverse Recovery Charge	$F = 30 \text{ A}, \text{ u/ul} = 300 \text{ A/} \mu \text{s}$	41		nC		

Q<sub>rr</sub> NOTES:

t<sub>rr</sub>

1. R<sub>0JA</sub> is determined with the device mounted on a FR-4 board using a specified pad of 2 oz copper as shown below. R<sub>0JC</sub> is guaranteed by design while R<sub>0CA</sub> is determined by the user's board design.







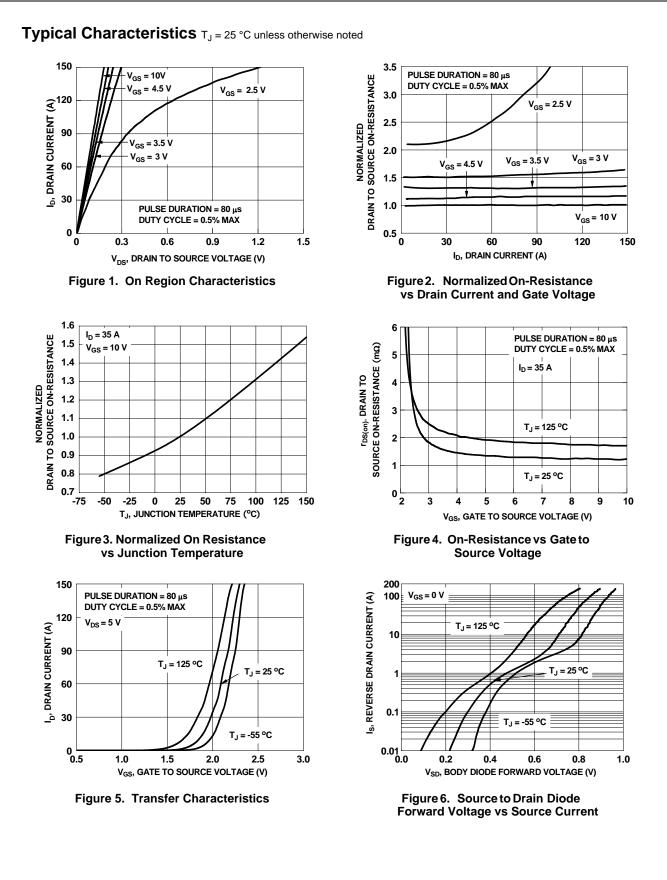
b 125 °C/W when mounted on a minimum pad of 2 oz copper.

3.  $E_{AS}$  of 79 mJ is based on starting  $T_J$  = 25 °C, L = 2.5 mH,  $I_{AS}$  = 8 A,  $V_{DD}$  = 23 V,  $V_{GS}$  = 10 V. 100% test at L = 0.1 mH,  $I_{AS}$  = 33.7 A.

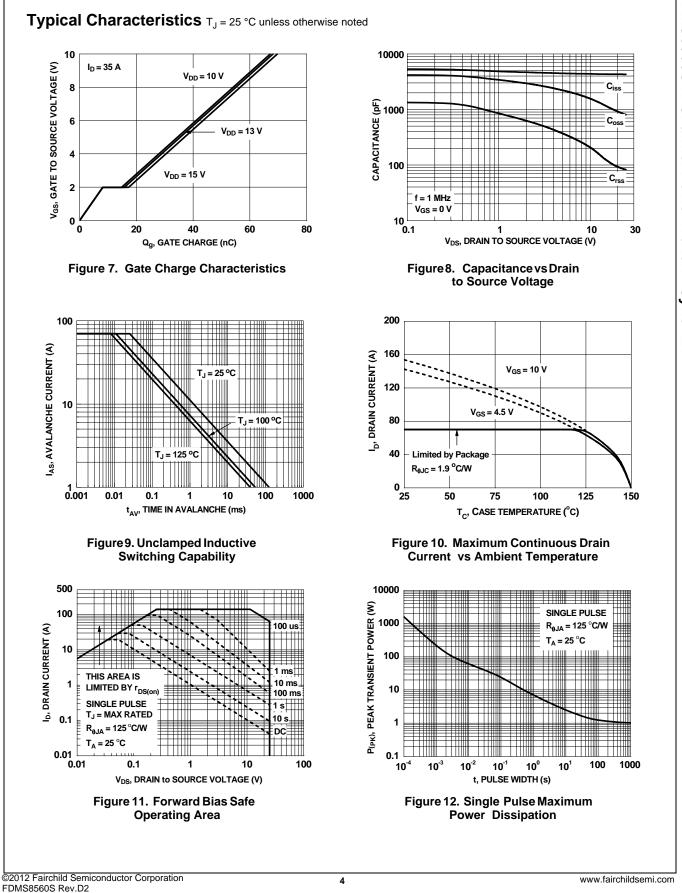
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FDMS8560S N-Channel PowerTrench<sup>®</sup> SyncFET<sup>TM</sup>

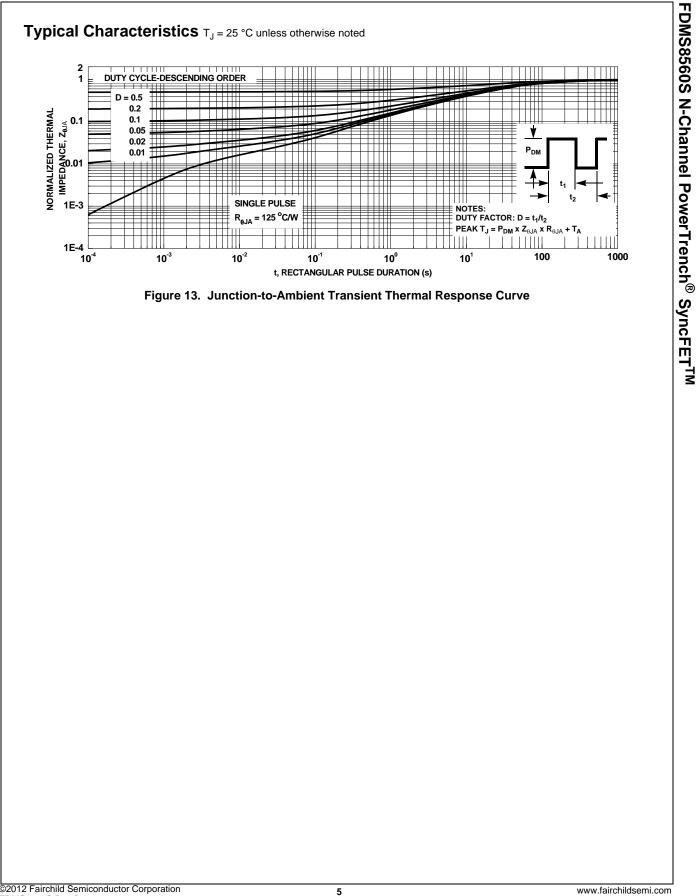
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FDMS8560S N-Channel PowerTrench<sup>®</sup> SyncFET<sup>TM</sup>



# FDMS8560S N-Channel PowerTrench<sup>®</sup> SyncFET<sup>TM</sup>

### Typical Characteristics (continued)

## SyncFET<sup>™</sup> Schottky body diode Characteristics

Fairchild's SyncFET<sup>TM</sup> process embeds a Schottky diode in parallel with PowerTrench MOSFET. This diode exhibits similar characteristics to a discrete external Schottky diode in parallel with a MOSFET. Figure 14 shows the reverse recovery characteristic of the FDMS8560S.

Schottky barrier diodes exhibit significant leakage at high temperature and high reverse voltage. This will increase the power in the device.

T<sub>.1</sub> = 125 °C

T<sub>J</sub> = 100 °C

T<sub>J</sub> = 25 °C

15

20

25

10<sup>-2</sup>

10<sup>-3</sup>

**10**<sup>-4</sup>

10<sup>-5</sup>

10<sup>-6</sup>

0

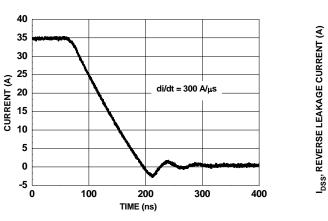


Figure 14. FDMS8560S SyncFET<sup>TM</sup> body diode reverse recovery characteristic

# Figure 15. SyncFET<sup>™</sup> body diode reverse

V<sub>DS</sub>, REVERSE VOLTAGE (V)

10

5

leakage versus drain-source voltage



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