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October 2014

FDMS86263P

P-Channel PowerTrench® MOSFET

-150 V, -22 A, 53 mΩ

Features

- Max $r_{DS(on)}$ = 53 m Ω at V_{GS} = -10 V, I_D = -4.4 A
- Max $r_{DS(on)} = 64 \text{ m}\Omega$ at $V_{GS} = -6 \text{ V}$, $I_D = -4 \text{ A}$
- Very low Rds-on in Mid-Voltage P-Channel silicon technology optimized for low Qg
- This product is optimised for fast switching applications as well as load switch applications
- 100% UIL tested
- RoHS Compliant

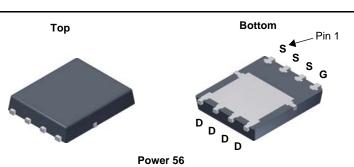
General Description

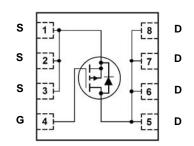
This P-Channel MOSFET is produced using Fairchild Semiconductor's advanced PowerTrench® technology. This very high density process is especially tailored to minimize on-state resistance and optimized for superior switching performance.

Applications

- Active Clamp Switch
- Load Switch







MOSFET Maximum Ratings T_A = 25 °C unless otherwise noted

Symbol	Parame	eter		Ratings	Units
V_{DS}	Drain to Source Voltage			-150	V
V_{GS}	Gate to Source Voltage			±25	V
I _D	Drain Current -Continuous	T _C = 25 °C		-22	
	-Continuous	T _A = 25 °C	(Note 1a)	-4.4	Α
	-Pulsed			-70	
E _{AS}	Single Pulse Avalanche Energy		(Note 3)	384	mJ
P _D	Power Dissipation	T _C = 25 °C		104	W
	Power Dissipation	T _A = 25 °C	(Note 1a)	2.5	VV
T _J , T _{STG}	Operating and Storage Junction Tempera	ature Range		-55 to +150	°C

Thermal Characteristics

$R_{ heta JC}$	Thermal Resistance, Junction to Case	1.2	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1a)	50	C/VV

Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
FDMS86263P	FDMS86263P	Power 56	13 "	12 mm	3000 units

Electrical Characteristics $T_J = 25$ °C unless otherwise noted

Symbol	Parameter Test Conditions		Min	Тур	Max	Units
Off Chara	cteristics					
BV _{DSS}	Drain to Source Breakdown Voltage	$I_D = -250 \mu A, V_{GS} = 0 V$	-150			V
$\frac{\Delta BV_{DSS}}{\Delta T_{J}}$	Breakdown Voltage Temperature Coefficient	I_D = -250 μ A, referenced to 25 °C		-116		mV/°C
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} = -120 V, V _{GS} = 0 V			-1	μΑ
I _{GSS}	Gate to Source Leakage Current	$V_{GS} = \pm 25 \text{ V}, V_{DS} = 0 \text{ V}$			±100	nA

On Characteristics

$V_{GS(th)}$	Gate to Source Threshold Voltage	$V_{GS} = V_{DS}, I_{D} = -250 \mu A$	-2	-2.9	-4	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate to Source Threshold Voltage Temperature Coefficient	I_D = -250 μ A, referenced to 25 °C		7		mV/°C
		$V_{GS} = -10 \text{ V}, I_D = -4.4 \text{ A}$		42	53	
r _{DS(on)}	Static Drain to Source On Resistance	$V_{GS} = -6 \text{ V}, I_D = -4 \text{ A}$		45	64	mΩ
, ,		$V_{GS} = -10 \text{ V}, I_D = -4.4 \text{ A}, T_J = 125 \text{ °C}$		71	94	
9 _{FS}	Forward Transconductance	$V_{DS} = -10 \text{ V}, I_{D} = -4.4 \text{ A}$		19		S

Dynamic Characteristics

C _{iss}	Input Capacitance	75.77.77		2935	3905	pF
C _{oss}	Output Capacitance	V _{DS} = -75 V, V _{GS} = 0 V, f = 1 MHz		238	315	pF
C _{rss}	Reverse Transfer Capacitance			11	20	pF
R _a	Gate Resistance		0.1	2.7	5.4	Ω

Switching Characteristics

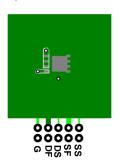
t _{d(on)}	Turn-On Delay Time			17	31	ns
t _r	Rise Time	$V_{DD} = -75 \text{ V}, I_D = -4.4 \text{ A},$		10	21	ns
t _{d(off)}	Turn-Off Delay Time	$V_{GS} = -10 \text{ V}, R_{GEN} = 6 \Omega$		37	59	ns
t _f	Fall Time			14	25	ns
Q_{g}	Total Gate Charge	V _{GS} = 0 V to -10 V		45	63	nC
Qg	Total Gate Charge	$V_{GS} = 0 \text{ V to -6 V}$ $V_{DD} = -$	75 V,	29	40	nC
Q_{gs}	Gate to Source Charge	$I_{D} = -4.4$	4 A	11.3		nC
Q_{gd}	Gate to Drain "Miller" Charge			8.9		nC

Drain-Source Diode Characteristics

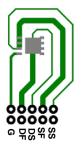
V _{SD}	Course to Drain Diado, Forward Voltage	$V_{GS} = 0 \text{ V}, I_{S} = -4.4 \text{ A}$	(Note 2)	-0.79	-1.3	V
	Source to Drain Diode Forward Voltage	$V_{GS} = 0 \text{ V}, I_{S} = -2 \text{ A}$	(Note 2)	-0.75	-1.2	V
t _{rr}	Reverse Recovery Time	I _F = -4.4 A, di/dt = 100 A/μs		91	146	ns
Q _{rr}	Reverse Recovery Charge			287	460	nC

Notes

^{1.} R_{BJA} is determined with the device mounted on a 1 in² pad 2 oz copper pad on a 1.5 x 1.5 in. board of FR-4 material. R_{BJC} is guaranteed by design while R_{BCA} is determined by the user's board design.



a) 50 °C/W when mounted on a 1 in² pad of 2 oz copper



b) 125 °C/W when mounted on a minimum pad of 2 oz copper.

- 2. Pulse Test: Pulse Width < 300 $\mu\text{s},$ Duty cycle < 2.0%.
- 3. Starting T_J = 25 °C; P-ch: L = 3 mH, I_{AS} = -16 A, V_{DD} = -150 V, V_{GS} = -10 V. 100% test at L = 0.1 mH, I_{AS} = -52 A.

Typical Characteristics T_J = 25 °C unless otherwise noted

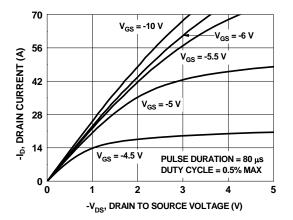


Figure 1. On Region Characteristics

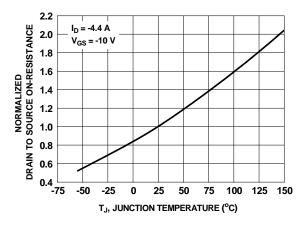


Figure 3. Normalized On Resistance vs Junction Temperature

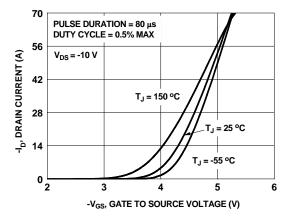


Figure 5. Transfer Characteristics

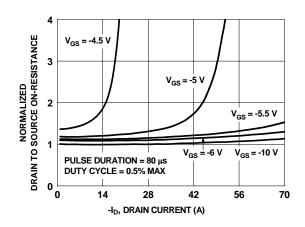


Figure 2. Normalized On-Resistance vs Drain Current and Gate Voltage

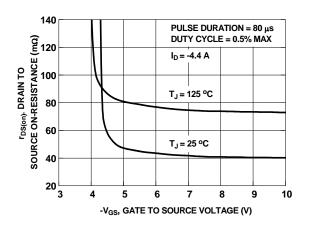


Figure 4. On-Resistance vs Gate to Source Voltage

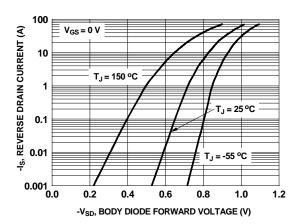


Figure 6. Source to Drain Diode Forward Voltage vs Source Current

Typical Characteristics $T_J = 25$ °C unless otherwise noted

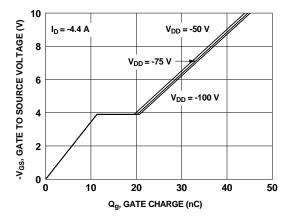
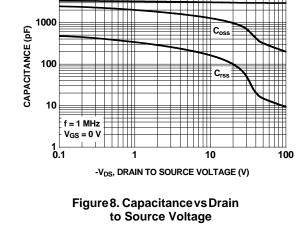


Figure 7. Gate Charge Characteristics



10000

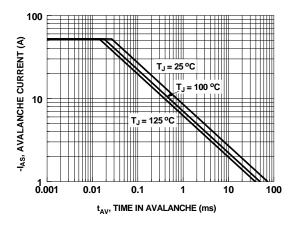


Figure 9. Unclamped Inductive Switching Capability

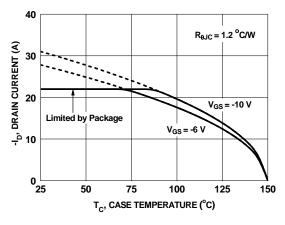


Figure 10. Maximum Continuous Drain Current vs Case Temperature

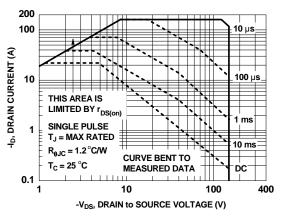


Figure 11. Forward Bias Safe Operating Area

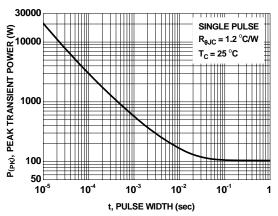


Figure 12. Single Pulse Maximum Power Dissipation

Typical Characteristics $T_J = 25$ °C unless otherwise noted

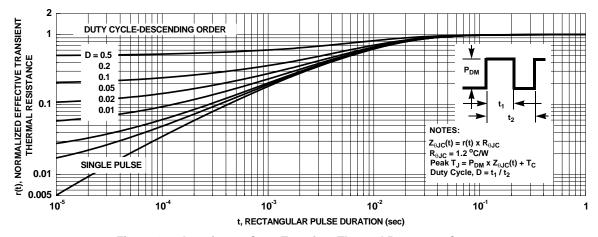
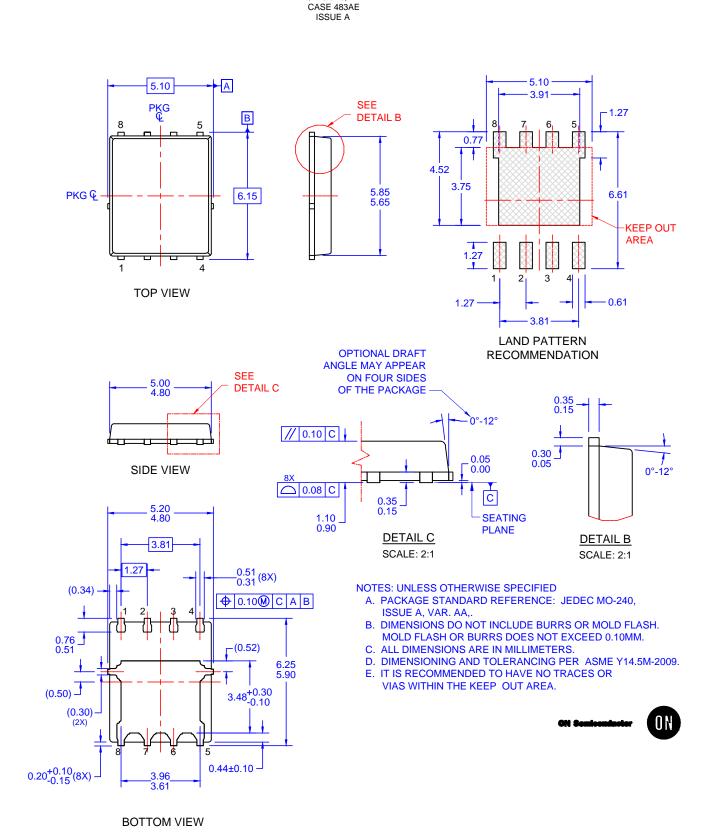


Figure 13. Junction-to-Case Transient Thermal Response Curve



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