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Please note: As part of the Fairchild Semiconductor integration, some of the Fairchild orderable part numbers will need to change in order to meet ON Semiconductor's system requirements. Since the ON Semiconductor product management systems do not have the ability to manage part nomenclature that utilizes an underscore (_), the underscore (_) in the Fairchild part numbers will be changed to a dash (-). This document may contain device numbers with an underscore (_). Please check the ON Semiconductor website to verify the updated device numbers. The most current and up-to-date ordering information can be found at www.onsemi.com. Please email any questions regarding the system integration to Fairchild_questions@onsemi.com.

September 2016

FDN028N20

N-Channel PowerTrench® MOSFET

20 V, 6.1 A, 28 mΩ

Features

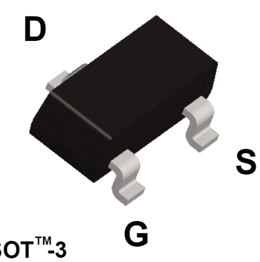
- Max $r_{DS(on)}$ = 28 mΩ at V_{GS} = 4.5 V, I_D = 5.2 A
- Max $r_{DS(on)}$ = 45 mΩ at V_{GS} = 2.5 V, I_D = 4.4 A
- High Performance Trench Technology for Extremely Low $r_{DS(on)}$
- High Power and Current Handling Capability in a Widely Used Surface Mount Package
- Fast Switching Speed
- 100% UIL Tested
- RoHS Compliant

General Description

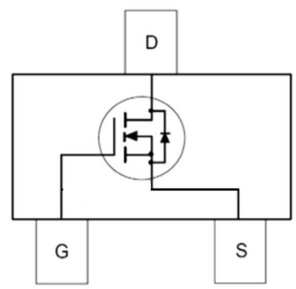
This N-Channel PowerTrench MOSFET is produced using Fairchild's advanced PowerTrench® process that has been especially tailored to minimize on-state resistance and yet maintain low gate charge for superior switching performance.

Applications

- Primary DC-DC Switch
- Load Switch



SuperSOT™-3



MOSFET Maximum Ratings T_C = 25°C unless otherwise noted.

Symbol	Parameter			Ratings	Units
V_{DS}	Drain to Source Voltage			20	V
V_{GS}	Gate to Source Voltage		(Note 3)	±12	V
I_D	-Continuous	T_A = 25°C	(Note 1a)	6.1	A
	-Pulsed		(Note 5)	52	
E_{AS}	Single Pulse Avalanche Energy		(Note 4)	6	mJ
P_D	Power Dissipation		(Note 1a)	1.5	W
	Power Dissipation		(Note 1b)	0.6	
T_J, T_{STG}	Operating and Storage Junction Temperature Range			-55 to + 150	°C

Thermal Characteristics

$R_{\theta JC}$	Thermal Resistance, Junction-to-Case	(Note 1)	75	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	(Note 1a)	80	°C/W

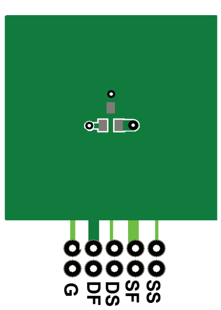
Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
28N	FDN028N20	SSOT-3	7 ”	8 mm	3000 units

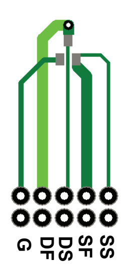
Electrical Characteristics T_J = 25°C unless otherwise noted.

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
Off Characteristics						
BV_{DSS}	Drain to Source Breakdown Voltage	I_D = 250 μA, V_{GS} = 0 V	20			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	I_D = 250 μA, referenced to 25°C		15		mV/°C
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 16 V, V_{GS} = 0 V			1	μA
I_{GSS}	Gate to Source Leakage Current	V_{GS} = 12 V, V_{DS} = 0 V			100	nA
On Characteristics						
$V_{GS(th)}$	Gate to Source Threshold Voltage	V_{GS} = V_{DS}, I_D = 250 μA	0.5	0.9	1.5	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate to Source Threshold Voltage Temperature Coefficient	I_D = 250 μA, referenced to 25°C		-3		mV/°C
$r_{DS(on)}$	Static Drain to Source On Resistance	V_{GS} = 4.5 V, I_D = 5.2 A		23	28	mΩ
		V_{GS} = 2.5 V, I_D = 4.4 A		32	45	
		V_{GS} = 4.5 V, I_D = 5.2 A, T_J = 125°C		30	41	
g_{FS}	Forward Transconductance	V_{DS} = 5 V, I_D = 5.2 A		28		S
Dynamic Characteristics						
C_{iss}	Input Capacitance	V_{DS} = 10 V, V_{GS} = 0 V, f = 1 MHz		399	600	pF
C_{oss}	Output Capacitance			91	140	pF
C_{rss}	Reverse Transfer Capacitance			87	130	pF
Switching Characteristics						
$t_{d(on)}$	Turn-On Delay Time	V_{DD} = 10 V, I_D = 5.2 A, V_{GS} = 10 V, R_{GEN} = 6 Ω		5	10	ns
t_r	Rise Time			2	10	ns
$t_{d(off)}$	Turn-Off Delay Time			15	29	ns
t_f	Fall Time			2	10	ns
$Q_{g(TOT)}$	Total Gate Charge	V_{GS} = 0 V to 4.5 V; V_{DD} = 10 V, I_D=5.2 A		4.3	6.0	nC
$Q_{g(TOT)}$	Total Gate Charge	V_{GS} = 0 V to 2.5 V		2.8	3.9	nC
Q_{gs}	Gate to Source Charge			0.7		nC
Q_{gd}	Gate to Drain “Miller” Charge			1.6		nC
Drain-Source Diode Characteristics						
V_{SD}	Source to Drain Diode Forward Voltage	V_{GS} = 0 V, I_S = 5.2 A (Note 2)		0.85	1.2	V
t_{rr}	Reverse Recovery Time	I_F = 5.2 A, di/dt = 100 A/μs		13	27	ns
Q_{rr}	Reverse Recovery Charge			3	10	nC

Notes:
1. $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.



a) 80 °C/W when mounted on a 1 in^2 pad of 2 oz copper



b) 180 °C/W when mounted on a minimum pad.

2. Pulse Test: Pulse Width < 300 μs, Duty cycle < 2.0%.
3. As an N-ch device, the negative Vgs rating is for low duty cycle pulse occurrence only. No continuous rating is implied.
4. E_{AS} of 6 mJ is based on starting T_J = 25 °C, L = 3 mH, I_{AS} = 2 A, V_{DD} = 20 V, V_{GS} = 10 V. 100% test at L = 0.1 mH, I_{AS} = 7 A.
5. Pulsed Id please refer to Fig 10 SOA graph for more details.

Typical Characteristics T_J = 25 °C unless otherwise noted.

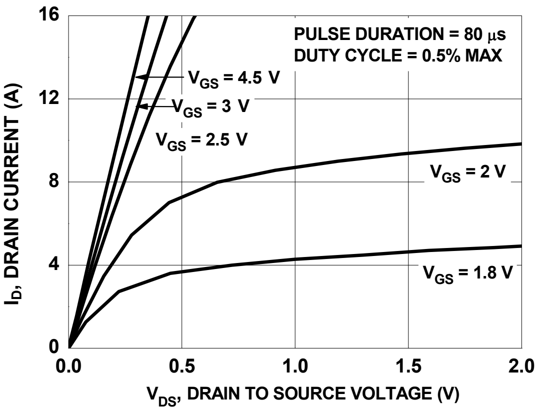


Figure 1. On Region Characteristics

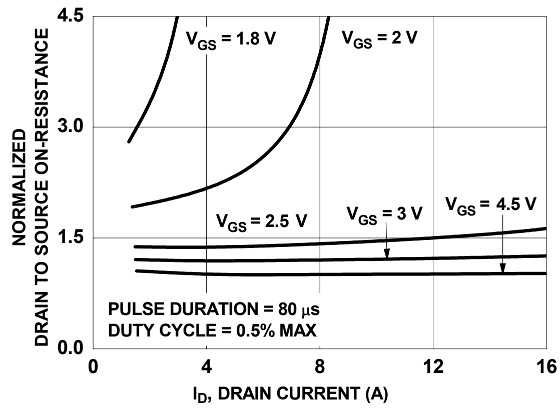


Figure 2. Normalized On-Resistance vs. Drain Current and Gate Voltage

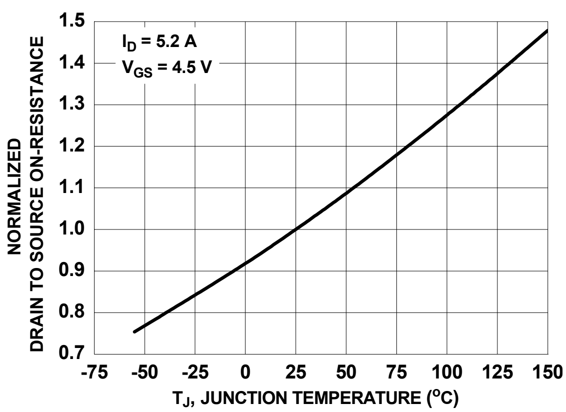


Figure 3. Normalized On Resistance vs. Junction Temperature

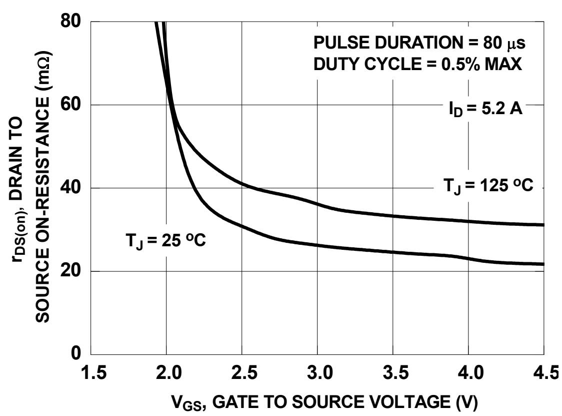


Figure 4. On-Resistance vs. Gate to Source Voltage

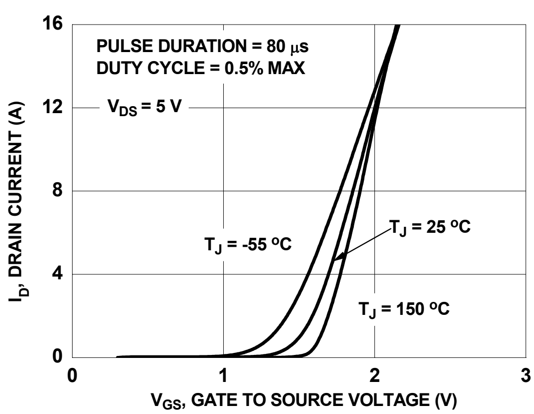


Figure 5. Transfer Characteristics

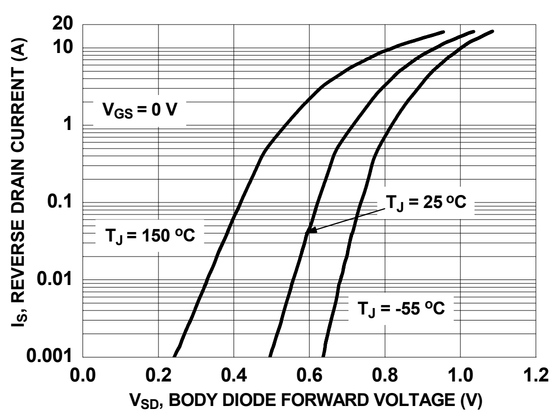


Figure 6. Source to Drain Diode Forward Voltage vs. Source Current

Typical Characteristics T_J = 25 °C unless otherwise noted.

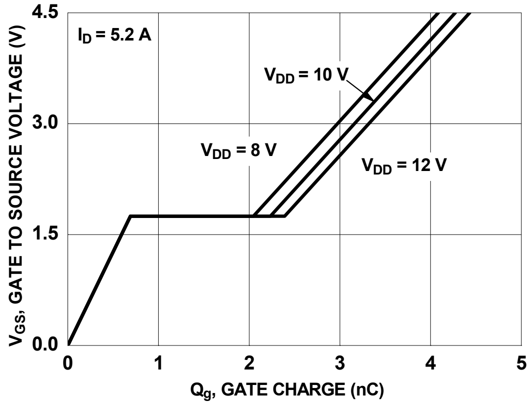


Figure 7. Gate Charge Characteristics

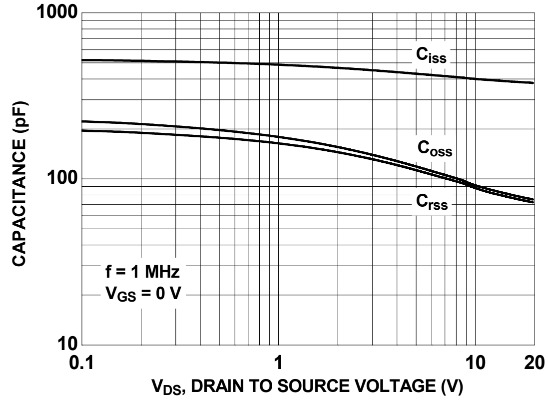


Figure 8. Capacitance vs. Drain to Source Voltage

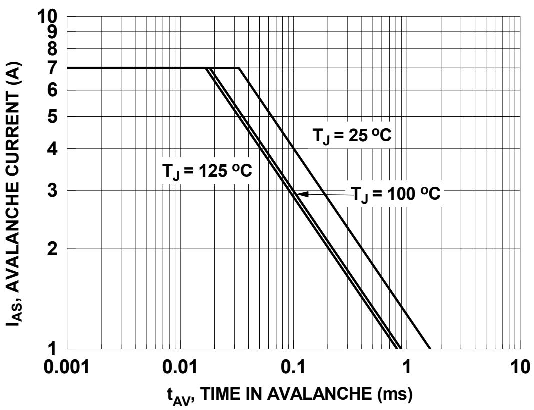


Figure 9. Unclamped Inductive Switching Capability

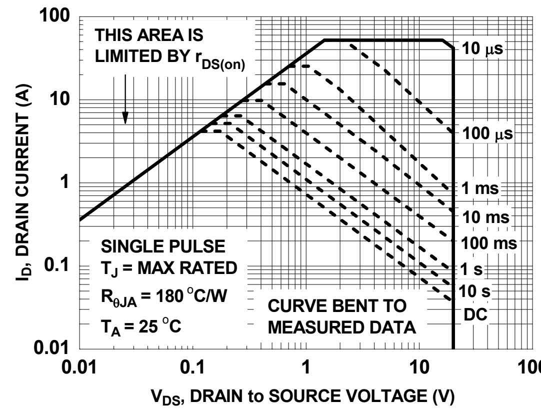


Figure 10. Forward Bias Safe Operating Area

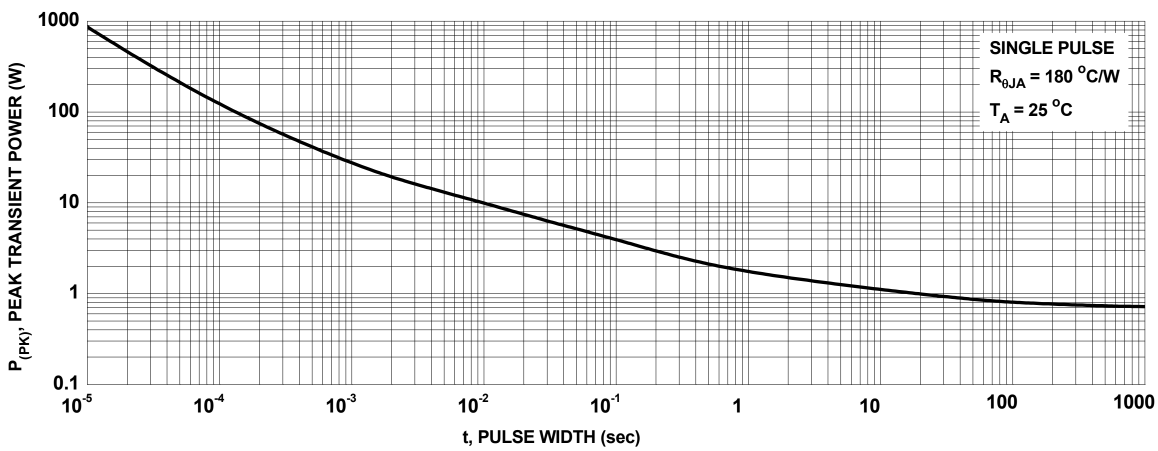


Figure 11. Single Pulse Maximum Power Dissipation

Typical Characteristics T_J = 25 °C unless otherwise noted.

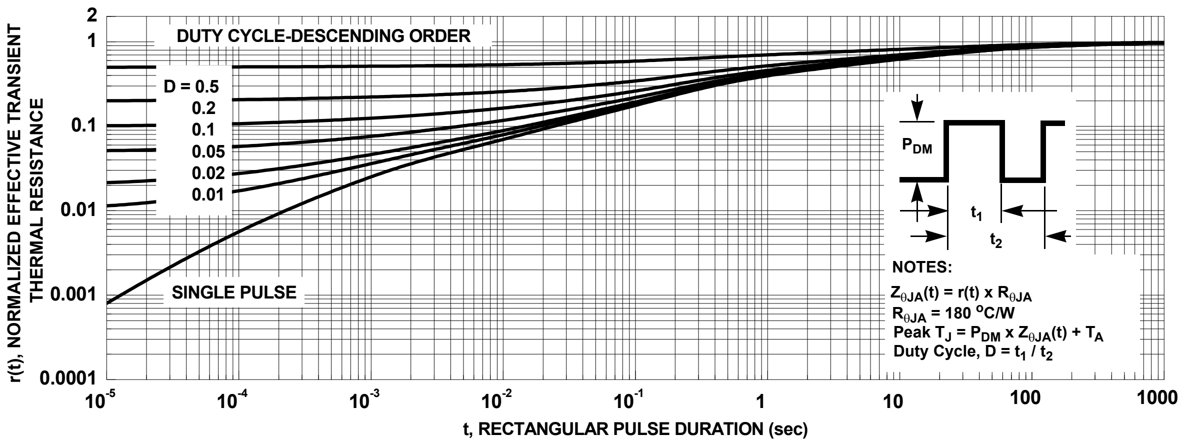
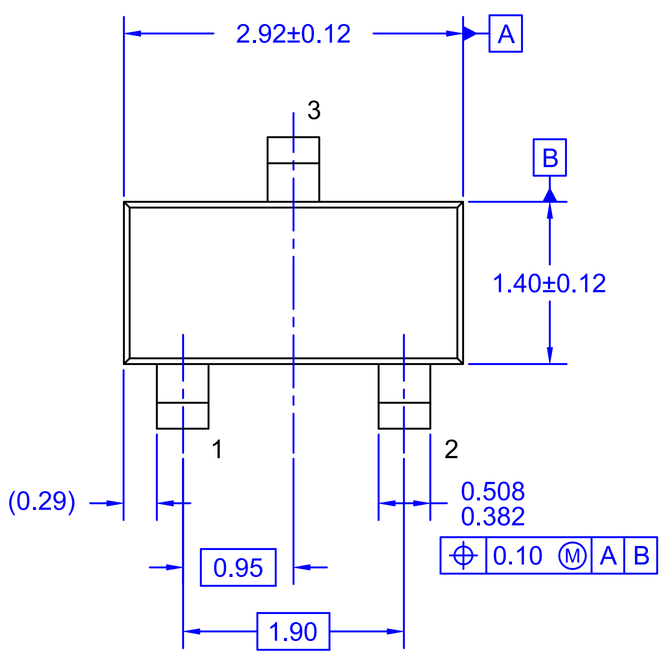
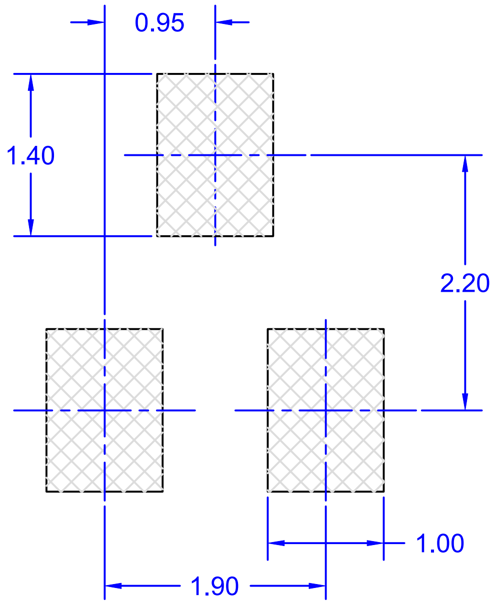
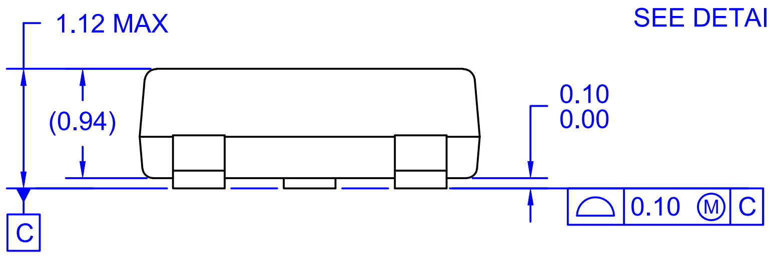


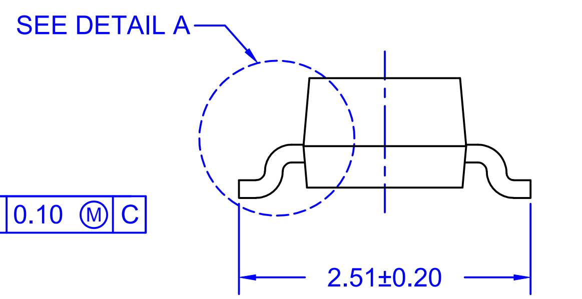
Figure 12. Junction-to-Ambient Transient Thermal Response Curve

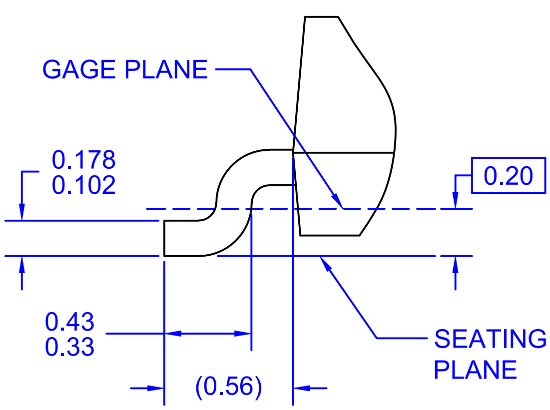




LAND PATTERN RECOMMENDATION







DETAIL A

SCALE: 50:1

NOTES: UNLESS OTHERWISE SPECIFIED

A) NO JEDEC REFERENCE AS OF AUGUST 2003
B) ALL DIMENSIONS ARE IN MILLIMETERS.
C) DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH AND TIE BAR EXTRUSIONS.
D) DIMENSIONING AND TOLERANCING PER ASME Y14.5M - 2009.
E) DRAWING FILE NAME: MKT-MA03BREV3

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