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FDN338P

November 2013

FDN338P

FAIRCHILD SEMICONDUCTOR IN

P-Channel 2.5V Specified PowerTrench[®] MOSFET

General Description

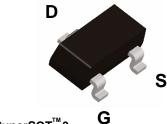
This P-Channel 2.5V specified MOSFET uses Fairchild's advanced low voltage PowerTrench process. It has been optimized for battery power management applications.

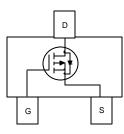
Applications

- Battery management
- Load switch
- Battery protection

Features

- -1.6 A, -20 V. $R_{DS(ON)} = 115 \text{ m}\Omega @ V_{GS} = -4.5 \text{ V}$ $R_{DS(ON)} = 155 \text{ m}\Omega @ V_{GS} = -2.5 \text{ V}$
- Fast switching speed
- High performance trench technology for extremely low R_{DS(ON)}
- SuperSOTTM -3 provides low $R_{DS(ON)}$ and 30% higher power handling capability than SOT23 in the same footprint





SuperSOT[™]-3

Absolute Maximum Ratings T_A=25°C unless otherwise noted

V _{DSS} Drain-Source Voltage -20 V _{GSS} Gate-Source Voltage ±8 Ib Drain Current - Continuous -1.6 - Pulsed 5 PD Maximum Power Dissipation (Note 1a) 0.5 (Note 1b) 0.466 -55 to +150	Symbol	Parameter		Ratings	Units
Ib Drain Current - Continuous -1.6 - Pulsed -5 -5 PD Maximum Power Dissipation (Note 1a) 0.5 (Note 1b) 0.46 0.46	DSS	Drain-Source Voltage		-20	V
- Pulsed 5 PD Maximum Power Dissipation (Note 1a) 0.5 (Note 1b) 0.46 0.46	GSS	Gate-Source Voltage		±8	V
Pb Maximum Power Dissipation (Note 1a) 0.5 (Note 1b) 0.46)	Drain Current – Continuous		-1.6	A
(Note 1b) 0.46		- Pulsed		-5	
	b	Maximum Power Dissipation	(Note 1a)	0.5	W
T _J , T _{STG} Operating and Storage Junction Temperature Range -55 to +150			(Note 1b)	0.46	
	j, T _{stg}	Operating and Storage Junction Temperature Range		-55 to +150	°C
Thermal Characteristics	hermal				

$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	(Note 1a)	250	°C/W
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case	(Note 1)	75	°C/W

Package Marking and Ordering Information

Device Marking	Device	Reel Size	Tape width	Quantity
338	FDN338P	7"	8mm	3000 units

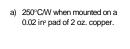
©2001 Fairchild Semiconductor Corporation

Symbol	Parameter	Test Conditions	Min	Тур	Max	Units
Off Char	acteristics					
BV _{DSS}	Drain–Source Breakdown Voltage	$V_{GS} = 0 V, I_{D} = -250 \mu A$	-20			V
$\Delta BV_{DSS} \Delta T_{J}$	Breakdown Voltage Temperature Coefficient	$l_{\rm D}$ = -250 µA, Referenced to 25°C		-16		mV/°C
IDSS	Zero Gate Voltage Drain Current	$V_{DS} = -16 V$, $V_{GS} = 0 V$			-1	μA
GSSF	Gate-Body Leakage, Forward	$V_{GS} = 8 \text{ V}, \qquad V_{DS} = 0 \text{ V}$			100	nA
GSSR	Gate–Body Leakage, Reverse	$V_{GS} = -8 \text{ V}, \qquad V_{DS} = 0 \text{ V}$			-100	nA
On Char	acteristics (Note 2)					
V _{GS(th)}	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_D = -250 \ \mu A$	-0.4	-0.8	-1.5	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate Threshold Voltage Temperature Coefficient	$I_D = -250 \ \mu\text{A}$, Referenced to 25°C		2.7		mV/°C
R _{DS(on)}	Static Drain–Source On–Resistance	$ \begin{array}{l} V_{GS} = -4.5 \ V, I_D = -1.6 \ A \\ V_{GS} = -2.5 \ V, I_D = -1.3 \ A \\ V_{GS} = -4.5 \ V, \ I_D = -1.6 \ A, \ T_J = 125^\circ C \end{array} $		88 117 116	115 155 165	mΩ
D(on)	On–State Drain Current	$V_{GS} = -4.5 V$, $V_{DS} = -5 V$	-5			Α
g fs	Forward Transconductance	$V_{DS} = -5 V$, $I_D = -1.6 A$		6		S
Dynamic	Characteristics					
Ciss	Input Capacitance	$V_{DS} = -10 V$, $V_{GS} = 0 V$,		451		pF
Coss	Output Capacitance	f = 1.0 MHz		75		pF
Crss	Reverse Transfer Capacitance			33		pF
Switchin	g Characteristics (Note 2)					
t _{d(on)}	Turn–On Delay Time	$V_{DD} = -10 V$, $I_D = -1 A$,		10	20	ns
tr	Turn–On Rise Time	$V_{GS} = -4.5 \text{ V}, \qquad R_{GEN} = 6 \ \Omega$		11	20	ns
t _{d(off)}	Turn–Off Delay Time			16	29	ns
t _f	Turn–Off Fall Time			6.5	13	ns
Qg	Total Gate Charge	$V_{DS} = -10 \text{ V}, I_D = -1.6 \text{ A},$		4.4	6.2	nC
Q _{gs}	Gate-Source Charge	$V_{GS} = -4.5 V$		1.1		nC
Q _{gd}	Gate–Drain Charge			0.7		nC
Drain-So	ource Diode Characteristics	and Maximum Ratings				
ls	Maximum Continuous Drain–Source				-0.42	Α
V _{SD}	Drain–Source Diode Forward Voltage	$V_{GS} = 0 V$, $I_S = -0.42$ (Note 2)		-0.7	-1.2	V

 R_{0JA} is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. R_{0JC} is guaranteed by design while R_{0CA} is determined by the user's board design.

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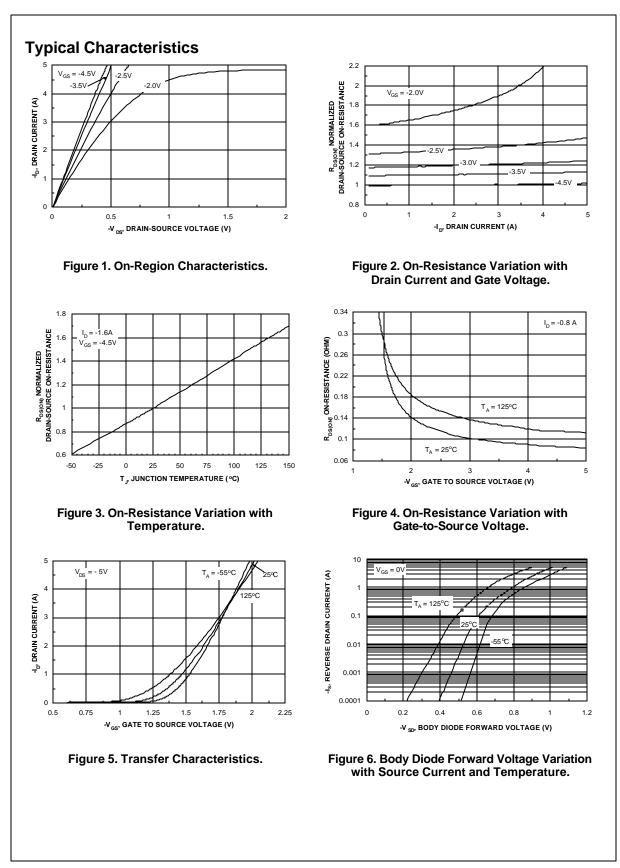


b) 270°C/W when mounted on a minimum pad.

Scale 1 : 1 on letter size paper

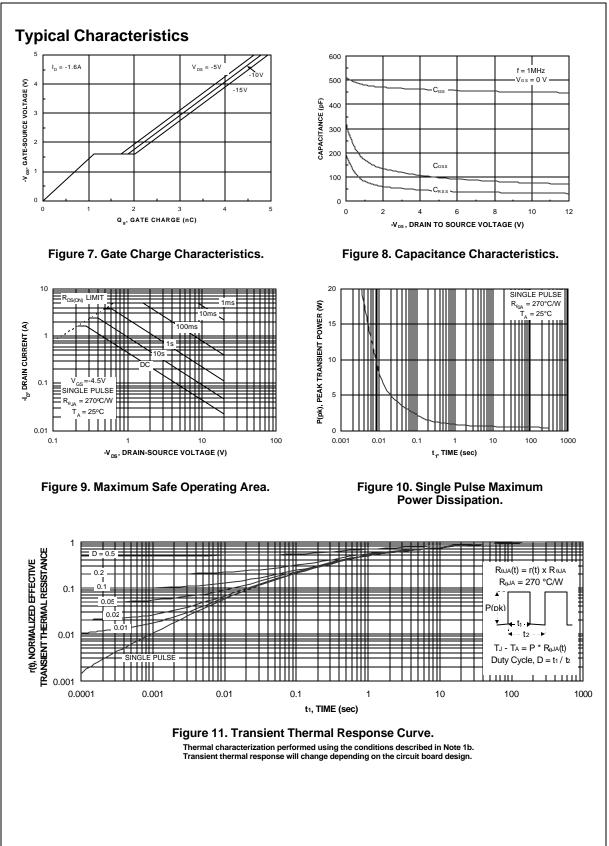
J

2. Pulse Test: Pulse Width \leq 300 μ s, Duty Cycle \leq 2.0%



FDN338P

FDN338P Rev F1(W)



FDN338P

FDN338P Rev F1(W)



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