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November 2013

FDP12N60NZ / FDPF12N60NZ N-Channel UniFETTM II MOSFET 600 V, 12 A, 650 m Ω

Features

- $R_{DS(on)}$ = 530 $m\Omega$ (Typ.) @ V_{GS} = 10 V, I_D = 6 A
- Low Gate Charge (Typ. 26 nC)
- Low C_{rss} (Typ. 12 pF)
- · 100% Avalanche Tested
- · Improved dv/dt Capability
- · ESD Improved Capability
- RoHS Compliant

Applications

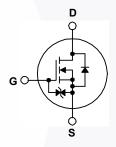
- LCD/ LED/ PDP TV
- Lighting
- · Uninterruptible Power Supply

Description

UniFETTM II MOSFET is Fairchild Semiconductor's high voltage MOSFET family based on advanced planar stripe and DMOS technology. This advanced MOSFET family has the smallest on-state resistance among the planar MOSFET, and also provides superior switching performance and higher avalanche energy strength. In addition, internal gate-source ESD diode allows UniFET II MOSFET to withstand over 2kV HBM surge stress. This device family is suitable for switching power converter applications such as power factor correction (PFC), flat panel display (FPD) TV power, ATX and electronic lamp ballasts.







MOSFET Maximum Ratings T_C = 25°C unless otherwise noted.

Symbol		Parameter	FD	P12N60NZ	FDPF12N60NZ	Unit	
V_{DSS}	Drain to Source Voltage	Drain to Source Voltage			600		
V_{GSS}	Gate to Source Voltage			±	30	V	
	Drain Current	- Continuous (T _C = 25°C)		12	12*	Α	
ID	Drain Current - Continuous (T _C = 100°C)			7.2	7.2*	A	
I _{DM}	Drain Current	- Pulsed (No	te 1)	48	48*	Α	
E _{AS}	Single Pulsed Avalanche Energy (Note 2)		te 2)	565		mJ	
I _{AR}	Avalanche Current (Note 1		te 1)) 12		Α	
E _{AR}	Repetitive Avalanche Energy (Note 1)		te 1)	24		mJ	
dv/dt	MOSFET dv/dt Ruggedness			20		V/ns	
uv/ut	Peak Diode Recovery dv/dt	(No	te 3)	3) 10		V/ns	
Б	$(T_C = 25^{\circ}C)$			240	39	W	
P_{D}	Power Dissipation - Derate Above 25°C			2.0	0.3	W/°C	
T _J , T _{STG}	Operating and Storage Temperature Range -55 to +150			+150	°C		
T _L	Maximum Lead Temperature for	or Soldering, 1/8" from Case for 5 Seco	nds	30	00	°C	

^{*}Drain current limited by maximum junction temperature

Thermal Characteristics

Symbol	Parameter FDP		FDPF12N60NZ	Unit
$R_{\theta JC}$	Thermal Resistance, Junction to Case, Max.	0.52	3.2	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient, Max.	62.5	62.5	- 0/00

Package Marking and Ordering Information

Part Number	Top Mark	Package	Packing Method	Reel Size	Tape Width	Quantity
FDP12N60NZ	FDP12N60NZ	TO-220	Tube	N/A	N/A	50 units
FDPF12N60NZ	FDPF12N60NZ	TO-220F	Tube	N/A	N/A	50 units

Electrical Characteristics T_C = 25°C unless otherwise noted.

Symbol	Parameter	Test Conditions	Min.	Тур.	Max.	Unit
Off Charac	cteristics					
BV _{DSS}	Drain to Source Breakdown Voltage	$I_D = 250 \mu A, V_{GS} = 0 V, T_J = 25^{\circ} C$	600	-	-	V
ΔBV _{DSS} / ΔT _J	Breakdown Voltage Temperature Coefficient	I_D = 250 μ A, Referenced to 25°C	-	0.6	-	V/°C
	Zero Gate Voltage Drain Current	V _{DS} = 600 V, V _{GS} = 0 V	-	-	1	μА
I _{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = 480 \text{ V}, T_{C} = 125^{\circ}\text{C}$	-	-	10	μΑ
I _{GSS}	Gate to Body Leakage Current	V _{GS} = ±30 V, V _{DS} = 0 V	-	-	±10	μΑ

On Characteristics

$V_{GS(th)}$	Gate Threshold Voltage	$V_{GS} = V_{DS}, I_{D} = 250 \mu\text{A}$	3	-	5	V
R _{DS(on)}	Static Drain to Source On Resistance	$V_{GS} = 10 \text{ V}, I_D = 6 \text{ A}$	-	0.53	0.65	Ω
9 _{FS}	Forward Transconductance	V _{DS} = 20 V, I _D = 6 A	-	13.5	-	S

Dynamic Characteristics

C _{iss}	Input Capacitance	V 05.V.V 0.V		-	1260	1676	pF
C _{oss}	Output Capacitance	V _{DS} = 25 V, V _{GS} = 0 V, f = 1 MHz		-	150	200	pF
C _{rss}	Reverse Transfer Capacitance	1 - 1 1/11/12	-	- \	12	18	pF
Q _{g(tot)}	Total Gate Charge at 10V	V _{DS} = 480 V, I _D = 12 A,		- \	26	34	nC
Q_{gs}	Gate to Source Gate Charge	V _{GS} = 10 V	-	-	6	-	nC
Q_{gd}	Gate to Drain "Miller" Charge	((Note 4)	-	10	-	nC

Switching Characteristics

t _{d(on)}	Turn-On Delay Time		-	25	60	ns
t _r		$V_{DD} = 300 \text{ V}, I_D = 12 \text{ A},$	-	50	110	ns
t _{d(off)}	Turn-Off Delay Time	V_{GS} = 10 V, R_G = 25 Ω	-	80	170	ns
t _f	Turn-Off Fall Time	(Note 4)	-	60	130	ns

Drain-Source Diode Characteristics

Is	Maximum Continuous Drain to Source Dioc	Maximum Continuous Drain to Source Diode Forward Current		-	12	Α
I _{SM}	Maximum Pulsed Drain to Source Diode Forward Current		-	-	48	Α
V _{SD}	Drain to Source Diode Forward Voltage	V _{GS} = 0 V, I _{SD} = 12 A	-	-	1.4	V
t _{rr}	Reverse Recovery Time	V _{GS} = 0 V, I _{SD} = 12 A,	-	350	/ -	ns
Q _{rr}	Reverse Recovery Charge	dI _F /dt = 100 A/μs	-	2.2	-	μC

- 1: Repetitive rating: pulse-width limited by maximum junction temperature.
- 2: L = 7.85 mH, I_{AS} = 12 A, V_{DD} = 50 V, R_{G} = 25 Ω , starting T_{J} = 25°C. 3: I_{SD} \leq 12 A, di/dt \leq 200 A/ μ s, V_{DD} \leq BV $_{DSS}$, starting T_{J} = 25°C.
- 4: Essentially independent of operating temperature typical characteristics.



Typical Performance Characteristics

Figure 1. On-Region Characteristics

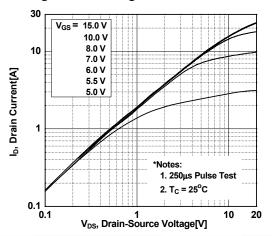


Figure 3. On-Resistance Variation vs.

Drain Current and Gate Voltage

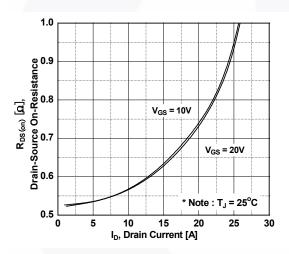


Figure 5. Capacitance Characteristics

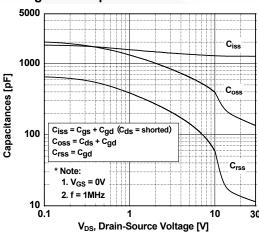


Figure 2. Transfer Characteristics

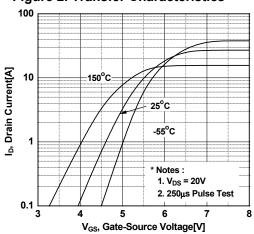


Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature

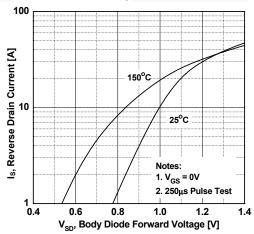
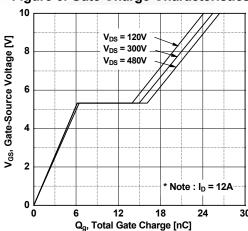


Figure 6. Gate Charge Characteristics



Typical Performance Characteristics (Continued)

Figure 7. Breakdown Voltage Variation vs. Temperature

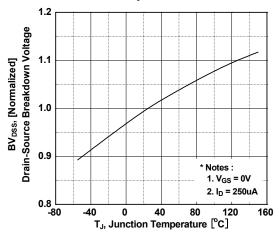


Figure 9. Maximum Safe Operating Area - FDPF12N60NZ

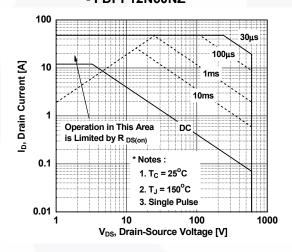


Figure 8. On-Resistance Variation vs Temperature

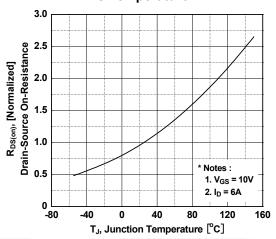


Figure 10. Maximum Safe Operating Area - FDP12N60NZ

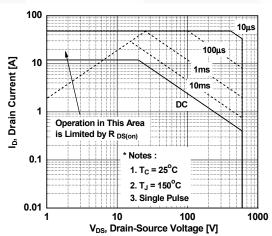
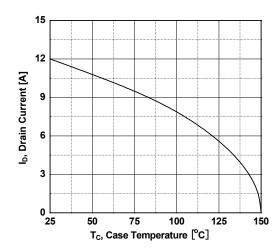


Figure 11. Maximum Drain Current vs. Case Temperature



Typical Performance Characteristics (Continued)

Figure 12. Transient Thermal Response Curve - FDPF12N60NZ

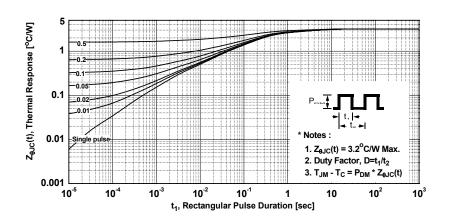
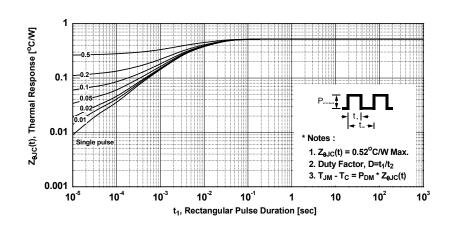


Figure 13. Transient Thermal Response Curve - FDP12N60NZ



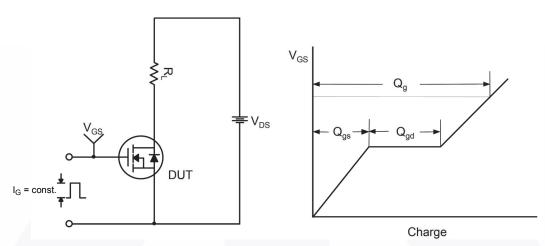


Figure 14. Gate Charge Test Circuit & Waveform

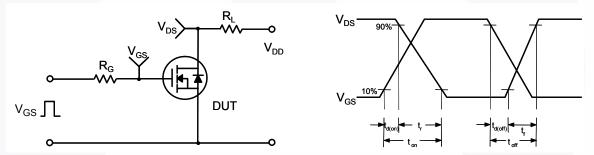


Figure 15. Resistive Switching Test Circuit & Waveforms

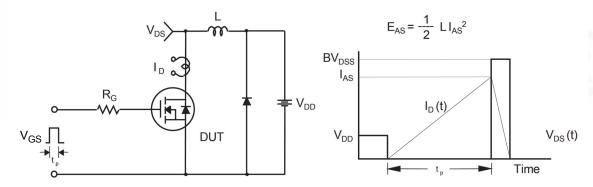


Figure 16. Unclamped Inductive Switching Test Circuit & Waveforms

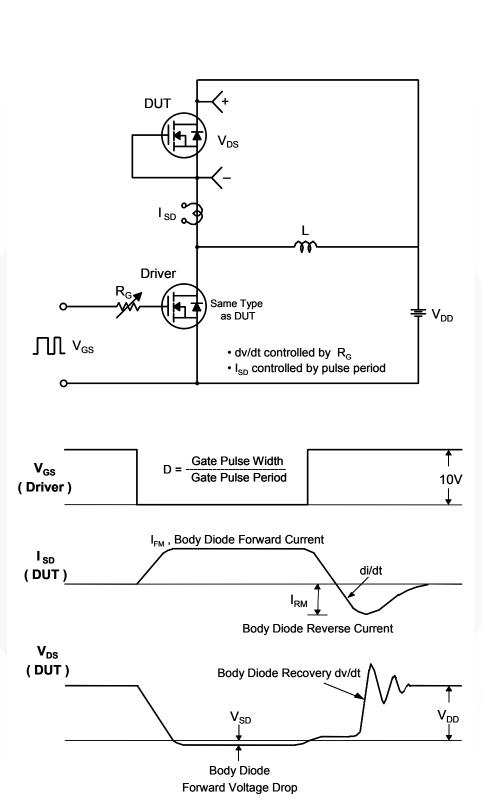


Figure 17. Peak Diode Recovery dv/dt Test Circuit & Waveforms

Mechanical Dimensions

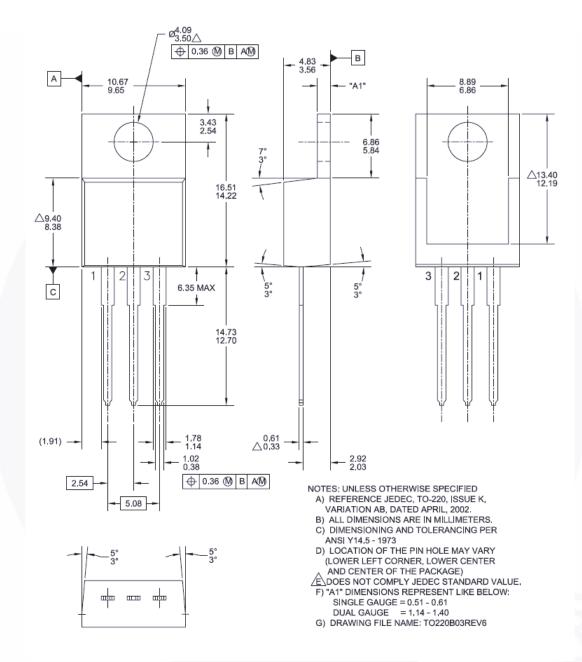


Figure 18. TO-220, Molded, 3-Lead, Jedec Variation AB

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Mechanical Dimensions

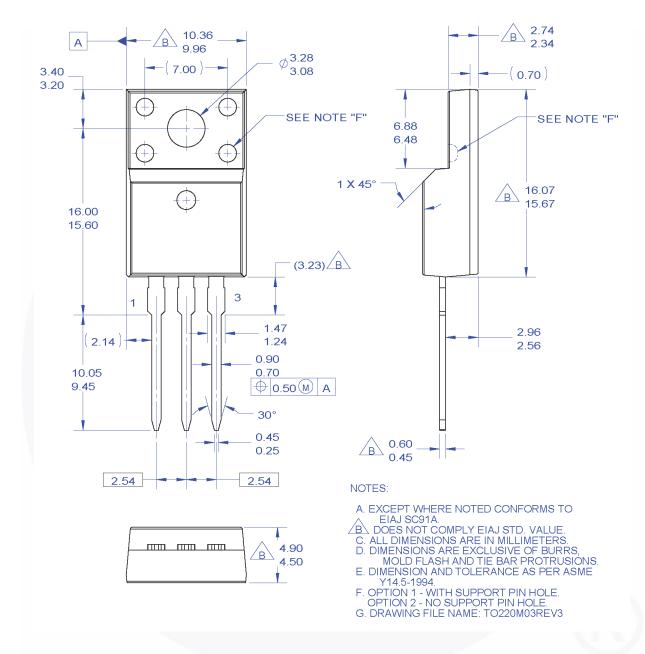


Figure 19. TO220, Molded, 3-Lead, Full Pack, EIAJ SC91, Straight Lead

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