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December 2013

FDP5N50NZ / FDPF5N50NZ

N-Channel UniFETTM II MOSFET 500 V, 4.5 A, 1.5 Ω

Features

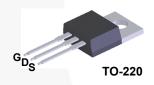
- R $_{\mathrm{DS(on)}}$ = 1.38 Ω (Typ.) @ $\mathrm{V_{GS}}$ = 10 V, $\mathrm{I_{D}}$ = 2.25 A
- Low Gate Charge (Typ. 9 nC)
- Low C_{RSS} (Typ. 4 pF)
- · 100% Avalanche Tested
- · Improved dv/dt Capability
- · ESD Improved Capability
- RoHS Compliant

Applications

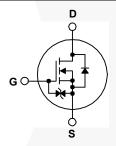
- · LCD/ LED TV
- Lighting
- Uninterruptible Power Supply
- · AC-DC Power Supply

Description

UniFETTM II MOSFET is Fairchild Semiconductor's high voltage MOSFET family based on advanced planar stripe and DMOS technology. This advanced MOSFET family has the smallest on-state resistance among the planar MOSFET, and also provides superior switching performance and higher avalanche energy strength. In addition, internal gate-source ESD diode allows UniFET II MOSFET to withstand over 2kV HBM surge stress. This device family is suitable for switching power converter applications such as power factor correction (PFC), flat panel display (FPD) TV power, ATX and electronic lamp ballasts.







MOSFET Maximum Ratings T_C = 25°C unless otherwise noted.

Symbol		Parameter		FDP5N50NZ	FDPF5N50NZ	Unit
V _{DSS}	Drain to Source Voltage	Drain to Source Voltage		5	V	
V _{GSS}	Gate to Source Voltage			±25		V
	Drain Current	- Continuous (T _C = 25°C)		4.5	4.5*	Α
ID	Dialii Cuiterii	- Continuous (T _C = 100°C)	1	2.7	2.7*	_ A
I _{DM}	Drain Current	- Pulsed	(Note 1)	18	18*	Α
E _{AS}	Single Pulsed Avalanche Energy		(Note 2)	160		mJ
I _{AR}	Avalanche Current		(Note 1)	4.5		Α
E _{AR}	Repetitive Avalanche Energy		(Note 1)	7.8		mJ
dv/dt	Peak Diode Recovery dv/dt		(Note 3)		10	V/ns
D	Dower Discinstian	(T _C = 25°C)		78	30	W
P_{D}	Power Dissipation	- Derate above 25°C		0.62	0.24	W/ºC
T _J , T _{STG}	Operating and Storage Temperature Range		-55 to +150		°C	
T _L	Maximum Lead Temperature for Soldering , 1/8" from Case for 5 Seconds.			3	300	°C

^{*}Drain current limited by maximum junction temperature

Thermal Characteristics

Symbol	Parameter	FDP5N50NZ	FDPF5N50NZ	Unit
$R_{\theta JC}$	Thermal Resistance, Junction to Case, Max.	1.6	4.1	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient, Max.	62.5	62.5	- 0/00

Package Marking and Ordering Information

Part Number	Top Mark	Package	Packing Method	Reel Size	Tape Width	Quantity
FDP5N50NZ	FDP5N50NZ	TO-220	Tube	N/A	N/A	50 units
FDPF5N50NZ	FDPF5N50NZ	TO-220F	Tube	N/A	N/A	50 units

Test Conditions

Min.

Тур.

Max.

Unit

Electrical Characteristics $T_C = 25^{\circ}C$ unless otherwise noted. **Parameter**

BV _{DSS}	Drain to Source Breakdown Voltage	1 050 A V 0 V T 0500	500	_	T _	V
DVDSS	Diam to Source Dreakdown Voltage	$I_D = 250 \mu\text{A}, V_{GS} = 0 \text{V}, T_C = 25^{\circ}\text{C}$	300	_	_	V
ΔBV _{DSS} / ΔΤ _J	Breakdown Voltage Temperature Coefficient	$I_D = 250 \mu\text{A}$, Referenced to 25°C	-	0.5	-	0
I	Zero Gate Voltage Drain Current	V _{DS} = 500 V, V _{GS} = 0 V	-	-	1	μА
DSS	Zero Gate Voltage Drain Gurrent	$V_{DS} = 400 \text{ V}, V_{GS} = 0 \text{ V}, T_{C} = 125^{\circ}\text{C}$	-	-	10	μΛ
I _{GSS}	Gate to Body Leakage Current	$V_{GS} = \pm 25 \text{ V}, V_{DS} = 0 \text{ V}$	-	-	±10	μΑ

On Characteristics

Symbol

٧	/ _{GS(th)}	Gate Threshold Voltage	$V_{GS} = V_{DS}, I_{D} = 250 \mu\text{A}$	3.0	-	5.0	V
R	R _{DS(on)}	Static Drain to Source On Resistance	$V_{GS} = 10 \text{ V}, I_D = 2.25 \text{ A}$	•	1.38	1.5	Ω
g	JFS	Forward Transconductance	$V_{DS} = 20 \text{ V}, I_{D} = 2.25 \text{ A}$	-	3.54	-	S

Dynamic Characteristics

C _{iss}	Input Capacitance	V 25 V V 20 V	-	330	440	pF
Coss	Output Capacitance	$V_{DS} = 25 \text{ V}, V_{GS} = 0 \text{ V}$ f = 1 MHz		50	70	pF
C _{rss}	Reverse Transfer Capacitance	1 - 1 1011 12	-	4	8	pF
Q _{g(tot)}	Total Gate Charge at 10V		-	9	12	nC
Q _{gs}	Gate to Source Gate Charge	$V_{DS} = 400 \text{ V I}_{D} = 4.5 \text{ A}$	-	2	-	nC
Q _{gd}	Gate to Drain "Miller" Charge	V _{GS} = 10 V (Note	4) -	4	-	nC

Switching Characteristics

t _{d(on)}	Turn-On Delay Time		-	12	35	ns
t _r		$V_{DD} = 250 \text{ V}, I_D = 4.5 \text{ A}$	-/	22	55	ns
t _{d(off)}	Turn-Off Delay Time	$V_{GS} = 10 \text{ V}, R_{GEN} = 25 \Omega$	-	28	65	ns
t _f	Turn-Off Fall Time	(Note 4)	/-	21	50	ns

Drain-Source Diode Characteristics

I _S	Maximum Continuous Drain to Source Dioc	Maximum Continuous Drain to Source Diode Forward Current		-	4.5	Α
I_{SM}	Maximum Pulsed Drain to Source Diode Forward Current		-	-	18	Α
V_{SD}	Drain to Source Diode Forward Voltage	V _{GS} = 0 V, I _{SD} = 4.5 A	-	- y	1.4	V
t _{rr}	Reverse Recovery Time	V _{GS} = 0 V, I _{SD} = 4.5 A	-	210	-	ns
Q _{rr}	Reverse Recovery Charge	$dI_F/dt = 100 A/\mu s$	-	1.1	-	μС

- 1: Repetitive rating: pulse-width limited by maximum junction temperature.
- 2: L = 15.8 mH, I $_{AS}$ = 4.5 A, V $_{DD}$ = 50 V, R $_{G}$ = 25 $\Omega,~$ starting T $_{J}$ = 25 $^{\circ}C.$
- 3: I_{SD} $\,\leq$ 2.8 A, di/dt \leq 200 A/µs $\,$, V_{DD} \leq BV_{DSS}, starting T_J = 25°C.
- 4: Essentially independent of operating temperature typical characteristics.

Typical Performance Characteristics

Figure 1. On-Region Characteristics

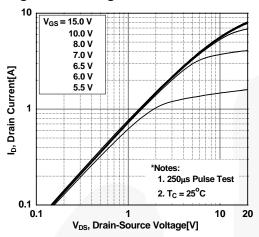


Figure 3. On-Resistance Variation vs.

Drain Current and Gate Voltage

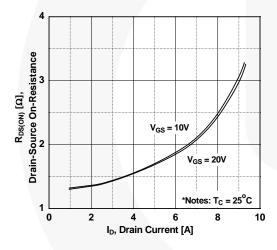


Figure 5. Capacitance Characteristics

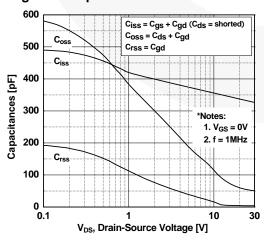


Figure 2. Transfer Characteristics

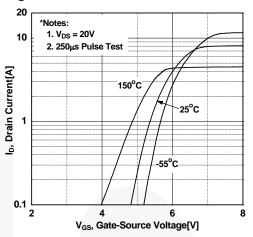


Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature

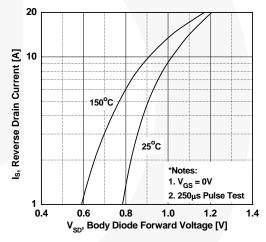
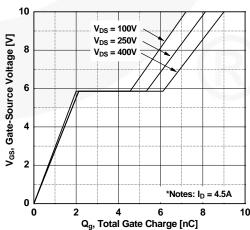


Figure 6. Gate Charge Characteristics



Typical Performance Characteristics (Continued)

Figure 7. Breakdown Voltage Variation vs. Temperature

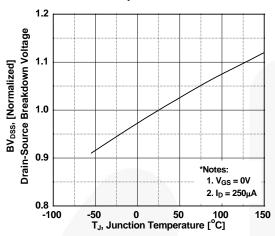


Figure 9. Maximum Safe Operating Area for FDP5N50NZ

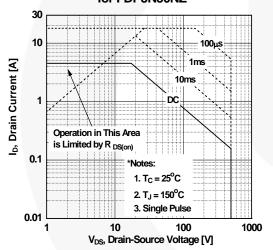


Figure 11. Maximum Drain Current vs. Case Temperature

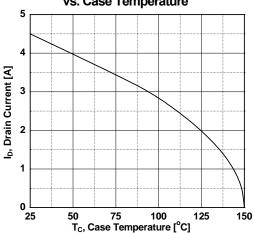


Figure 8. On-Resistance Variation vs. Temperature

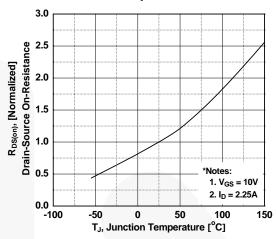
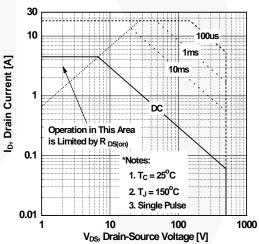


Figure 10. Maximum Safe Operating Area for FDPF5N50NZ



Typical Performance Characteristics (Continued)

Figure 12. Transient Thermal Response Curve for FDP5N50NZ

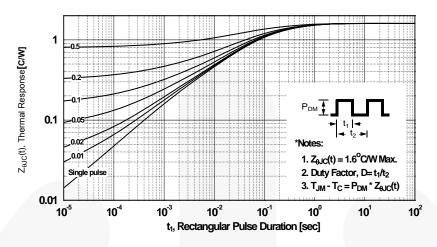
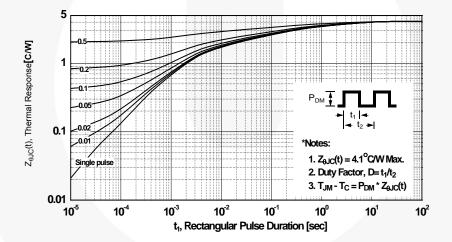


Figure 13. Transient Thermal Response Curve for FDPF5N50NZ



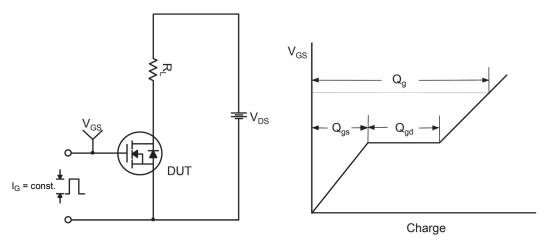


Figure 14. Gate Charge Test Circuit & Waveform

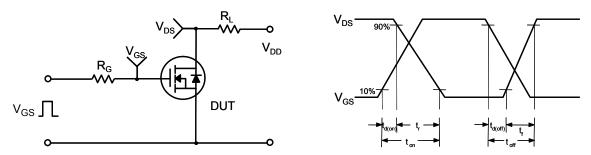


Figure 15. Resistive Switching Test Circuit & Waveforms

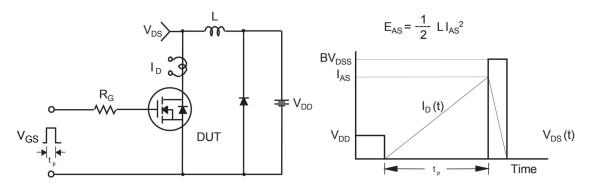
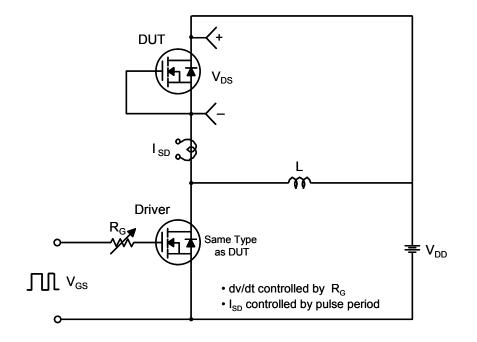


Figure 16. Unclamped Inductive Switching Test Circuit & Waveforms



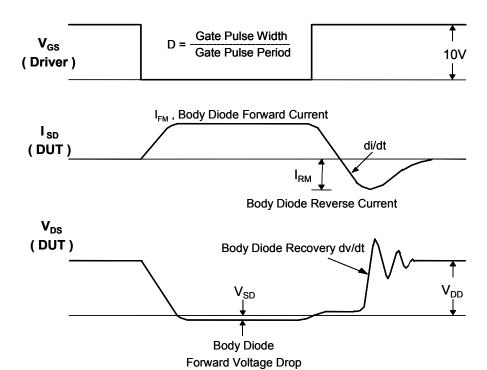


Figure 17. Peak Diode Recovery dv/dt Test Circuit & Waveforms

Mechanical Dimensions

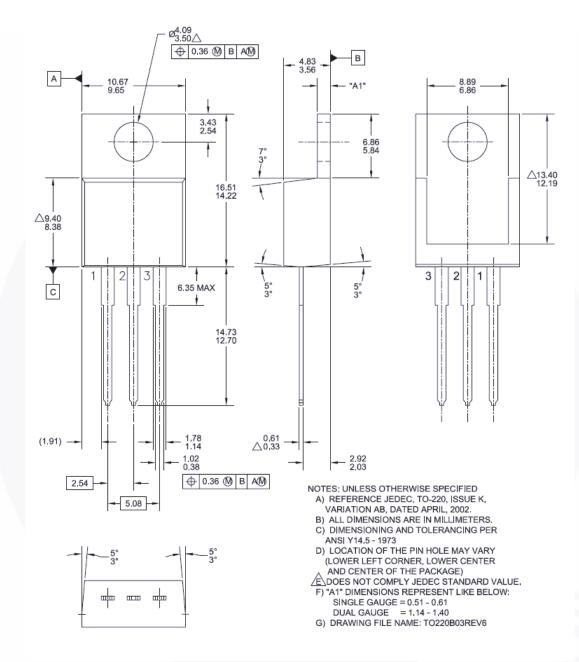


Figure 18. TO-220, Molded, 3-Lead, Jedec Variation AB

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Mechanical Dimensions

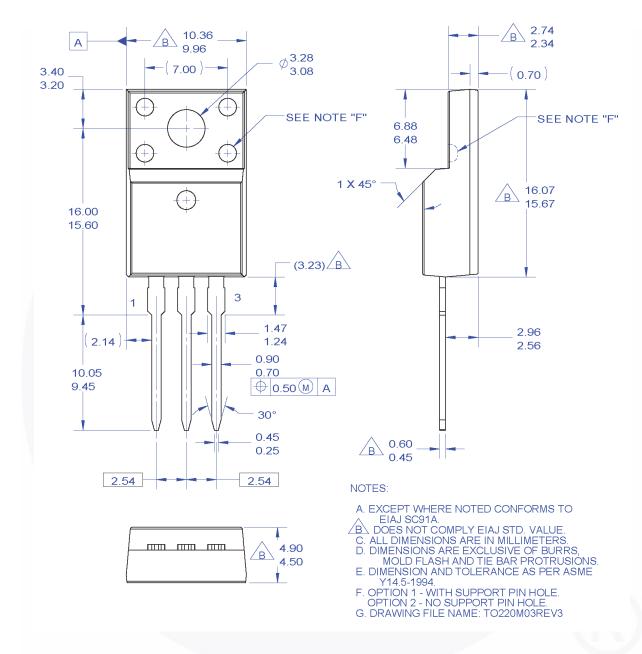


Figure 19. TO220, Molded, 3-Lead, Full Pack, EIAJ SC91, Straight Lead

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