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October 2016

FDPC3D5N025X9D

PowerTrench® Power Clip
25V Symmetric Dual N-Channel MOSFET

Features

Q1: N-Channel

- Max $r_{DS(on)}$ = 3.01 mΩ at V_{GS} = 10 V, I_D = 18 A
- Max $r_{DS(on)}$ = 3.67 mΩ at V_{GS} = 4.5 V, I_D = 16 A

Q2: N-Channel

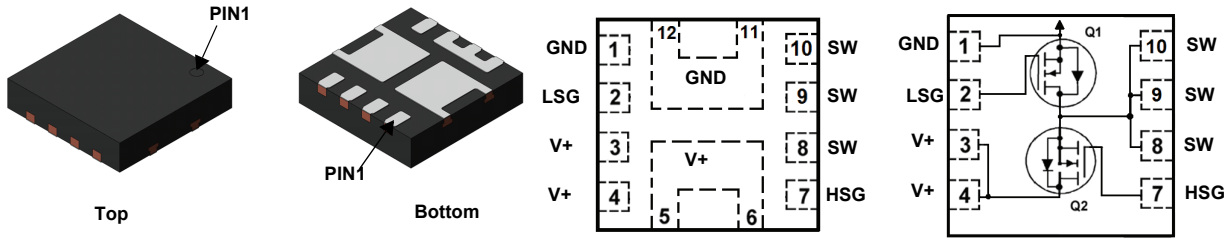
- Max $r_{DS(on)}$ = 3.01 mΩ at V_{GS} = 10 V, I_D = 18 A
- Max $r_{DS(on)}$ = 3.67 mΩ at V_{GS} = 4.5 V, I_D = 16 A
- Low Inductance Packaging Shortens Rise/Fall Times, Resulting in Lower Switching Losses
- MOSFET Integration Enables Optimum Layout for Lower Circuit Inductance and Reduced Switch Node Ringing
- RoHS Compliant

General Description

This device includes two specialized N-Channel MOSFETs in a dual package. The switch node has been internally connected to enable easy placement and routing of synchronous buck converters. The control MOSFET (Q2) and synchronous (Q1) have been designed to provide optimal power efficiency.

Applications

- Computing
- Communications
- General Purpose Point of Load



Power Clip 33 Symmetric

Pin	Name	Description	Pin	Name	Description	Pin	Name	Description
1,11,12	GND(LSS)	Low Side Source	3,4,5,6	V+(HSD)	High Side Drain	8,9,10	SW	Switching Node, Low Side Drain
2	LSG	Low Side Gate	7	HSG	High Side Gate			

MOSFET Maximum Ratings T_A = 25 °C unless otherwise noted.

Symbol	Parameter				Q1	Q2	Units
V_{DS}	Drain to Source Voltage				25	25	V
V_{GS}	Gate to Source Voltage				±12	±12	V
I_D	Drain Current	-Continuous	T_C = 25 °C	(Note5)	74	74	A
		-Continuous	T_C = 100 °C	(Note5)	47	47	
		-Continuous	T_A = 25 °C		18[Note1a]	18[Note1b]	
		-Pulsed	T_A = 25 °C	(Note 4)	349	349	
E_{AS}	Single Pulse Avalanche Energy			(Note 3)	96	96	mJ
P_D	Power Dissipation for Single Operation		T_C = 25 °C		26	26	W
	Power Dissipation for Single Operation		T_A = 25 °C		1.8[Note1a]	1.8[Note1b]	
T_J, T_{STG}	Operating and Storage Junction Temperature Range				-55 to +150		°C

Thermal Characteristics

$R_{\theta JC}$	Thermal Resistance, Junction to Case	4.8	4.8	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	70[Note1a]	70[Note1b]	
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	135[Note1c]	135[Note1d]	

Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
FDPCN025X9D	FDPC3D5N025X9D	Power Clip 33 Symm	13 ”	12 mm	3000 units

Electrical Characteristics T_J = 25 °C unless otherwise noted.

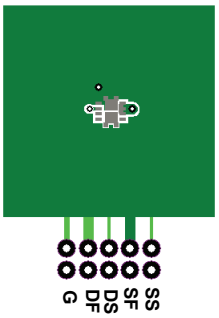
Symbol	Parameter	Test Conditions	Type	Min.	Typ.	Max.	Units
Off Characteristics							
BV_{DSS}	Drain to Source Breakdown Voltage	I_D = 250 μA, V_{GS} = 0 V I_D = 250 μA, V_{GS} = 0 V	Q1 Q2	25 25			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	I_D = 250 μA, referenced to 25 °C I_D = 250 μA, referenced to 25 °C	Q1 Q2		23 23		mV/°C
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 20 V, V_{GS} = 0 V V_{DS} = 20 V, V_{GS} = 0 V	Q1 Q2			1 1	μA μA
I_{GSS}	Gate to Source Leakage Current, Forward	V_{GS} = 12 V/-8 V, V_{DS}= 0 V V_{GS} = 12 V/-8 V, V_{DS}= 0 V	Q1 Q2			±100 ±100	nA nA
On Characteristics							
$V_{GS(th)}$	Gate to Source Threshold Voltage	V_{GS} = V_{DS}, I_D = 250 μA V_{GS} = V_{DS}, I_D = 250 μA	Q1 Q2	1.0 1.0	1.5 1.5	3.0 3.0	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate to Source Threshold Voltage Temperature Coefficient	I_D = 250 μA, referenced to 25 °C I_D = 250 μA, referenced to 25 °C	Q1 Q2		-4 -4		mV/°C
$r_{DS(on)}$	Drain to Source On Resistance	V_{GS} = 10V, I_D = 18 A V_{GS} = 4.5 V, I_D = 16 A V_{GS} = 10 V, I_D = 18 A,T_J =125 °C	Q1		2.0 2.4 2.87	3.01 3.67 4.32	mΩ
		V_{GS} = 10V, I_D = 18 A V_{GS} = 4.5 V, I_D = 16 A V_{GS} = 10 V, I_D = 18 A ,T_J =125 °C	Q2		2.5 2.9 3.6	3.01 3.67 4.33	
g_{FS}	Forward Transconductance	V_{DS} = 5 V, I_D = 18 A V_{DS} = 5 V, I_D = 18 A	Q1 Q2		133 124		S
Dynamic Characteristics							
C_{iss}	Input Capacitance	Q1: V_{DS} = 13 V, V_{GS} = 0 V, f = 1 MHZ Q2: V_{DS} = 13 V, V_{GS} = 0 V, f = 1 MHZ	Q1 Q2		2385 2385	3340 3340	pF
C_{oss}	Output Capacitance		Q1 Q2		612 612	860 860	pF
C_{rss}	Reverse Transfer Capacitance		Q1 Q2		78 78	130 130	pF
R_g	Gate Resistance		Q1 Q2	0.1 0.1	0.6 0.6	1.8 1.8	Ω
Switching Characteristics							
$t_{d(on)}$	Turn-On Delay Time	Q1: V_{DD} = 13V, I_D = 18 A, R_{GEN} = 6 Ω Q2: V_{DD} = 13 V, I_D = 18 A, R_{GEN} = 6 Ω	Q1 Q2		10 10	20 20	ns
t_r	Rise Time		Q1 Q2		3 3	10 10	ns
$t_{d(off)}$	Turn-Off Delay Time		Q1 Q2		29 29	46 46	ns
t_f	Fall Time		Q1 Q2		3 3	10 10	ns
Q_g	Total Gate Charge	V_{GS} = 0 V to 10 V Q1 V_{DD} = 13 V, I_D = 18 A Q2 V_{DD} = 13 V, I_D = 18 A	Q1 Q2		36 36	51 51	nC
Q_g	Total Gate Charge	V_{GS} = 0 V to 4.5 V	Q1 Q2		17 17	24 24	nC
Q_{gs}	Gate to Source Gate Charge		Q1 Q2		5.3 5.3		nC
Q_{gd}	Gate to Drain “Miller” Charge		Q1 Q2		3.9 3.9		nC

Electrical Characteristics T_J = 25 °C unless otherwise noted.

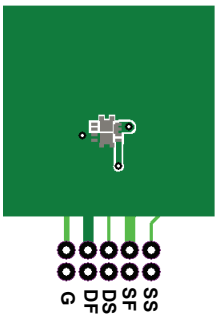
Symbol	Parameter	Test Conditions	Type	Min.	Typ.	Max.	Units
Drain-Source Diode Characteristics							
V_{SD}	Source to Drain Diode Forward Voltage	V_{GS} = 0 V, I_S = 18 A (Note 2) V_{GS} = 0 V, I_S = 18 A (Note 2)	Q1 Q2		0.8 0.8	1.2 1.2	V
I_S	Diode continuous forward current	T_C = 25 °C	Q1 Q2		74 74		A
$I_{S,Pulse}$	Diode pulse current		Q1 Q2		349 349		A
t_{rr}	Reverse Recovery Time	Q1 I_F = 18 A, di/dt = 100 A/µs	Q1 Q2		35 35	56 56	ns
Q_{rr}	Reverse Recovery Charge	Q2 I_F = 18 A, di/dt = 100 A/µs	Q1 Q2		19 19	35 35	nC

Notes:

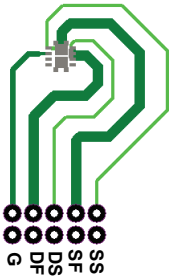
1.$R_{\theta JA}$ is determined with the device mounted on a 1 in^2 pad 2 oz copper pad on a 1.5 x 1.5 in. board of FR-4 material. $R_{\theta CA}$ is determined by the user's board design.



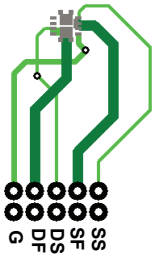
a. 70 °C/W when mounted on a 1 in^2 pad of 2 oz copper



b. 70 °C/W when mounted on a 1 in^2 pad of 2 oz copper



c. 135 °C/W when mounted on a minimum pad of 2 oz copper



d. 135 °C/W when mounted on a minimum pad of 2 oz copper

2. Pulse Test: Pulse Width < 300 µs, Duty cycle < 2.0%.

3. Q1 :E_{AS} of 96 mJ is based on starting T_J = 25 °C; N-ch: L = 3 mH, I_{AS} = 8 A, V_{DD} = 25 V, V_{GS} = 10 V. 100% test at L= 0.1 mH, I_{AS} = 26 A.
Q2: E_{AS} of 96 mJ is based on starting T_J = 25 °C; N-ch: L = 3 mH, I_{AS} = 8 A, V_{DD} = 25 V, V_{GS} = 10 V. 100% test at L= 0.1 mH, I_{AS} = 26 A.

4. Pulse Id refers to Figure.11 & Figure. 26 Forward Bias Safe Operation Area.

5. Computed continuous current limited to Max Junction Temperature only, actual continuous current will be limited by thermal & electro-mechanical application board design.

Typical Characteristics (Q1 N-Channel) T_J = 25°C unless otherwise noted.

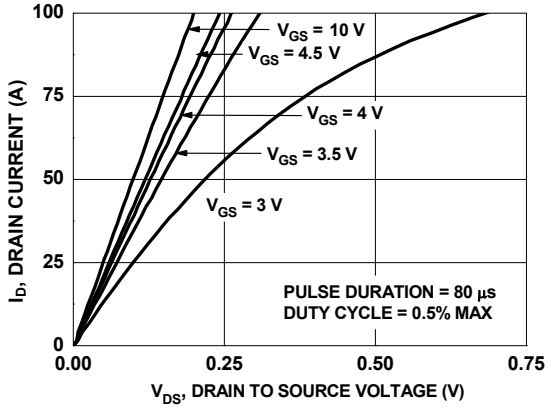


Figure 1. On Region Characteristics

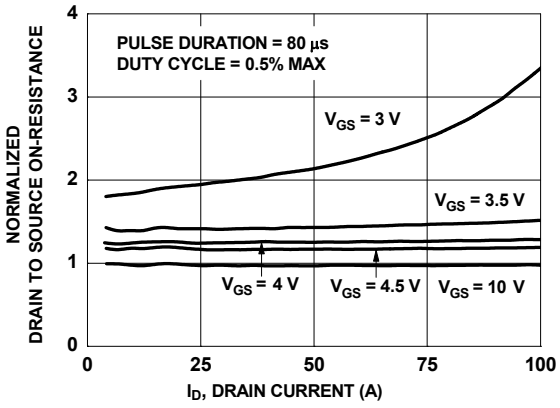


Figure 2. Normalized On-Resistance vs. Drain Current and Gate Voltage

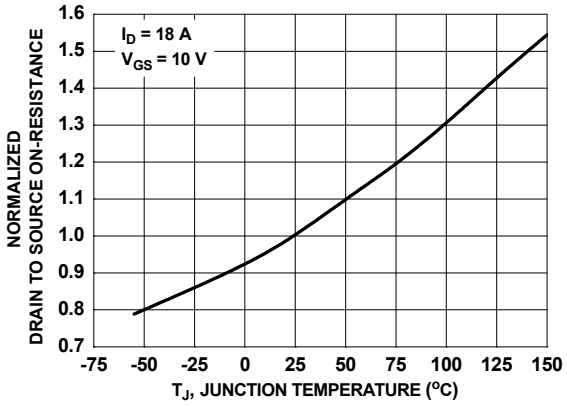


Figure 3. Normalized On Resistance vs. Junction Temperature

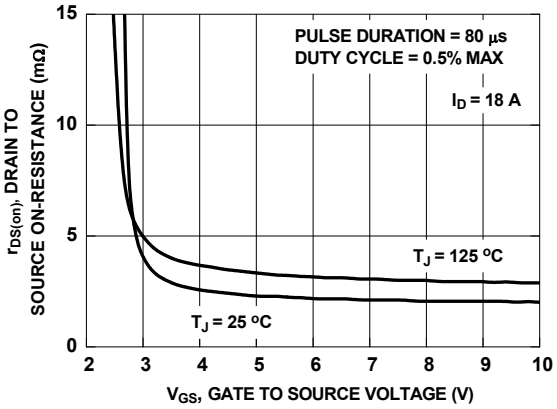


Figure 4. On-Resistance vs. Gate to Source Voltage

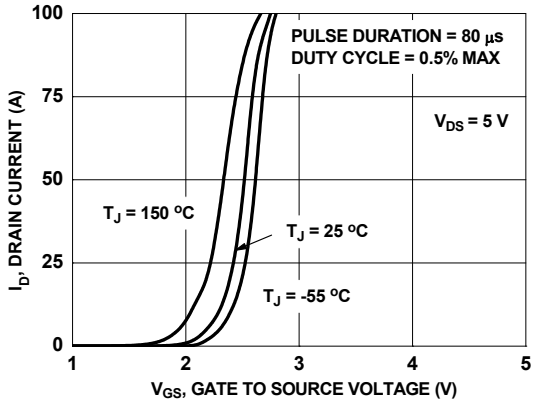


Figure 5. Transfer Characteristics

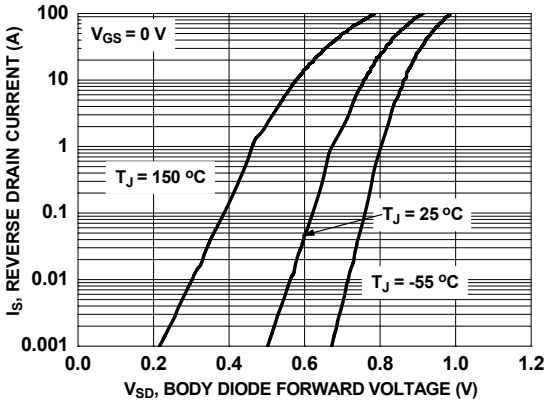


Figure 6. Source to Drain Diode Forward Voltage vs. Source Current

Typical Characteristics (Q1 N-Channel) T_J = 25°C unless otherwise noted.

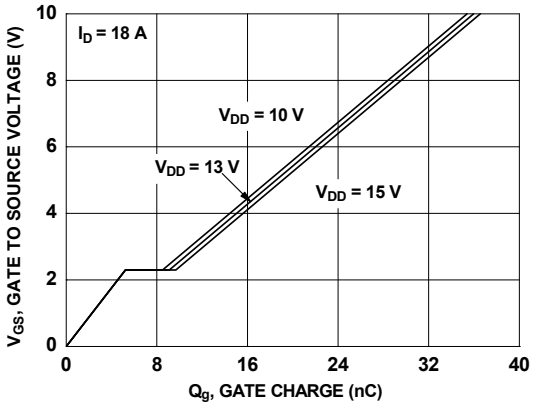


Figure 7. Gate Charge Characteristics

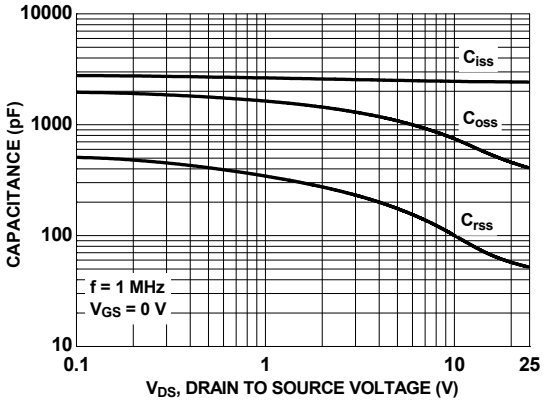


Figure 8. Capacitance vs. Drain to Source Voltage

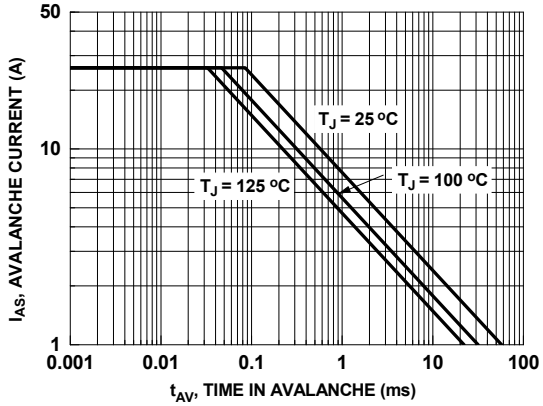


Figure 9. Unclamped Inductive Switching Capability

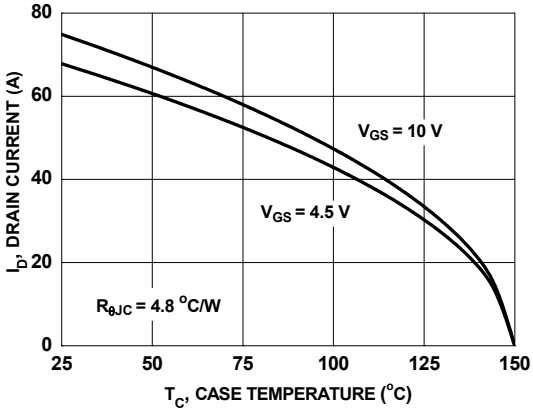


Figure 10. Maximum Continuous Drain Current vs. Case Temperature

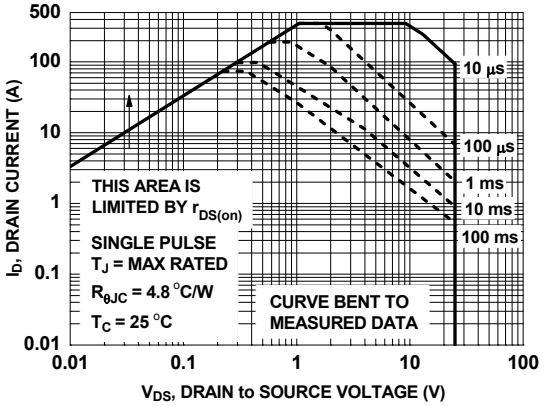


Figure 11. Forward Bias Safe Operating Area

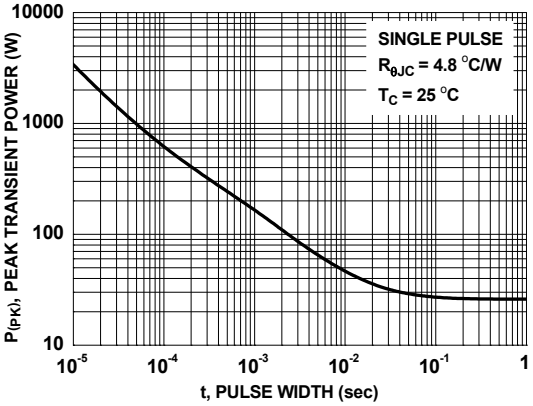


Figure 12. Single Pulse Maximum Power Dissipation

Typical Characteristics (Q1 N-Channel) T_J = 25°C unless otherwise noted.

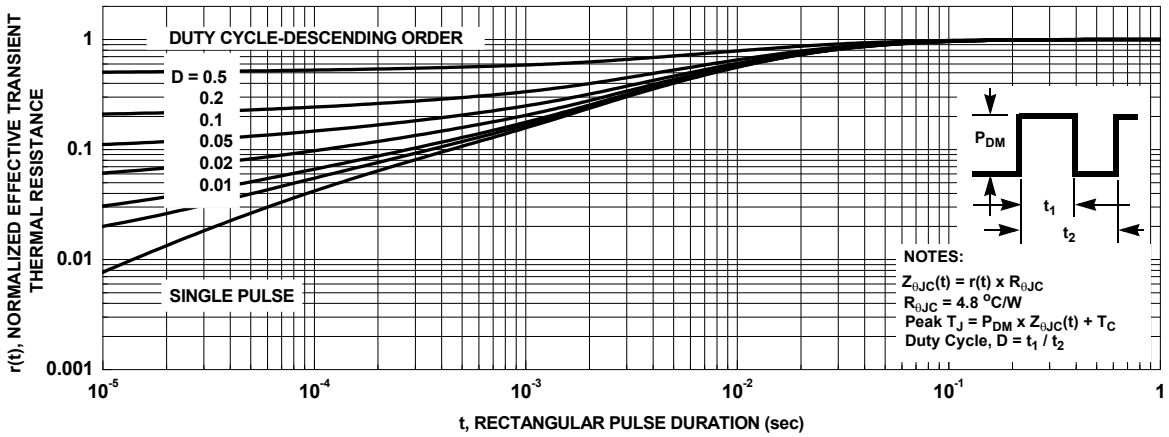


Figure 13. Junction-to-Case Transient Thermal Response Curve

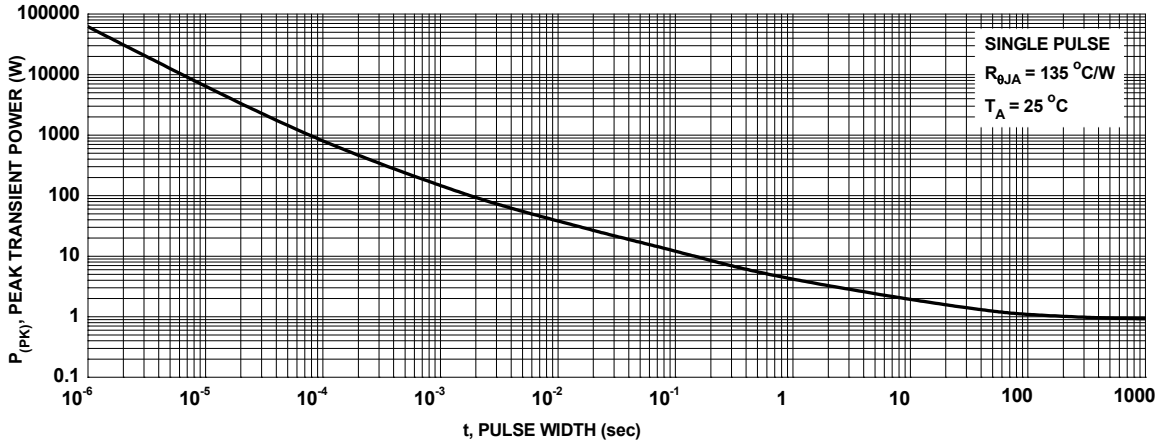


Figure 14. Single Pulse Maximum Power Dissipation

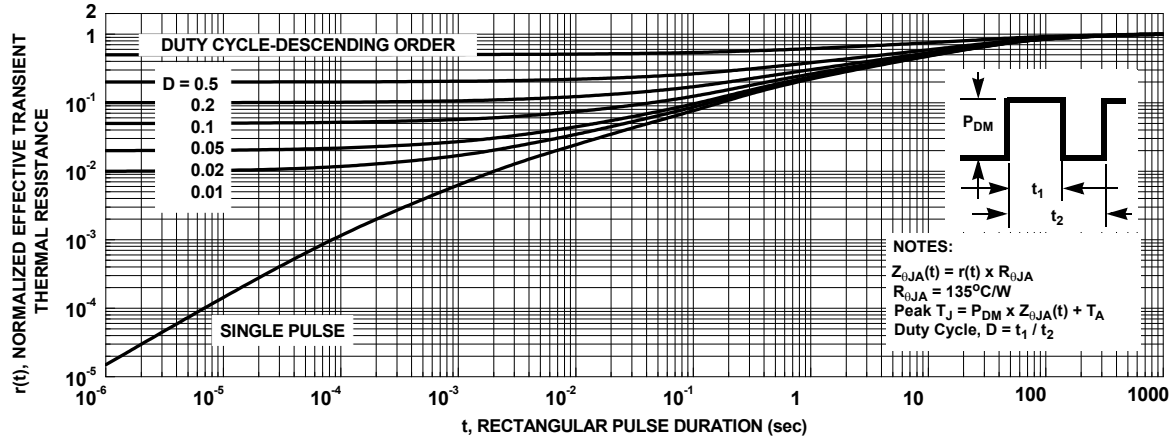


Figure 15. Junction-to-Ambient Transient Thermal Response Curve

Typical Characteristics (Q2 N-Channel) T_J = 25 °C unless otherwise noted.

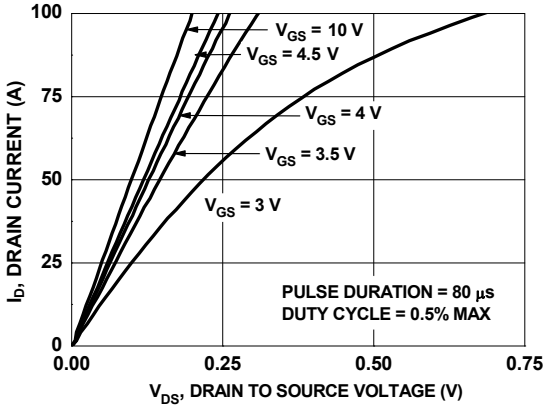


Figure 16. On- Region Characteristics

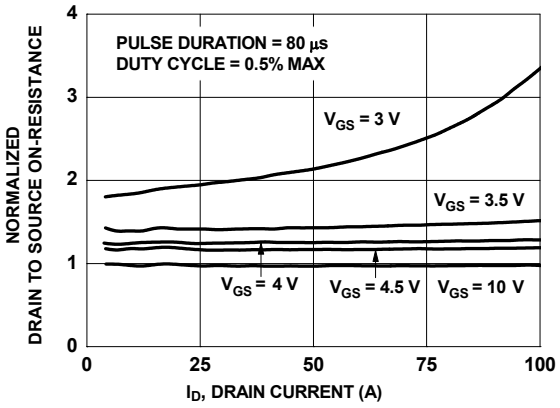


Figure 17. Normalized on-Resistance vs. Drain Current and Gate Voltage

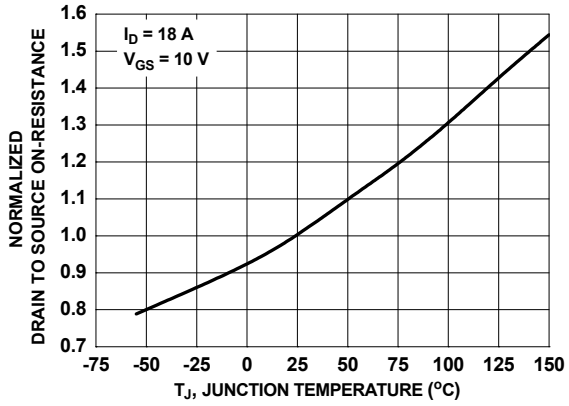


Figure 18. Normalized On-Resistance vs. Junction Temperature

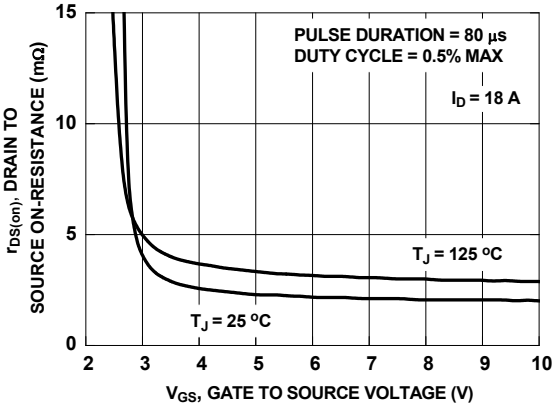


Figure 19. On-Resistance vs. Gate to Source Voltage

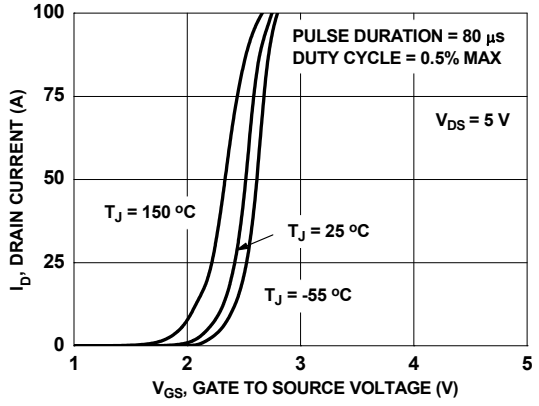


Figure 20. Transfer Characteristics

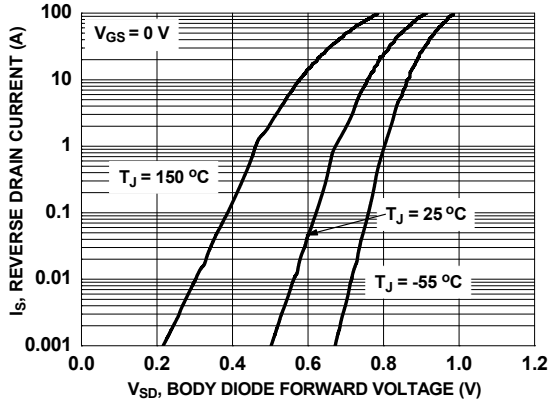


Figure 21. Source to Drain Diode Forward Voltage vs. Source Current

Typical Characteristics (Q2 N-Channel) T_J = 25°C unless otherwise noted.

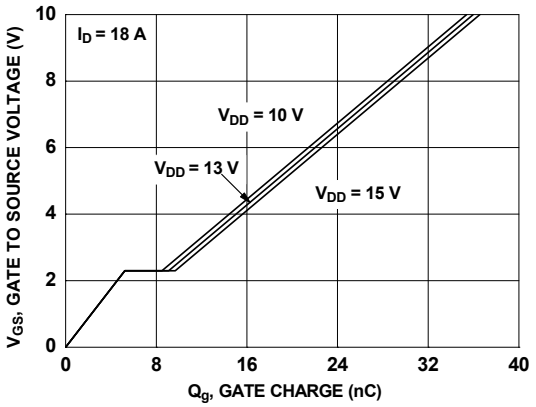


Figure 22. Gate Charge Characteristics

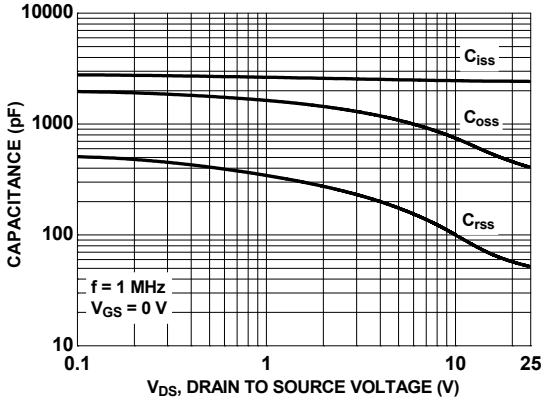


Figure 23. Capacitance vs. Drain to Source Voltage

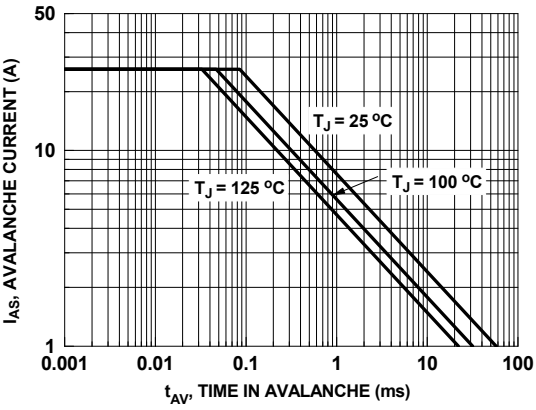


Figure 24. Unclamped Inductive Switching Capability

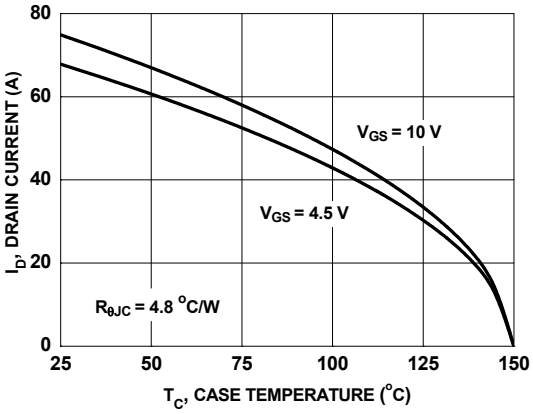


Figure 25. Maximum Continuous Drain Current vs. Case Temperature

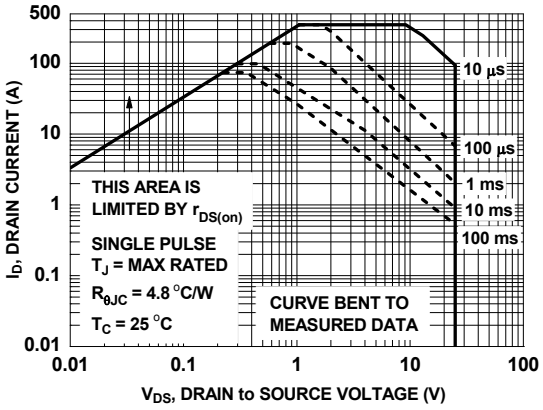


Figure 26. Forward Bias Safe Operating Area

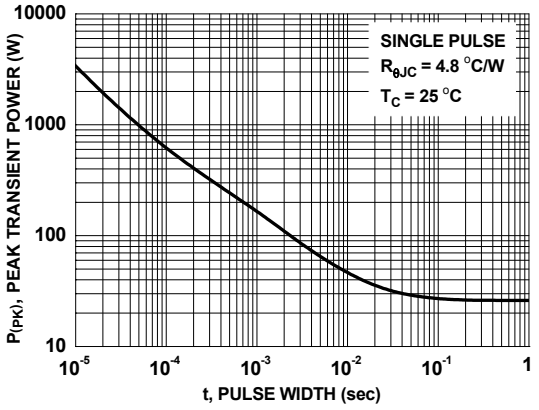


Figure 27. Single Pulse Maximum Power Dissipation

Typical Characteristics (Q2 N-Channel) T_J = 25 °C unless otherwise noted.

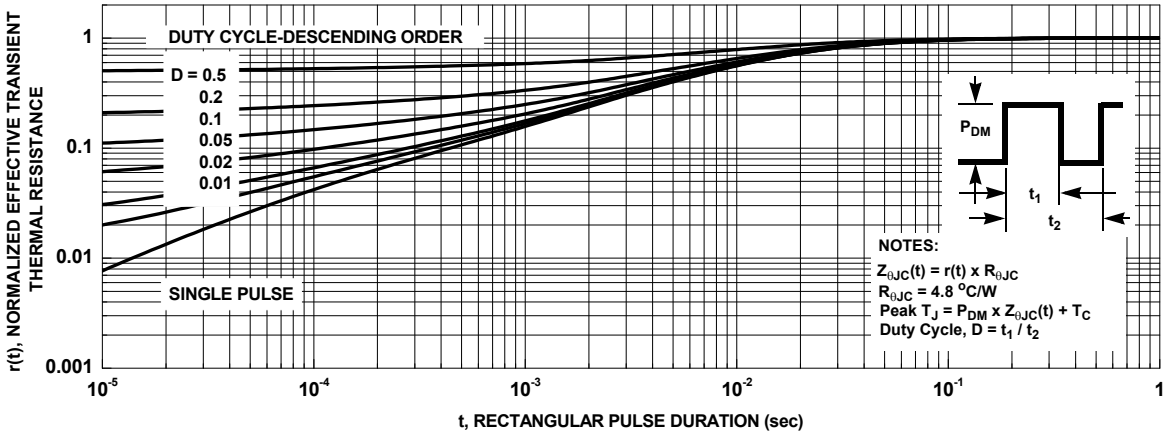


Figure 28. Junction-to-Case Transient Thermal Response Curve

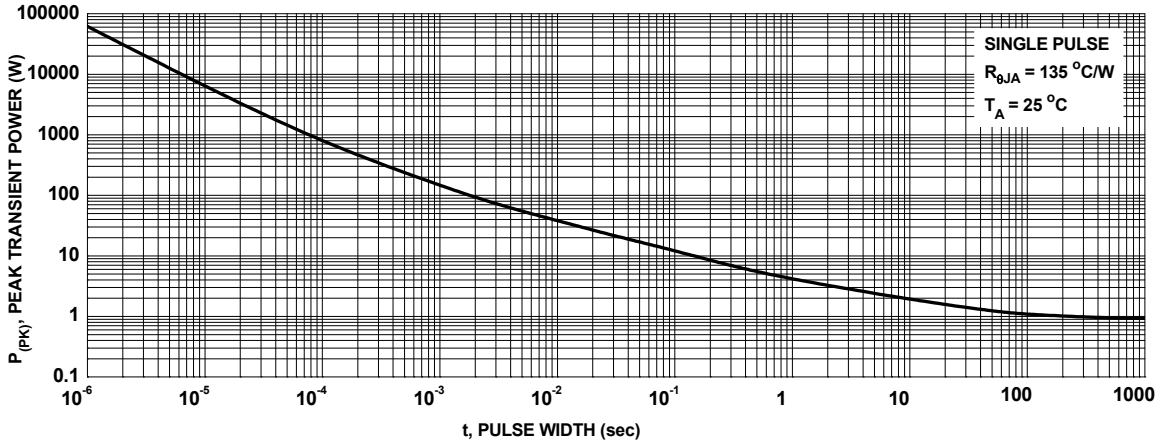


Figure 29. Single Pulse Maximum Power Dissipation

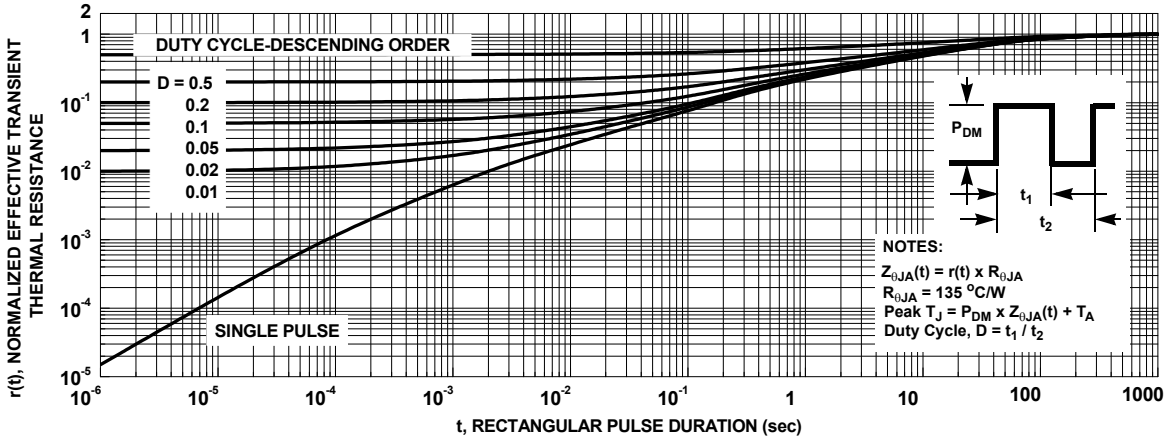
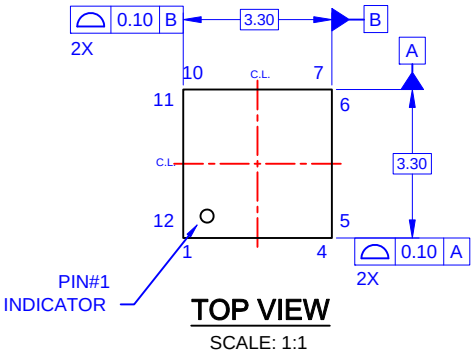
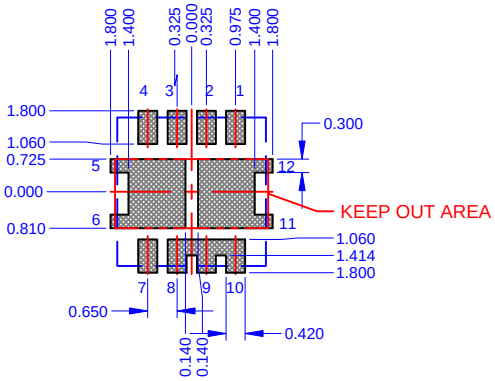


Figure 30. Junction-to-Ambient Transient Thermal Response Curve



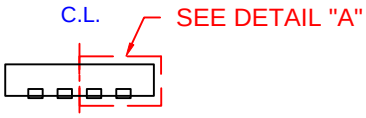
TOP VIEW

SCALE: 1:1



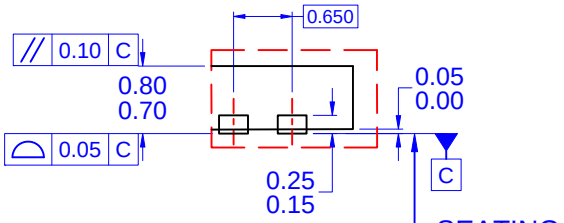
LAND PATTERN RECOMMENDATION

SCALE 1:1



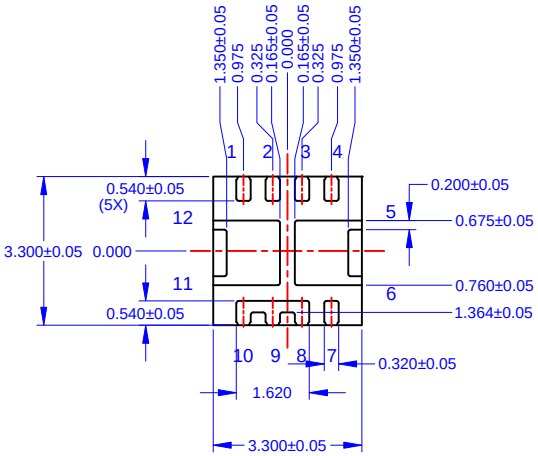
FRONT VIEW

SCALE: 1:1



DETAIL 'A'

SCALE: 2:1



BOTTOM VIEW

SCALE: 1:1

NOTES: UNLESS OTHERWISE SPECIFIED

A) DRAWING DOES NOT FULLY CONFORM TO JEDEC REGISTRATION MO-220, VARIATION WEEC-1
B) ALL DIMENSIONS ARE IN MILLIMETERS.
C) DIMENSIONS DO NOT INCLUDE BURRS OR MOLD FLASH. MOLD FLASH OR BURRS DOES NOT EXCEED 0.10MM.
D) DRAWING FILE NAME: MKT-PQFN12A_REV1

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