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# FDP8D5N10C / FDPF8D5N10C

# N-Channel Shielded Gate PowerTrench<sup>®</sup> MOSFET 100 V, 76 A, 8.5 m $\Omega$

#### **Features**

- Max  $r_{DS(on)}$  = 8.5 m $\Omega$  at  $V_{GS}$  = 10 V,  $I_D$  = 76 A
- Extremely Low Reverse Recovery Charge, Qrr
- 100% UIL Tested
- RoHS Compliant

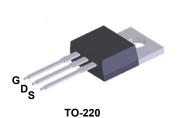
#### **General Description**

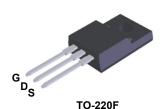
This N-Channel MV MOSFET is produced using ON Semiconductor's advanced PowerTrench® process that incorporates Shielded Gate technology. This process has been optimized to minimize on-state resistance and yet maintain superior switching performance with best in class soft body diode.

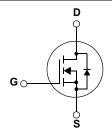
# **Applications**

- Synchronous Rectification for ATX / Server / Telecom PSU
- Motor drives and Uninterruptible Power Supplies
- Micro Solar Inverter









## **MOSFET Maximum Ratings** $T_C = 25$ °C unless otherwise noted.

Symbol	Doromotor		Rat	Unito		
Symbol	Parameter			FDP8D5N10C	FDPF8D5N10C	Units
V <sub>DS</sub>	Drain to Source Voltage			100	100	V
V <sub>GS</sub>	Gate to Source Voltage			±20	±20	V
I <sub>D</sub>	Drain Current -Continuous	T <sub>C</sub> = 25°C	(Note 3)	76	76*	
	-Continuous	T <sub>C</sub> = 100°C	(Note 3)	54	54*	Α
	-Pulsed	-	(Note 1)	304	304*	
E <sub>AS</sub>	Single Pulse Avalanche Energy		(Note 2)	181		mJ
	Power Dissipation	T <sub>C</sub> = 25°C		107	35	W
$P_D$	Power Dissipation	T <sub>A</sub> = 25°C		2.4	2.4	VV
T <sub>J</sub> , T <sub>STG</sub>	Operating and Storage Junction	Temperature Range		-55 to +175	-55 to +175	°C
	nited by maximum junction temperature.					1

## **Thermal Characteristics**

Symbol	Parameter	FDP8D5N10C	FDPF8D5N10C	Units
$R_{\theta JC}$	Thermal Resistance, Junction to Case	1.4	4.2	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	62.5	62.5	C/VV

#### **Package Marking and Ordering Information**

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
FDP8D5N10C	FDP8D5N10C	TO-220	-	-	50 units
FDPF8D5N10C	FDPF8D5N10C	TO-220F	-	-	50 units

# **Electrical Characteristics** $T_J = 25$ °C unless otherwise noted.

Symbol	Parameter	Test Conditions	Min.	Тур.	Max.	Units
Off Chara	acteristics					
$BV_{DSS}$	Drain to Source Breakdown Voltage	$I_D = 250 \mu A, V_{GS} = 0 V$	100			V
$\frac{\Delta BV_{DSS}}{\Delta T_{J}}$	Breakdown Voltage Temperature Coefficient	I <sub>D</sub> = 250 μA, referenced to 25 °C		57		mV/°C
L	Zero Gate Voltage Drain Current	V <sub>DS</sub> = 80 V, V <sub>GS</sub> = 0 V			1	μΑ
I <sub>DSS</sub>		V <sub>DS</sub> = 80 V, T <sub>J</sub> = 150°C			500	μΑ
I <sub>GSS</sub>	Gate to Source Leakage Current	$V_{GS} = \pm 20 \text{ V}, V_{DS} = 0 \text{ V}$			±100	nA

#### **On Characteristics**

V <sub>GS(th)</sub>	Gate to Source Threshold Voltage	$V_{GS} = V_{DS}, I_{D} = 130 \mu A$	2.0	3.0	4.0	٧
r <sub>DS(on)</sub>	Static Drain to Source On Resistance	$V_{GS} = 10 \text{ V}, I_D = 76 \text{ A}$		7.4	8.5	mΩ
9 <sub>FS</sub>	Forward Transconductance	V <sub>DS</sub> = 5 V, I <sub>D</sub> = 76 A		68		S

#### **Dynamic Characteristics**

C <sub>iss</sub>	Input Capacitance	V <sub>DS</sub> = 50 V, V <sub>GS</sub> = 0 V, f = 1 MHz		1765	2475	pF
C <sub>oss</sub>	Output Capacitance			1010	1415	pF
C <sub>rss</sub>	Reverse Transfer Capacitance			16	25	pF
$R_g$	Gate Resistance		0.1	0.8	1.6	Ω

#### **Switching Characteristics**

t <sub>d(on)</sub>	Turn-On Delay Time		12	22	ns
t <sub>r</sub>	Rise Time	V <sub>DD</sub> = 50 V, I <sub>D</sub> = 76 A,	11	20	ns
t <sub>d(off)</sub>	Turn-Off Delay Time	$V_{GS}$ = 10 V, $R_{GEN}$ = 6 $\Omega$	18	28	ns
t <sub>f</sub>	Fall Time		4	10	ns
Qg	Total Gate Charge	V <sub>GS</sub> = 0 V to 10 V V <sub>DD</sub> = 50 V,	25	34	nC
Q <sub>gs</sub>	Gate to Source Gate Charge	V <sub>DD</sub> = 50 V, I <sub>D</sub> = 76 A	9		nC
$Q_{gd}$	Gate to Drain "Miller" Charge	10 - 70 A	5		nC
Q <sub>oss</sub>	Output Charge	V <sub>DD</sub> = 50 V, V <sub>GS</sub> = 0 V	68		nC

#### **Drain-Source Diode Characteristic**

I <sub>S</sub>	Maximum Continuous Drain to Source Diode Forward Current		-	-	76	Α
I <sub>SM</sub>	Maximum Pulsed Drain to Source Diode Forward Current		-	-	304	Α
$V_{SD}$	Source to Drain Diode Forward Voltage	V <sub>GS</sub> = 0 V, I <sub>S</sub> = 76 A		1.0	1.3	V
t <sub>rr</sub>	Reverse Recovery Time	V <sub>GS</sub> = 0 V, V <sub>DD</sub> = 50 V, I <sub>F</sub> = 76 A,		58	92	ns
$Q_{rr}$	Reverse Recovery Charge	dI <sub>F</sub> /dt = 100 A/μs		53	85	nC
t <sub>rr</sub>	Reverse Recovery Time	V <sub>GS</sub> = 0 V, V <sub>DD</sub> = 50 V, I <sub>F</sub> = 76 A,		51	81	ns
$Q_{rr}$	Reverse Recovery Charge	dI <sub>F</sub> /dt = 300 A/μs		141	226	nC

#### Notes:

- 1. Pulsed Id please refer to Figure 11 & Figure 12 "Forward Bias Safe Operating Area" for more details.
- 2.  $E_{AS}$  of 181 mJ is based on starting  $T_{J}$  = 25  $^{\circ}C$ , L = 3 mH,  $I_{AS}$  = 11 A,  $V_{DD}$  = 100 V,  $V_{GS}$  = 10 V. 100% test at L = 0.3 mH,  $I_{AS}$  = 25 A.
- 3. Computed continuous current limited to Max Junction Temperature only, actual continuous current will be limited by thermal & electro-mechanical application board design.

#### Typical Characteristics T<sub>J</sub> = 25 °C unless otherwise noted.

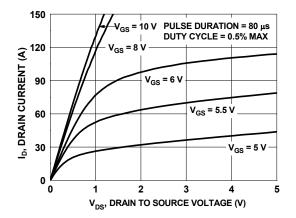


Figure 1. On Region Characteristics

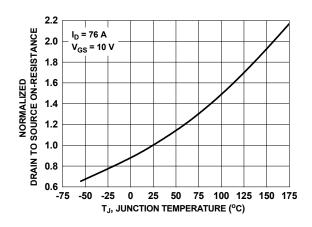


Figure 3. Normalized On Resistance vs. Junction Temperature

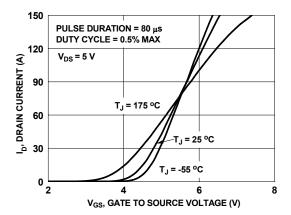


Figure 5. Transfer Characteristics

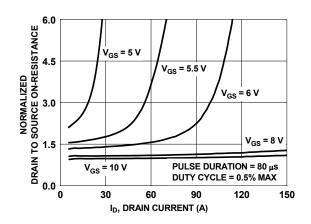


Figure 2. Normalized On-Resistance vs. Drain Current and Gate Voltage

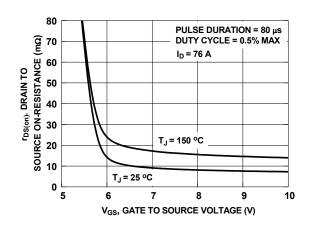


Figure 4. On-Resistance vs. Gate to Source Voltage

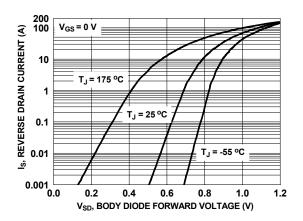


Figure 6. Source to Drain Diode Forward Voltage vs. Source Current

# **Typical Characteristics** $T_J = 25$ °C unless otherwise noted.

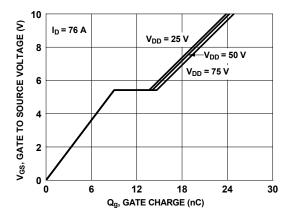


Figure 7. Gate Charge Characteristics

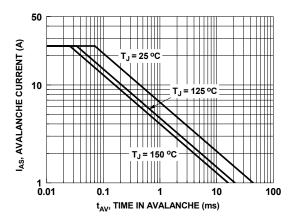


Figure 9. Unclamped Inductive Switching Capability

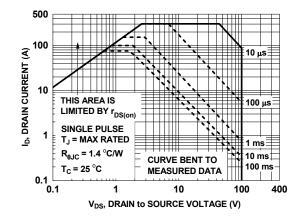


Figure 11. Forward Bias Safe Operating Area for FDP8D5N10C

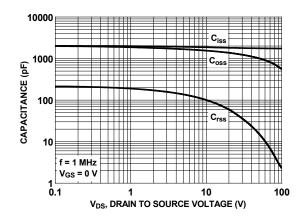


Figure 8. Capacitance vs. Drain to Source Voltage

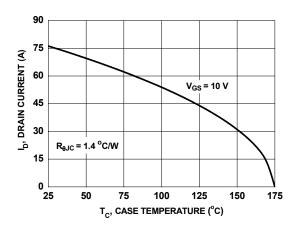


Figure 10. Maximum Continuous Drain Current vs. Case Temperature for FDP8D5N10C

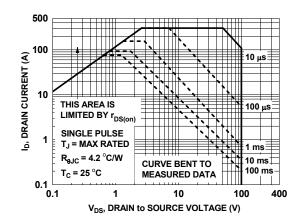
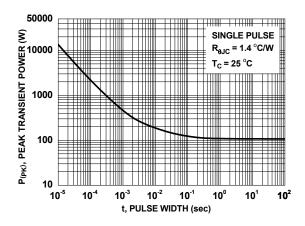


Figure 12. Forward Bias Safe Operating Area for FDPF8D5N10C

#### **Typical Characteristics** $T_J = 25$ °C unless otherwise noted.



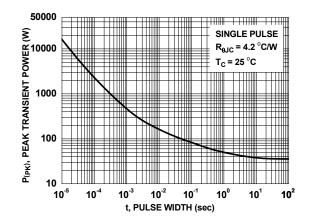


Figure 13. Single Pulse Maximum Power Dissipation for FDP8D5N10C

Figure 14. Single Pulse Maximum Power Dissipation for FDPF8D5N10C

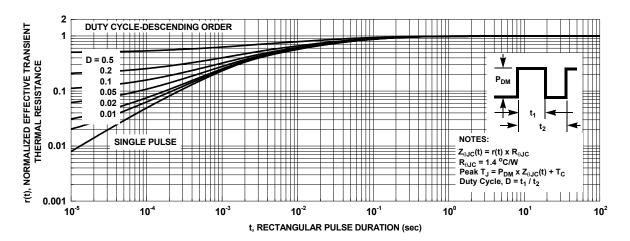


Figure 15. Junction-to-Case Transient Thermal Response Curve for FDP2D3N10C

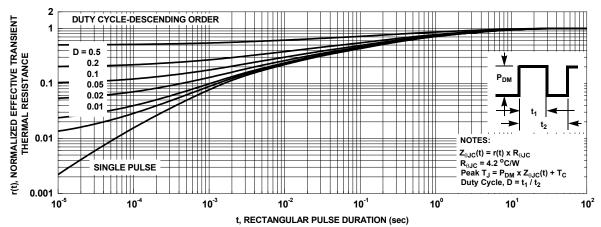
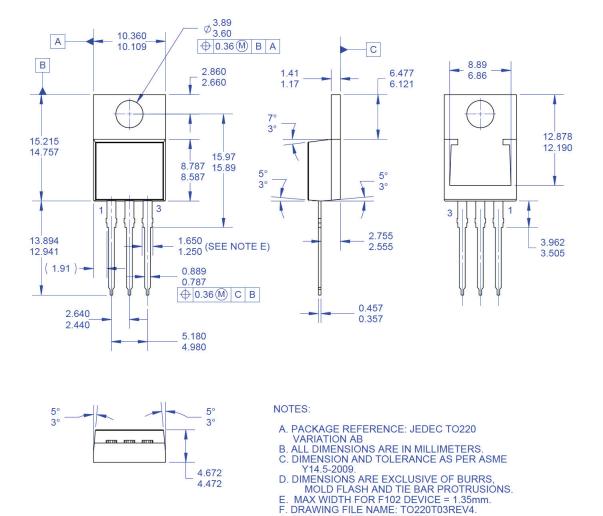


Figure 16. Junction-to-Case Transient Thermal Response Curve for FDPF2D3N10C

### **Dimensional Outline and Pad Layout**



TO-220, Molded, 3-Lead, Jedec Variation AB (Delta)

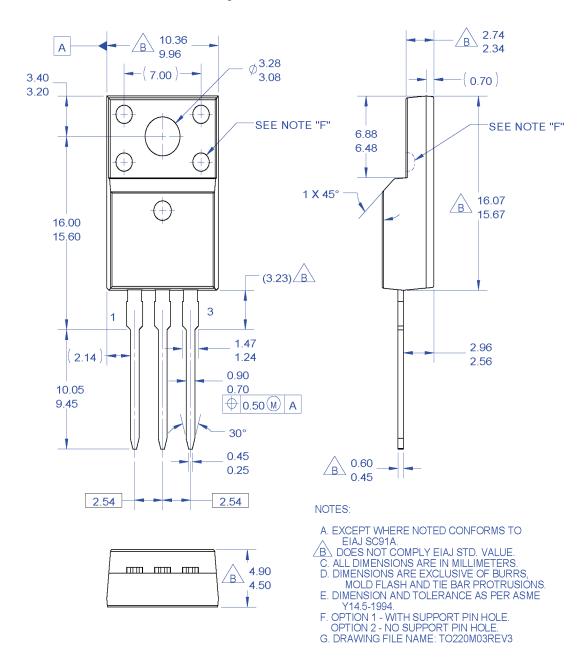
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# **Dimensional Outline and Pad Layout**



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