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FAIRCHILD SEMICONDUCTOR®

July 2013

FDS2572

150V, 0.047 Ohms, 4.9A, N-Channel UltraFET® Trench MOSFET

General Description

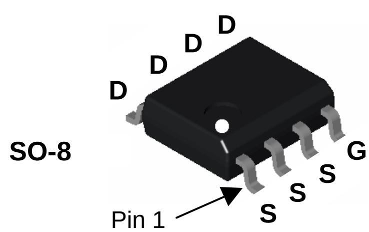
UltraFET® devices combine characteristics that enable benchmark efficiency in power conversion applications. Optimized for Rds(on), low ESR, low total and Miller gate charge, these devices are ideal for high frequency DC to DC converters.

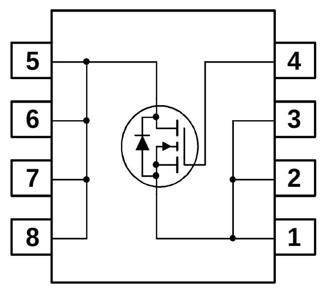
Applications

- DC/DC converters
- Telecom and Data-Com Distributed Power Architectures
- 48-volt I/P Half-Bridge/Full-Bridge
- 24-volt Forward and Push-Pull topologies

Features

- $R_{DS(ON)}$ = 0.040Ω (Typ.), V_{GS} = 10V
- $Q_{g(TOT)}$ = 29nC (Typ.), V_{GS} = 10V
- Low Q_{RR} Body Diode
- Maximized efficiency at high frequencies
- UIS Rated





MOSFET Maximum Ratings T_A=25°C unless otherwise noted

Symbol	Parameter	Ratings	Units
V_{DSS}	Drain to Source Voltage	150	V
V_{GS}	Gate to Source Voltage	±20	V
I_D	Drain Current Continuous (T_C = 25^{o}C, V_{GS} = 10V, $R_{\theta JA}$ = 50 ^{o}C/W)	4.9	A
	Continuous (T_C = 100^{o}C, V_{GS} = 10V, $R_{\theta JA}$ = 50 ^{o}C/W)	3.1	A
	Pulsed	Figure 4	A
P_D	Power dissipation Derate above 25^{o}C	2.5 20	W mW/^{o}C
T_J, T_{STG}	Operating and Storage Temperature	-55 to 150	^{o}C

Thermal Characteristics

$R_{\theta JC}$	Thermal Resistance Junction to Case	(NOTE1)	25	^{o}C/W
$R_{\theta JA}$	Thermal Resistance Junction to Case at 10 seconds	(NOTE2)	50	^{o}C/W
$R_{\theta JA}$	Thermal Resistance Junction to Case at steady state	(NOTE2)	85	^{o}C/W

Package Marking and Ordering Information

Device Marking	Device	Reel Size	Tape Width	Quantity
FDS2572	FDS2572	330mm	12mm	2500units

Electrical Characteristics $T_A = 25°C$ unless otherwise noted

Symbol	Parameter	Test Conditions		Min	Typ	Max	Units
Off Characteristics							
B_{VDSS}	Drain to Source Breakdown Voltage	$I_D = 250\mu A$, $V_{GS} = 0V$		150	-	-	V
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = 120V$		-	-	1	μA
		$V_{GS} = 0V$	$T_C = 150^oC$	-	-	250	
I_{GSS}	Gate to Source Leakage Current	$V_{GS} = \pm 20V$		-	-	±100	nA
On Characteristics							
$V_{GS(TH)}$	Gate to Source Threshold Voltage	$V_{GS} = V_{DS}$, $I_D = 250\mu A$		2	-	4	V
$r_{DS(ON)}$	Drain to Source On Resistance	$I_D = 4.9A$, $V_{GS} = 10V$		-	0.040	0.047	Ω
$r_{DS(ON)}$	Drain to Source On Resistance	$I_D = 4.9A$, $V_{GS} = 6V$		-	0.044	0.053	Ω
Dynamic Characteristics							
C_{ISS}	Input Capacitance	$V_{DS} = 25V$, $V_{GS} = 0V$, f = 1MHz		-	2050	2870	pF
C_{OSS}	Output Capacitance			-	220	310	pF
C_{RSS}	Reverse Transfer Capacitance			-	48	80	pF
R_g	Gate Resistance			0.1	1.3	3.0	Ω
$Q_{g(TOT)}$	Total Gate Charge at 10V	V_{GS}= 0V to 10V	$V_{DD} = 75V$, $I_D = 4.9A$, $I_g = 1.0mA$	-	29	38	nC
$Q_{g(TH)}$	Threshold Gate Charge	V_{GS} = 0V to 2V		-	4	6	nC
Q_{gs}	Gate to Source Gate Charge			-	8	-	nC
Q_{gd}	Gate to Drain “Miller” Charge			-	6	-	nC
Q_{gs2}	Gate Charge Threshold to Plateau			-	4	-	nC
Switching Characteristics							
t_{ON}	Turn-On Time	$V_{DD} = 75V$, $I_D = 4.9A$, $V_{GS} = 10V$, $R_G = 10\Omega$		-	-	27	ns
$t_{d(ON)}$	Turn-On Delay Time			-	14	-	ns
t_r	Rise Time			-	4	-	ns
$t_{d(OFF)}$	Turn-Off Delay Time			-	44	-	ns
t_f	Fall Time			-	22	-	ns
t_{OFF}	Turn-Off Time			-	-	100	ns
Drain-Source Diode Characteristics							
V_{SD}	Source to Drain Diode Voltage	$I_{SD} = 4.9A$		-	-	1.25	V
		$I_{SD} = 3.1A$		-	-	1.0	V
t_{rr}	Reverse Recovery Time	$I_{SD} = 4.9A$, $dI_{SD}/dt = 100A/\mu s$		-	-	72	ns
Q_{RR}	Reverse Recovered Charge	$I_{SD} = 4.9$, $dI_{SD}/dt = 100A/\mu s$		-	-	158	nC

Notes:

1. $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal referance is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.

2. $R_{\theta JA}$ is measured with $1.0in^2$ copper on FR-4 board

Typical Characteristic

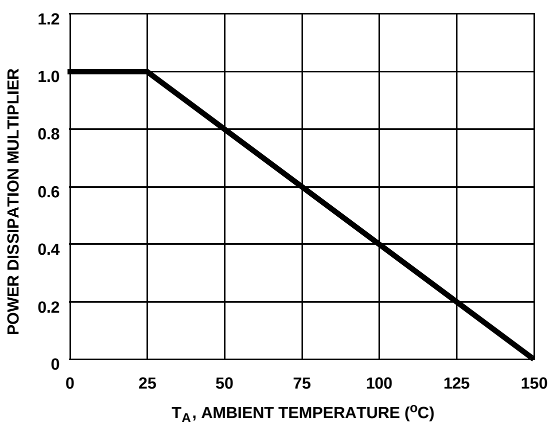


Figure 1. Normalized Power Dissipation vs Ambient Temperature

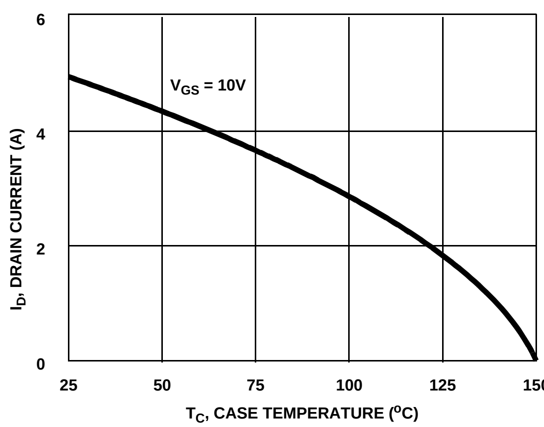


Figure 2. Maximum Continous Drain Current vs Case Temperature

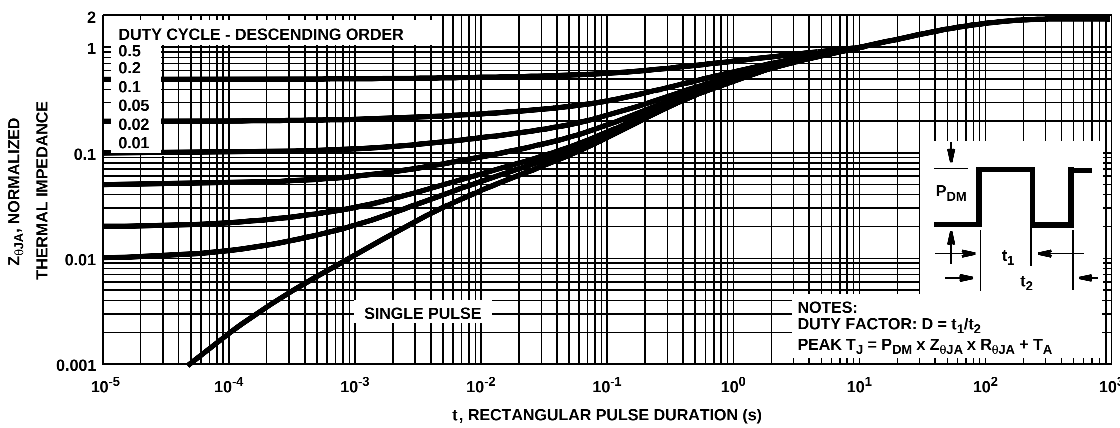


Figure 3. Normalized Maximum Transient Thermal Impedance

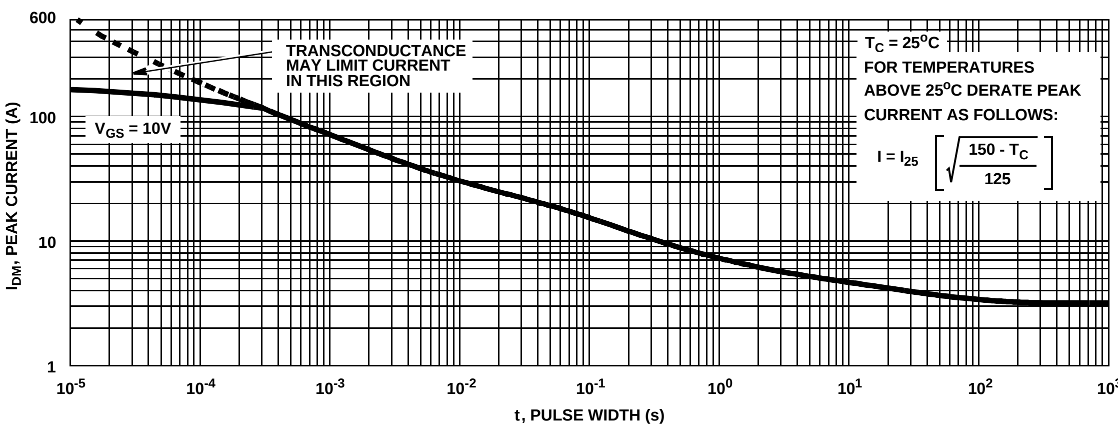


Figure 4. Peak Current Capability

Typical Characteristic (Continued)

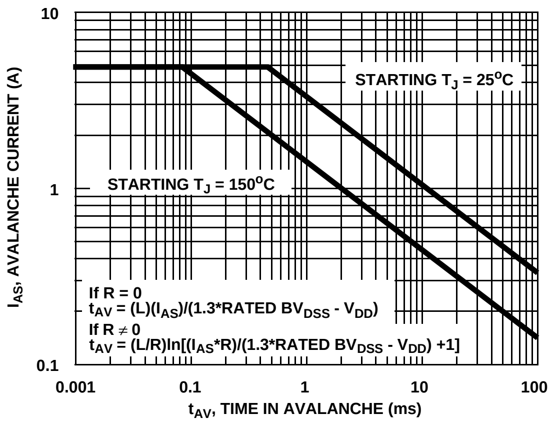


Figure 5. Unclamped Inductive Switching Capability

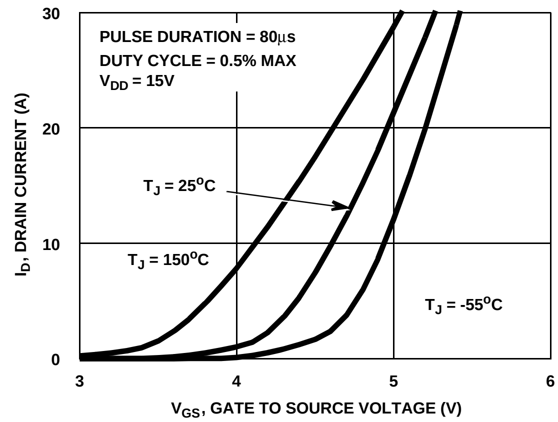


Figure 6. Transfer Characteristics

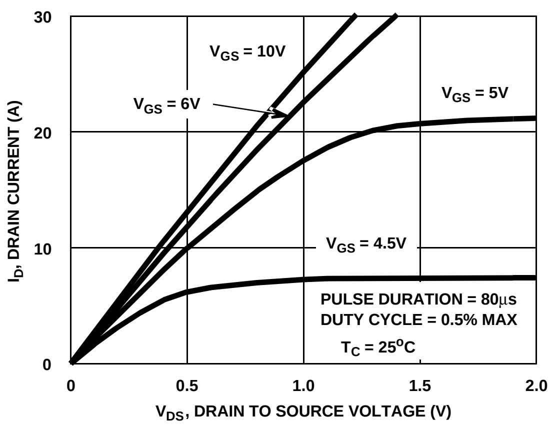


Figure 7. Saturation Characteristics

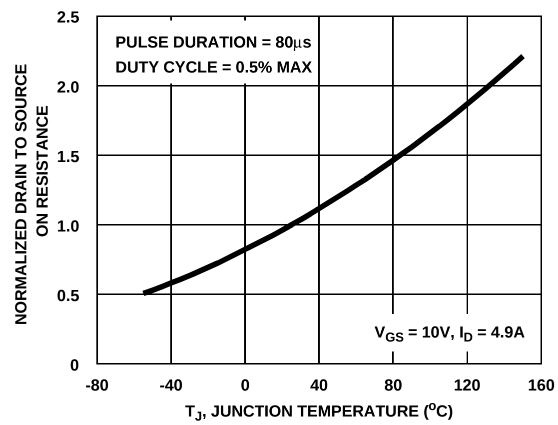


Figure 8. Normalized Drain to Source On Resistance vs Junction Temperature

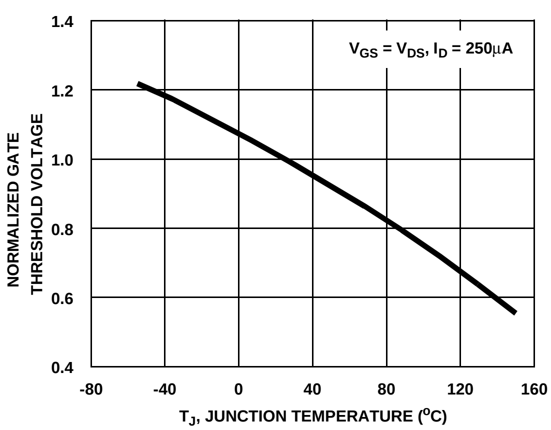


Figure 9. Normalized Gate Threshold Voltage vs Junction Temperature

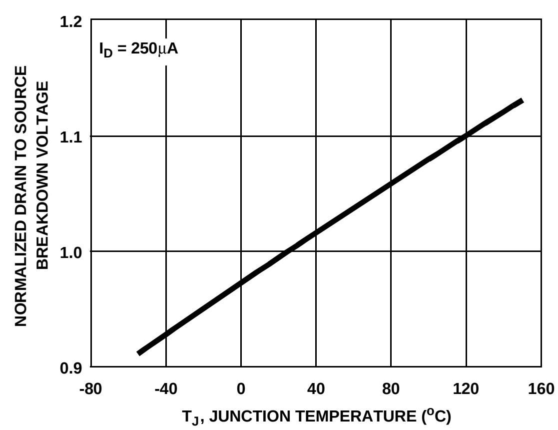


Figure 10. Normalized Drain to Source Breakdown Voltage vs Junction Temperature

Typical Characteristic (Continued)

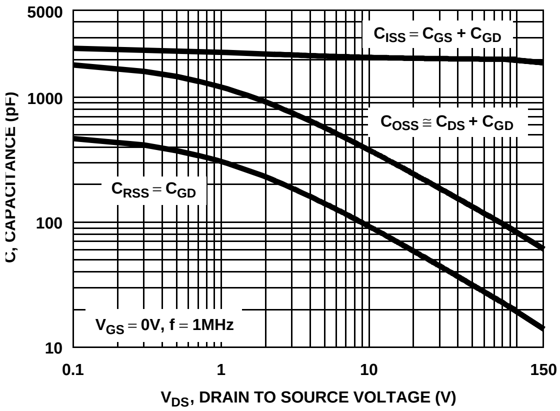


Figure 11. Capacitance vs Drain to Source Voltage

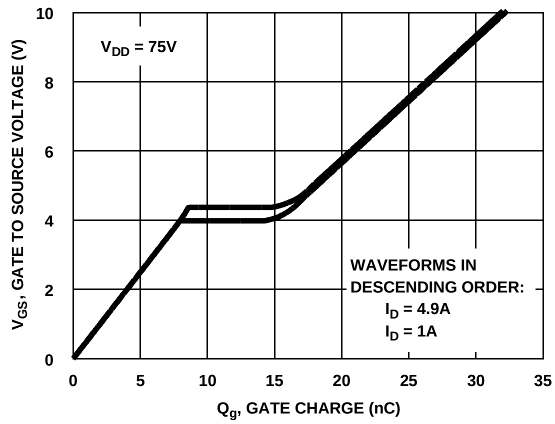


Figure 12. Gate Charge Waveforms for Constant Gate Currents

Test Circuits and Waveforms

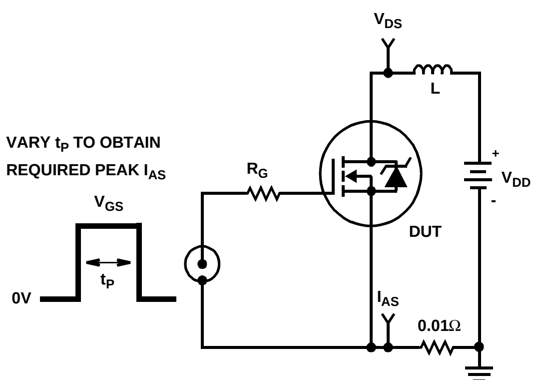


Figure 13. Unclamped Energy Test Circuit

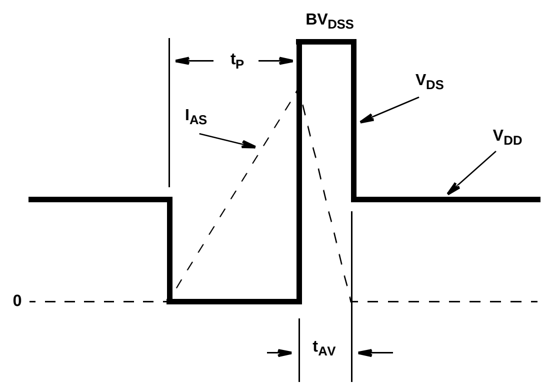


Figure 14. Unclamped Energy Waveforms

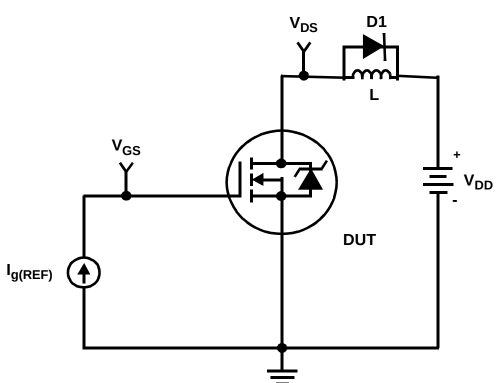


Figure 15. Gate Charge Test Circuit

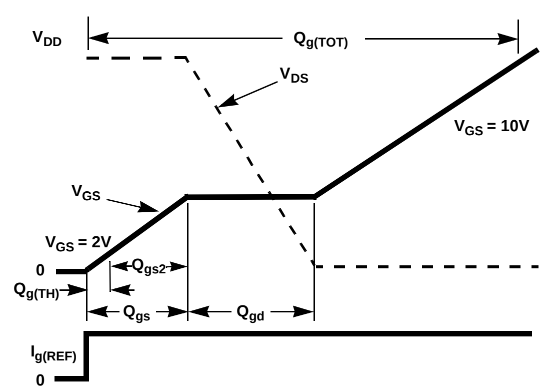


Figure 16. Gate Charge Waveforms

Test Circuits and Waveforms (Continued)

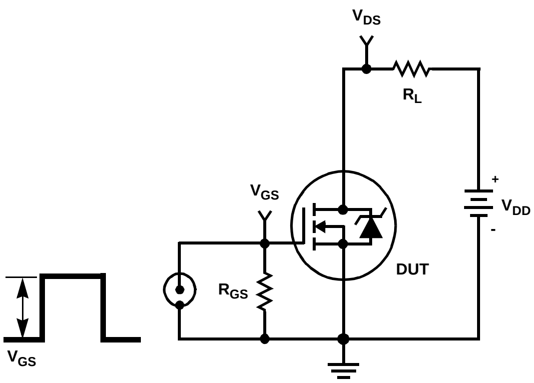


Figure 17. Switching Time Test Circuit

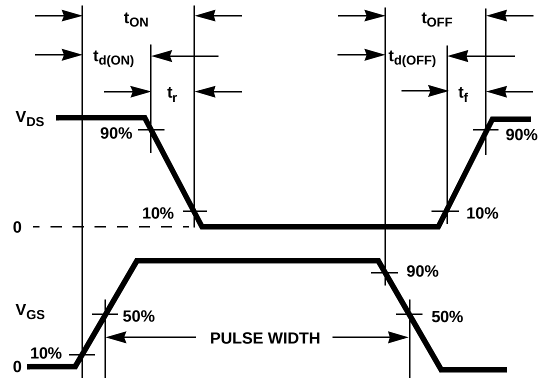


Figure 18. Switching Time Waveforms

Thermal Resistance vs. Mounting Pad Area

The maximum rated junction temperature, T_{JM}, and the thermal resistance of the heat dissipating path determines the maximum allowable device power dissipation, P_{DM}, in an application. Therefore the application's ambient temperature, T_A (^oC), and thermal resistance $R_{\theta JA}$ ($^oC/W$) must be reviewed to ensure that T_{JM} is never exceeded. Equation 1 mathematically represents the relationship and serves as the basis for establishing the rating of the part.

$$P_{DM} = \frac{(T_{JM} - T_A)}{R_{\theta JA}} \qquad \text{(EQ. 1)}$$

In using surface mount devices such as the SO8 package, the environment in which it is applied will have a significant influence on the part's current and maximum power dissipation ratings. Precise determination of P_{DM} is complex and influenced by many factors:

1. Mounting pad area onto which the device is attached and whether there is copper on one side or both sides of the board.
2. The number of copper layers and the thickness of the board.
3. The use of external heat sinks.
4. The use of thermal vias.
5. Air flow and board orientation.
6. For non steady state applications, the pulse width, the duty cycle and the transient thermal response of the part, the board and the environment they are in.

Fairchild provides thermal information to assist the designer's preliminary application evaluation. Figure 19 defines the $R_{\theta JA}$ for the device as a function of the top copper (component side) area. This is for a horizontally positioned FR-4 board with 1oz copper after 1000 seconds of steady state power with no air flow. This graph provides the necessary information for calculation of the steady state junction temperature or power dissipation. Pulse applications can be evaluated using the Fairchild device Spice thermal model or manually utilizing the normalized maximum transient thermal impedance curve.

Thermal resistances corresponding to other copper areas can be obtained from Figure 19 or by calculation using Equation 2. The area, in square inches is the top copper area including the gate and source pads.

$$R_{\theta JA} = 64 + \frac{26}{0.23 + Area} \qquad \text{(EQ. 2)}$$

The transient thermal impedance ($Z_{\theta JA}$) is also effected by varied top copper board area. Figure 20 shows the effect of copper pad area on single pulse transient thermal impedance. Each trace represents a copper pad area in square inches corresponding to the descending list in the graph. Spice and SABER thermal models are provided for each of the listed pad areas.

Copper pad area has no perceivable effect on transient thermal impedance for pulse widths less than 100ms. For pulse widths less than 100ms the transient thermal impedance is determined by the die and package. Therefore, CTHERM1 through CTHERM5 and RTHERM1 through RTHERM5 remain constant for each of the thermal models. A listing of the model component values is available in Table 1.

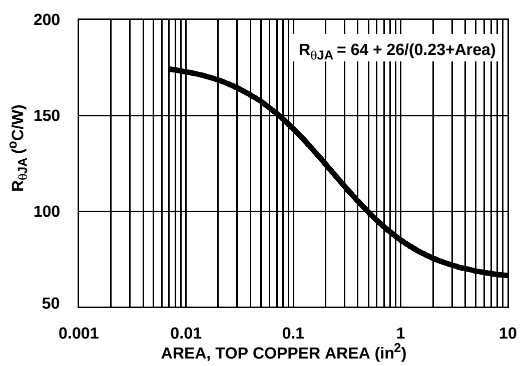


Figure 19. Thermal Resistance vs Mounting Pad Area

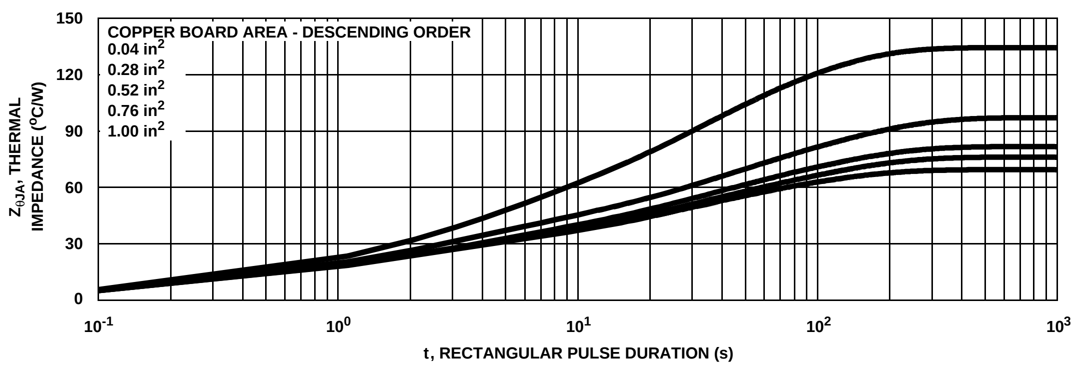
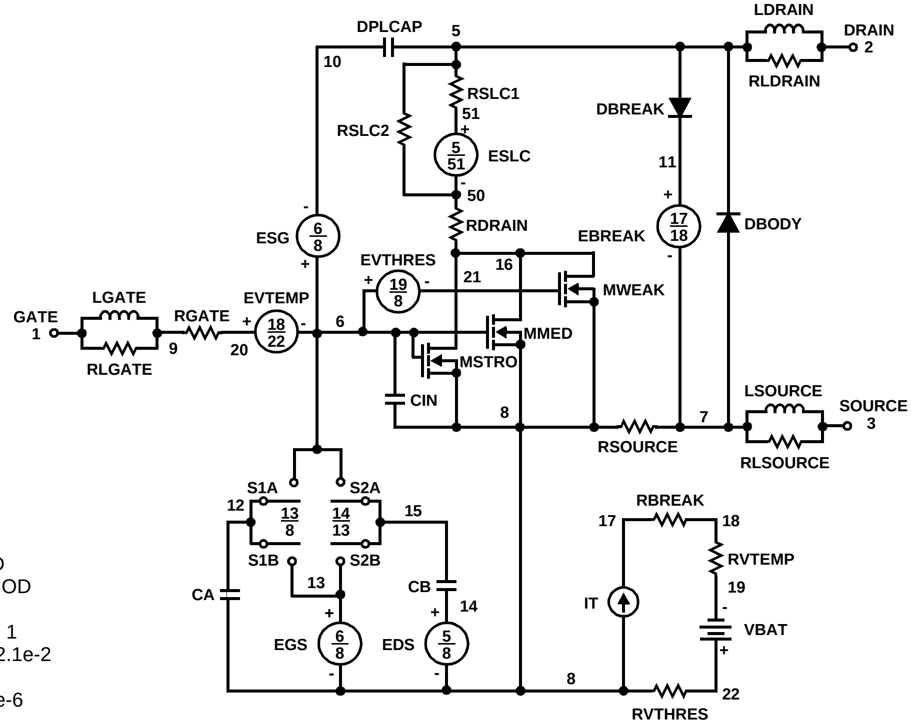


Figure 20. Thermal Impedance vs Mounting Pad Area

PSPICE Electrical Model

```
.SUBCKT FDS2572 2 1 3 ;       rev August 2001
CA  12  8 8e-10
Cb 15 14 8e-10
Cin 6 8 2e-9

Dbody 7 5 DbodyMOD
Dbreak 5 11 DbreakMOD
Dplcap 10 5 DplcapMOD

Ebreak 11 7 17 18 157.4
Eds 14 8 5 8 1
Egs 13 8 6 8 1
Esg 6 10 6 8 1
Evthres 6 21 19 8 1
Evtemp 20 6 18 22 1

It 8 17 1

Lgate 1 9 5.61e-9
Ldrain 2 5 1.0e-9
Lsource 3 7 1.98e-9

RLgate 1 9 56.1
RLdrain 2 5 10
RLsource 3 7 19.8

Mstro 16 6 8 8 MstroMOD
Mmed 16 6 8 8 MmedMOD
Mweak 16 21 8 8 MweakMOD

Rbreak 17 18 RbreakMOD 1
Rdrain 50 16 RdrainMOD 2.1e-2
Rgate 9 20 1.47
RSLC1 5 51 RSLCMOD 1e-6
RSLC2 5 50 1e3
Rsource 8 7 RsourceMOD 1.5e-2
Rvthres 22 8 RvthresMOD 1
Rvtemp 18 19 RvtempMOD 1
S1a 6 12 13 8 S1AMOD
S1b 13 12 13 8 S1BMOD
S2a 6 15 14 13 S2AMOD
S2b 13 15 14 13 S2BMOD

Vbat 22 19 DC 1

ESLC 51 50  VALUE={(V(5,51)/ABS(V(5,51)))*(PWR(V(5,51)/(1e-6*65),3))}

.MODEL DbodyMOD D (IS=4e-11 N=1.131 RS=4.4e-3 TRS1=2e-3 TRS2=1e-6
+ CJO=1.44e-9 M=0.67 TT=7.4e-8 XTI=4.2)
.MODEL DbreakMOD D (RS=0.38 TRS1=2e-3 TRS2=-8.9e-6)
.MODEL DplcapMOD D (CJO=5e-10 IS=1e-30 N=10 M=0.7)

.MODEL MstroMOD NMOS (VTO=4.05 KP=85 IS=1e-30 N=10 TOX=1 L=1u W=1u)
.MODEL MmedMOD NMOS (VTO=3.35 KP=5 IS=1e-30 N=10 TOX=1 L=1u W=1u RG=1.47)
.MODEL MweakMOD NMOS (VTO=2.76 KP=0.05 IS=1e-30 N=10 TOX=1 L=1u W=1u RG=14.7 RS=0.1)

.MODEL RbreakMOD RES (TC1=1.1e-3 TC2=-3e-7)
.MODEL RdrainMOD RES (TC1=1e-2 TC2=3e-5)
.MODEL RSLCMOD RES (TC1=3e-3 TC2=1e-6)
.MODEL RsourceMOD RES (TC1=4.5e-3 TC2=1e-6)
.MODEL RvtempMOD RES (TC1=-5e-3 TC2=2e-6)
.MODEL RvthresMOD RES (TC1=-3e-3 TC2=-1.4e-5)

.MODEL S1AMOD VSWITCH (RON=1e-5 ROFF=0.1 VON=-10 VOFF=-2)
.MODEL S1BMOD VSWITCH (RON=1e-5 ROFF=0.1 VON=-2 VOFF=-10)
.MODEL S2AMOD VSWITCH (RON=1e-5 ROFF=0.1 VON=-0.8 VOFF=0.3)
.MODEL S2BMOD VSWITCH (RON=1e-5 ROFF=0.1 VON=0.3 VOFF=-0.8)
.ENDS
```



Note: For further discussion of the PSPICE model, consult **A New PSPICE Sub-Circuit for the Power MOSFET Featuring Global Temperature Options**; IEEE Power Electronics Specialist Conference Records, 1991, written by William J. Hepp and C. Frank Wheatley.

SABER Electrical Model

REV August 2001
template FDS2572 n2,n1,n3
electrical n2,n1,n3
{
var i iscl
dp..model dbodymod = (isl=4e-11,nl=1.131,rs=4.4e-3,trs1=2e-3,trs2=1e-6,cjo=1.44e-9,m=0.67,tt=7.4e-8,xti=4.2)
dp..model dbreakmod = (rs=0.38,trs1=2e-3,trs2=-8.9e-6)
dp..model dplcapmod = (cjo=5e-10,isl=10e-30,nl=10,m=0.7)
m..model mstrongmod = (type=_n,vto=4.05,kp=85,is=1e-30, tox=1)
m..model mmedmod = (type=_n,vto=3.35,kp=5,is=1e-30, tox=1)
m..model mweakmod = (type=_n,vto=2.76,kp=0.05,is=1e-30, tox=1,rs=0.1)
sw_vcsp..model s1amod = (ron=1e-5,roff=0.1,von=-10,voff=-2)
sw_vcsp..model s1bmod = (ron=1e-5,roff=0.1,von=-2,voff=-10)
sw_vcsp..model s2amod = (ron=1e-5,roff=0.1,von=-0.8,voff=0.3)
sw_vcsp..model s2bmod = (ron=1e-5,roff=0.1,von=0.3,voff=-0.8)
c.ca n12 n8 = 8e-10
c.cb n15 n14 = 8e-10
c.cin n6 n8 = 2e-9

dp.dbody n7 n5 = model=dbodymod
dp.dbreak n5 n11 = model=dbreakmod
dp.dplcap n10 n5 = model=dplcapmod

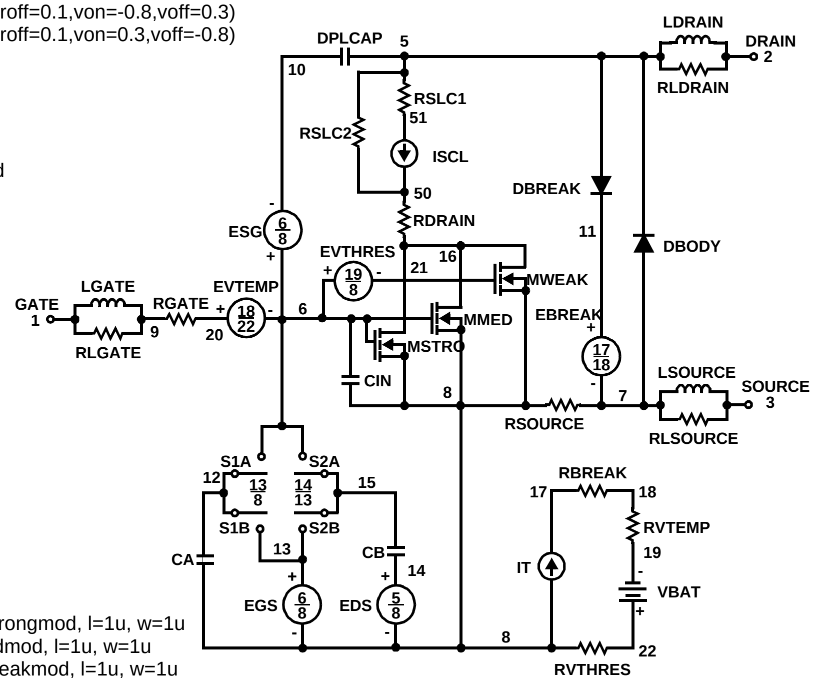
spe.ebreak n11 n7 n17 n18 = 157.4
spe.eds n14 n8 n5 n8 = 1
spe.egs n13 n8 n6 n8 = 1
spe.esg n6 n10 n6 n8 = 1
spe.evthres n6 n21 n19 n8 = 1
spe.evtemp n20 n6 n18 n22 = 1

i.it n8 n17 = 1

l.lgate n1 n9 = 5.61e-9
l.ldrain n2 n5 = 1.0e-9
l.lsource n3 n7 = 1.98e-9

res.rlgate n1 n9 = 56.1
res.rldrain n2 n5 = 10
res.rlsource n3 n7 = 19.8

m.mstrong n16 n6 n8 n8 = model=mstrongmod, l=1u, w=1u
m.mmed n16 n6 n8 n8 = model=mmedmod, l=1u, w=1u
m.mweak n16 n21 n8 n8 = model=mweakmod, l=1u, w=1u



res.rbreak n17 n18 = 1, tc1=1.1e-3,tc2=-3e-7
res.rdrain n50 n16 = 2.1e-2, tc1=1e-2,tc2=3e-5
res.rgate n9 n20 = 1.47
res.rslc1 n5 n51 = 1e-6, tc1=3e-3,tc2=1e-6
res.rslc2 n5 n50 = 1e3
res.rsource n8 n7 = 1.5e-2, tc1=4.5e-3,tc2=1e-6
res.rvthres n22 n8 = 1, tc1=-3e-3,tc2=-1.4e-5
res.rvtemp n18 n19 = 1, tc1=-5e-3,tc2=2e-6
sw_vcsp.s1a n6 n12 n13 n8 = model=s1amod
sw_vcsp.s1b n13 n12 n13 n8 = model=s1bmod
sw_vcsp.s2a n6 n15 n14 n13 = model=s2amod
sw_vcsp.s2b n13 n15 n14 n13 = model=s2bmod

v.vbat n22 n19 = dc=1
equations {
i (n51->n50) +=iscl
iscl: v(n51,n50) = ((v(n5,n51)/(1e-9+abs(v(n5,n51))))*((abs(v(n5,n51)*1e6/65))** 3))
}

SPICE Thermal Model

REV August 2001
FDS2572
Copper Area = 1 in^2

CTHERM1 TH 8 2.0e-3
CTHERM2 8 7 5.0e-3
CTHERM3 7 6 1.0e-2
CTHERM4 6 5 4.0e-2
CTHERM5 5 4 9.0e-2
CTHERM6 4 3 2.0e-1
CTHERM7 3 2 1
CTHERM8 2 TL 3

RTHERM1 TH 8 1.0e-1
RTHERM2 8 7 5.0e-1
RTHERM3 7 6 1
RTHERM4 6 5 5
RTHERM5 5 4 8
RTHERM6 4 3 12
RTHERM7 3 2 18
RTHERM8 2 TL 25

SABER Thermal Model

Copper Area = 1 in^2
template thermal_model th tl
thermal_c th, tl
{
ctherm.ctherm1 th c2 =2.0e-3
ctherm.ctherm2 c2 c3 =5.0e-3
ctherm.ctherm3 c3 c4 =1.0e-2
ctherm.ctherm4 c4 c5 =4.0e-2
ctherm.ctherm5 c5 c6 =9.0e-2
ctherm.ctherm6 c6 c7 =2.0e-1
ctherm.ctherm7 c7 c8 =1
ctherm.ctherm8 c8 tl =3

rtherm.rtherm1 th c2 =1.0e-1
rtherm.rtherm2 c2 c3 =5.0e-1
rtherm.rtherm3 c3 c4 =1
rtherm.rtherm4 c4 c5 =5
rtherm.rtherm5 c5 c6 =8
rtherm.rtherm6 c6 c7 =12
rtherm.rtherm7 c7 c8 =18
rtherm.rtherm8 c8 tl =25
}

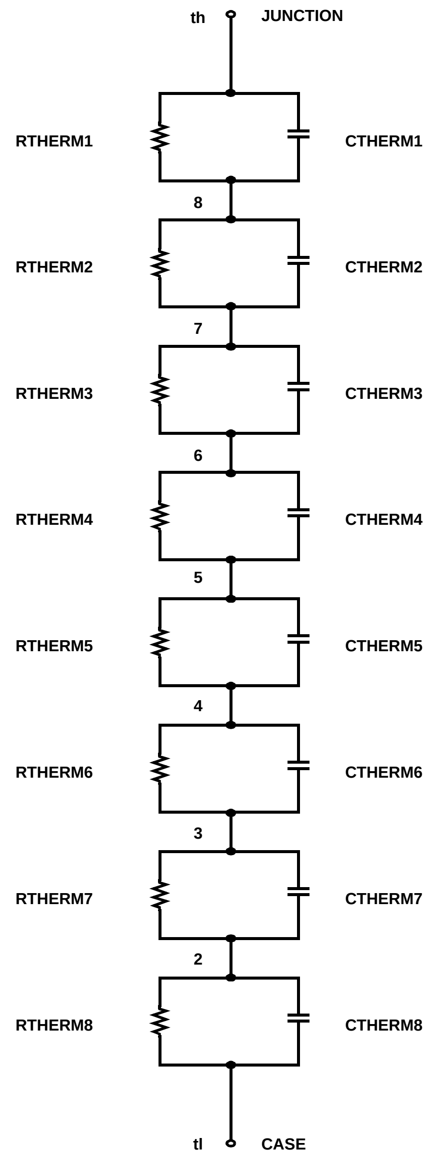
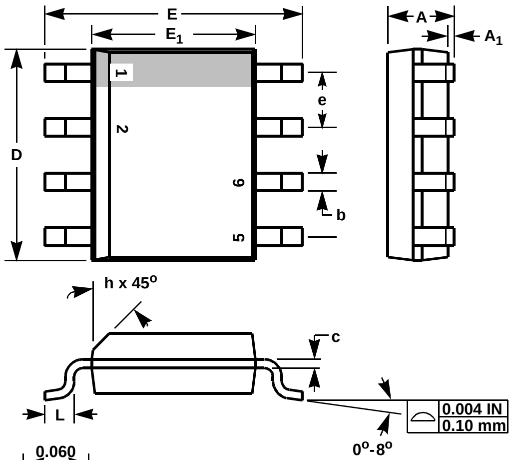


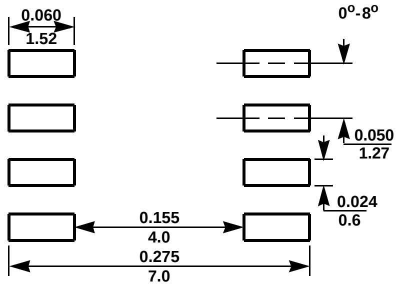
TABLE 1. THERMAL MODELS

COMPONANT	0.04 in^2	0.28 in^2	0.52 in^2	0.76 in^2	1.0 in^2
CTHERM6	1.2e-1	1.5e-1	2.0e-1	2.0e-1	2.0e-1
CTHERM7	0.5	1.0	1.0	1.0	1.0
CTHERM8	1.3	2.8	3.0	3.0	3.0
RTHERM6	26	20	15	13	12
RTHERM7	39	24	21	19	18
RTHERM8	55	38.7	31.3	29.7	25

MS-012AA

8 LEAD JEDEC MS-012AA SMALL OUTLINE PLASTIC PACKAGE





MINIMUM RECOMMENDED FOOTPRINT FOR SURFACE-MOUNTED APPLICATIONS

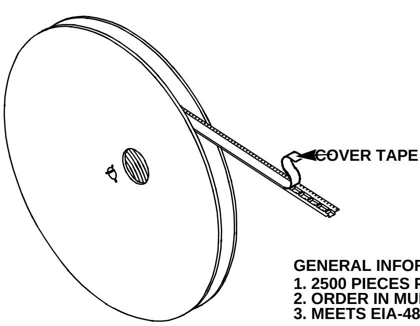
SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.0532	0.0688	1.35	1.75	-
A_1	0.004	0.0098	0.10	0.25	-
b	0.013	0.020	0.33	0.51	-
c	0.0075	0.0098	0.19	0.25	-
D	0.189	0.1968	4.80	5.00	2
E	0.2284	0.244	5.80	6.20	-
E_1	0.1497	0.1574	3.80	4.00	3
e	0.050 BSC		1.27 BSC		-
H	0.0099	0.0196	0.25	0.50	-
L	0.016	0.050	0.40	1.27	4

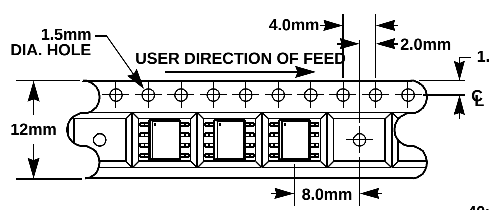
NOTES:

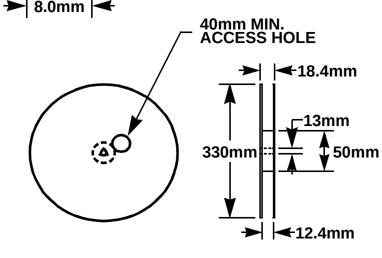
1. All dimensions are within allowable dimensions of Rev. C of JEDEC MS-012AA outline dated 5-90.
2. Dimension “D” does not include mold flash, protrusions or gate burrs. Mold flash, protrusions or gate burrs shall not exceed 0.006 inches (0.15mm) per side.
3. Dimension “E_1” does not include inter-lead flash or protrusions. Inter-lead flash and protrusions shall not exceed 0.010 inches (0.25mm) per side.
4. “L” is the length of terminal for soldering.
5. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
6. Controlling dimension: Millimeter.
7. Revision 8 dated 5-99.

MS-012AA

12mm TAPE AND REEL







GENERAL INFORMATION
1. 2500 PIECES PER REEL.
2. ORDER IN MULTIPLES OF FULL REELS ONLY.
3. MEETS EIA-481 REVISION “A” SPECIFICATIONS.

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Rev. I64

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