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## **FDS6898AZ**

# **Dual N-Channel Logic Level PWM Optimized PowerTrench® MOSFET**

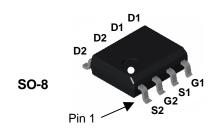
### **General Description**

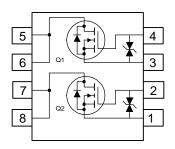
These N-Channel Logic Level MOSFETs are produced using Fairchild Semiconductor's advanced PowerTrench process that has been especially tailored to minimize the on-state resistance and yet maintain superior switching performance.

These devices are well suited for low voltage and battery powered applications where low in-line power loss and fast switching are required.

#### **Features**

- 9.4 A, 20 V  $R_{DS(ON)} = 14~m\Omega~@~V_{GS} = 4.5~V$   $R_{DS(ON)} = 18~m\Omega~@~V_{GS} = 2.5~V$
- Low gate charge (16 nC typical)
- ESD protection diode (note 3)
- High performance trench technology for extremely low  $R_{\text{DS}(\text{ON})}$
- · High power and current handling capability





### Absolute Maximum Ratings TA=25°C unless otherwise noted

Symbol	Parameter		Ratings	Units
$V_{DSS}$	Drain-Source Voltage		20	V
V <sub>GSS</sub>	Gate-Source Voltage		± 12	V
I <sub>D</sub>	Drain Current - Continuous	(Note 1a)	9.4	A
	- Pulsed		38	
P <sub>D</sub>	Power Dissipation for Dual Operation		2	W
	Power Dissipation for Single Operation	(Note 1a)	1.6	
		(Note 1b)	1	
		(Note 1c)	0.9	
T <sub>J</sub> , T <sub>STG</sub>	Operating and Storage Junction Temperature Range		-55 to +150	°C

### **Thermal Characteristics**

$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	(Note 1a)	78	°C/W
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case	(Note 1)	40	°C/W

### Package Marking and Ordering Information

Device Marking	Device	Reel Size	Tape width	Quantity
FDS6898AZ	FDS6898AZ	13"	12mm	2500 units

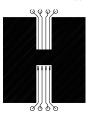
### **Electrical Characteristics**

T<sub>A</sub> = 25°C unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Тур	Max	Units
Off Char	acteristics					•
BV <sub>DSS</sub>	Drain-Source Breakdown Voltage	$V_{GS} = 0 \text{ V}, \qquad I_{D} = 250  \mu\text{A}$	20			V
ΔBV <sub>DSS</sub> ΔT <sub>J</sub>	Breakdown Voltage Temperature Coefficient	$I_D$ = 250 $\mu$ A, Referenced to 25°C		21		mV/°C
I <sub>DSS</sub>	Zero Gate Voltage Drain Current	V <sub>DS</sub> = 16 V, V <sub>GS</sub> = 0 V			1	μΑ
I <sub>GSSF</sub>	Gate-Body Leakage, Forward	$V_{GS} = 12 \text{ V},  V_{DS} = 0 \text{ V}$			10	μΑ
I <sub>GSSR</sub>	Gate-Body Leakage, Reverse	$V_{GS} = -12 \text{ V},  V_{DS} = 0 \text{ V}$			-10	μΑ
On Char	acteristics (Note 2)					
V <sub>GS(th)</sub>	Gate Threshold Voltage	$V_{DS} = V_{GS}$ , $I_D = 250 \mu A$	0.5	1	1.5	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate Threshold Voltage Temperature Coefficient	$I_D$ = 250 $\mu$ A, Referenced to 25°C		-3.5		mV/°C
R <sub>DS(on)</sub>	Static Drain–Source On–Resistance	$V_{GS} = 4.5 \text{ V}, I_D = 9.4 \text{ A}$ $V_{GS} = 2.5 \text{ V}, I_D = 8.3 \text{ A}$ $V_{GS} = 4.5 \text{ V}, I_D = 9.4 \text{ A}, T_J = 125^{\circ}\text{C}$		10 13 14	14 18 21	mΩ
I <sub>D(on)</sub>	On-State Drain Current	$V_{GS} = 4.5V, V_{DS} = 5 V$	19			Α
<b>g</b> FS	Forward Transconductance	$V_{DS} = 5 \text{ V}, \qquad I_{D} = 9.4 \text{ A}$		47		S
Dynamic	Characteristics					
C <sub>iss</sub>	Input Capacitance	$V_{DS} = 10 \text{ V},  V_{GS} = 0 \text{ V},$		1821		pF
Coss	Output Capacitance	f = 1.0 MHz		440		pF
C <sub>rss</sub>	Reverse Transfer Capacitance			208		pF
Switchir	ng Characteristics (Note 2)					
t <sub>d(on)</sub>	Turn-On Delay Time	$V_{DD} = 10 \text{ V},  I_D = 1 \text{ A},$		10	20	ns
t <sub>r</sub>	Turn-On Rise Time	$V_{GS} = 4.5 \text{ V},  R_{GEN} = 6 \Omega$		15	27	ns
t <sub>d(off)</sub>	Turn-Off Delay Time			34	55	ns
t <sub>f</sub>	Turn-Off Fall Time			16	29	ns
Q <sub>g</sub>	Total Gate Charge	$V_{DS} = 10 \text{ V},  I_{D} = 9.4 \text{ A},$		16	23	nC
Q <sub>gs</sub>	Gate-Source Charge	V <sub>GS</sub> = 4.5 V		3		nC
$Q_{gd}$	Gate-Drain Charge			4		nC
Drain-S	ource Diode Characteristics	and Maximum Ratings				
Is	Maximum Continuous Drain-Source	<b>v</b>			1.3	Α
V <sub>SD</sub>	Drain–Source Diode Forward Voltage	$V_{GS} = 0 \text{ V},  I_{S} = 1.3 \text{ A}$ (Note 2)		0.7	1.2	V

#### Notes

R<sub>8JA</sub> is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of
the drain pins. R<sub>8JC</sub> is guaranteed by design while R<sub>8CA</sub> is determined by the user's board design.



a) 78°C/W when mounted on a 0.5in<sup>2</sup> pad of 2 oz copper



b) 125°C/W when mounted on a 0.02 in<sup>2</sup> pad of 2 oz copper

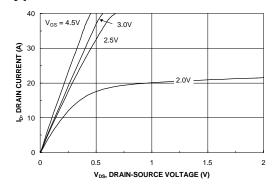


c) 135°C/W when mounted on a minimum mounting pad.

Scale 1:1 on letter size paper

- **2.** Pulse Test: Pulse Width <  $300\mu$ s, Duty Cycle < 2.0%
- 3. The diode connected between the gate and source serves only as protection against ESD. No gate overvoltage rating is implied

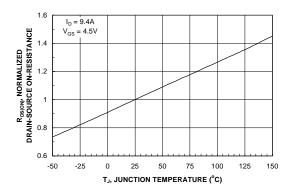
### **Typical Characteristics**



2.2

Figure 1. On-Region Characteristics.

Figure 2. On-Resistance Variation with Drain Current and Gate Voltage.



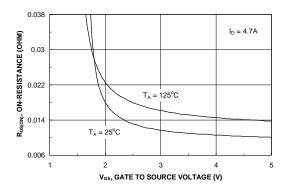
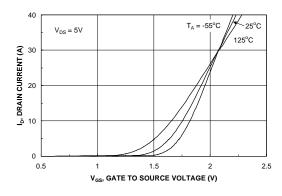


Figure 3. On-Resistance Variation with Temperature.

Figure 4. On-Resistance Variation with Gate-to-Source Voltage.



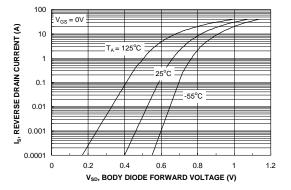
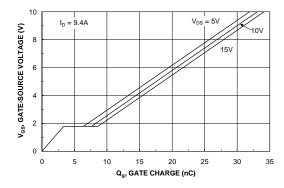


Figure 5. Transfer Characteristics.

Figure 6. Body Diode Forward Voltage Variation with Source Current and Temperature.

### **Typical Characteristics**



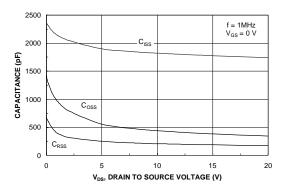


Figure 7. Gate Charge Characteristics.

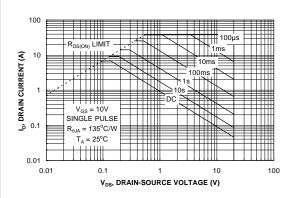


Figure 8. Capacitance Characteristics.

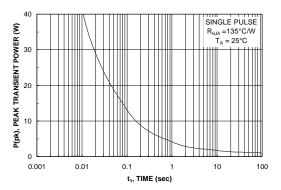


Figure 9. Maximum Safe Operating Area.



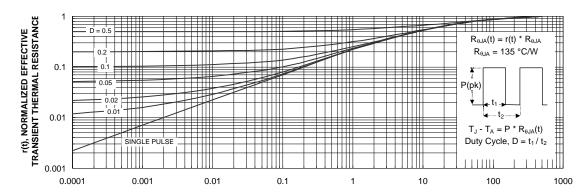


Figure 11. Transient Thermal Response Curve.

Thermal characterization performed using the conditions described in Note 1c. Transient thermal response will change depending on the circuit board design.

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