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FDZ2040L

Integrated Load Switch

Features

- Optimized for Low-Voltage Core ICs in Portable Systems
- Very Small Package Dimension: WL-CSP
0.8 X 0.8 X 0.5 mm³
- Current = 1.2 A, V_{IN} max. = 4 V
- Current = 2 A, V_{IN} max. = 4 V (Pulsed)
- R_{DS(ON)} = 80 mΩ at V_{ON} = 0 V, V_{IN} = 4 V
- R_{DS(ON)} = 85 mΩ at V_{ON} = 0 V, V_{IN} = 3.6 V
- R_{DS(ON)} = 90 mΩ at V_{ON} = 0 V, V_{IN} = 3 V
- RoHS Compliant

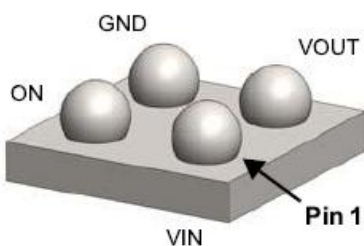


General Description

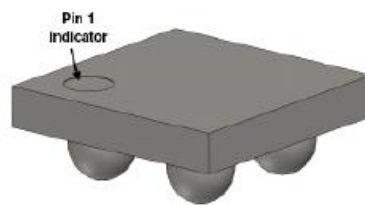
This device is particularly suited for compact power management in portable applications where 1.6 V to 4 V input and 1.2 A output current capability are needed. This load switch integrates a level-shifting function that drives a P-channel power MOSFET in the very small 0.8 X 0.8 X 0.5 mm³ WL-CSP package.

Applications

- Load Switch
- Power Management in Portable Applications



BOTTOM



TOP

Ordering Information

Part Number	Device Marking	Ball Pitch	Operating Temperature Range	Switch	Package	Packing Method
FDZ2040L	ZL	0.4 mm	-25 to 75°C	80 mΩ, P-Channel MOSFET	0.8x0.8x0.5 mm ³ WL-CSP	Tape and Reel

Application Diagram and Block Diagram

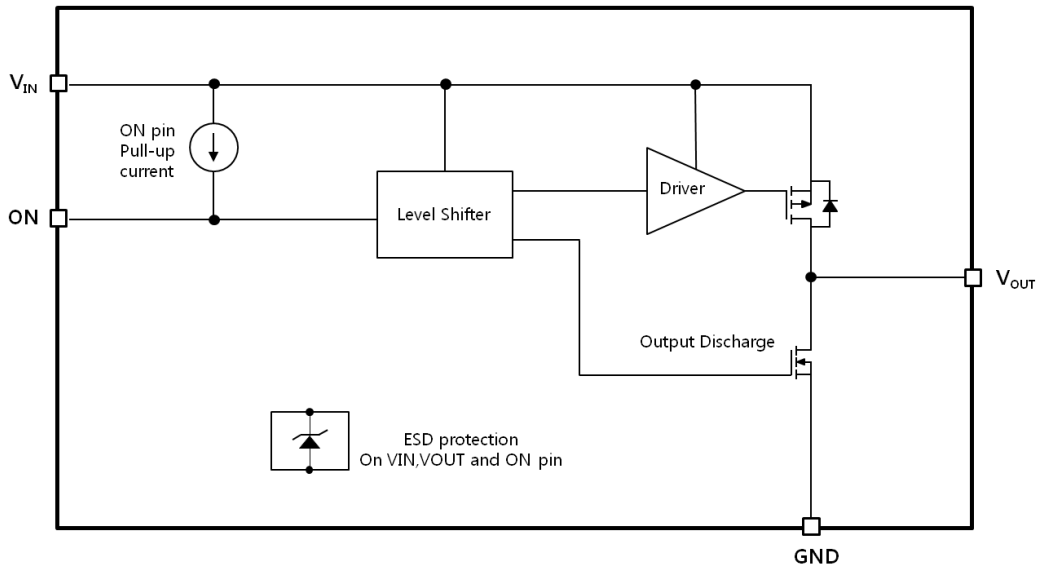


Figure 1. Block Diagram and Typical Application Pin Configuration

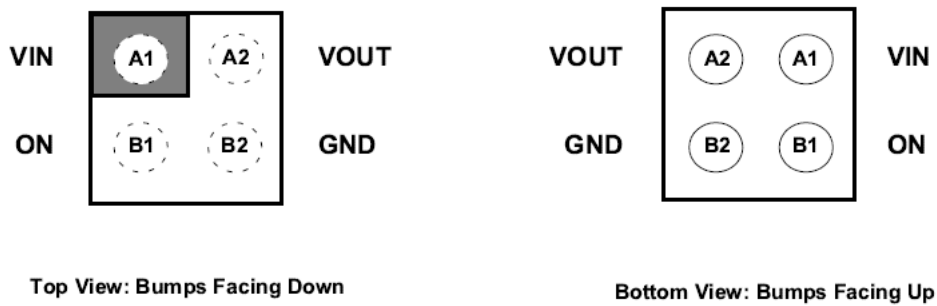


Figure 2. Pin Assignment

Pin Definitions

Pin #	Name	Description
A1	V _{IN}	Supply Input: Input to the load switch
A2	V _{OUT}	Switch Output: Output of the load switch
B1	ON	ON/OFF Control Input, Active LOW
B2	GND	Ground

Absolute Maximum Ratings

Parameter		Min.	Max.	Unit
V _{IN} , V _{OUT} , ON to GND		-0.3	4.2	V
I _{OUT} – Load Current (Continuous) ^(1a)			1.2	A
I _{OUT} – Load Current (Pulsed) ⁽²⁾			2	A
Power Dissipation @ T _A = 25°C ^(1a)			0.9	W
Operating Temperature Range		-40	105	°C
Storage Temperature		-65	150	°C
Electrostatic Discharge Capability	Human Body Model, JESD22-A114	8		kV
	Charged Device Model, JESD22-C101	2		

Thermal Characteristics

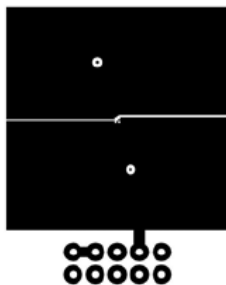
Parameter	Min.	Max.	Unit
Thermal Resistance, Junction to Ambient ^(1a)		117	°C/W

Recommended Operating Conditions

Parameter	Min.	Max.	Unit
V _{IN}	1.6	4.0	V
Ambient Operating Temperature, T _A	-25	75	°C

Notes:

- R_{θJA} is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. R_{θJC} is guaranteed by design while R_{θJA} is determined by the user's board design.



a. 117 °C/W when mounted on a 1 in² pad of 2 oz copper.



b. 277 °C/W when mounted on a minimum pad of 2 oz copper.

- Pulse Test: Pulse Width < 300 μs, Duty Cycle < 2.0%.

Electrical Characteristics

$T_J = 25\text{ }^\circ\text{C}$ unless otherwise noted.

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_{IN}	Operation Voltage		1.6		4.0	V
V_{IL}	ON Input Logic LOW Voltage	$V_{IN} = 1.6\text{ V}$, Ramp-Down V_{ON} from 1 V to 0 V, V_{OUT} LOW to HIGH, $T_J = -25$ to $75\text{ }^\circ\text{C}$			0.35	V
		$V_{IN} = 4\text{ V}$, Ramp-Down V_{ON} from 1 V to 0 V, V_{OUT} LOW to HIGH, $T_J = -25$ to $75\text{ }^\circ\text{C}$			0.35	V
V_{IH}	ON Input Logic HIGH Voltage	$V_{IN} = 1.6\text{ V}$, Ramp-Up V_{ON} from 0 V to 1 V, V_{OUT} HIGH to LOW, $T_J = -25$ to $75\text{ }^\circ\text{C}$	1.35			V
		$V_{IN} = 4\text{ V}$, Ramp-Up V_{ON} from 0 V to 1 V, V_{OUT} HIGH to LOW, $T_J = -25$ to $75\text{ }^\circ\text{C}$	1.35			V
I_Q	Quiescent Current	$V_{IN} = 3\text{ V}$, $V_{ON} = 0.35\text{ V}$, $I_{OUT} = 0\text{ A}$, $T_J = -25$ to $75\text{ }^\circ\text{C}$		1.55	2.50	μA
I_{Q_off}	Off Supply Current	$V_{IN} = 3\text{ V}$, $V_{ON} = 1.3\text{ V}$, $I_{OUT} = 0\text{ A}$, $T_J = -25$ to $75\text{ }^\circ\text{C}$		2.4	6.5	μA
I_{SD_off}	Off Switch Current	$V_{IN} = 3\text{ V}$, $V_{ON} = 1.3\text{ V}$, $V_{OUT} = 0\text{ V}$, $T_J = -25$ to $75\text{ }^\circ\text{C}$		0.1	3.5	μA
I_{Q_off} (V_{ON} float)	Off Supply Current with ON Pin Floating	$V_{IN} = 3\text{ V}$, $V_{ON} = \text{Floating}$, $I_{OUT} = 0\text{ A}$		1.6	2.3	μA
		$V_{IN} = 3\text{ V}$, $V_{ON} = \text{Floating}$, $I_{OUT} = 0\text{ A}$, $T_J = -25$ to $75\text{ }^\circ\text{C}$		1.6	4.0	μA
$R_{PULL-DOWN}$	Output Pull-Down Resistance	$V_{IN}=3\text{ V}$, $I_{OUT}=10\text{ mA}$		22		Ω
$R_{DS(ON)}$	On Resistance	$V_{IN} = 1.6\text{ V}$, $V_{ON} = 0\text{ V}$, $I_{OUT} = 300\text{ mA}$		68	120	m Ω
		$V_{IN} = 3\text{ V}$, $V_{ON} = 0\text{ V}$, $I_{OUT} = 300\text{ mA}$		50	90	
		$V_{IN} = 3.6\text{ V}$, $V_{ON} = 0\text{ V}$, $I_{OUT} = 300\text{ mA}$		48	85	
		$V_{IN} = 4\text{ V}$, $V_{ON} = 0\text{ V}$, $I_{OUT} = 300\text{ mA}$, $T_J = -25$ to $75\text{ }^\circ\text{C}$		47	80	
$C_{V-ON(INP)}$	ON Input Capacitance	$T_J = -25$ to $75\text{ }^\circ\text{C}$			5	pF
$I_{ON(PULL-UP)}$	ON Pull-Up Current	$V_{IN} = 3\text{ V}$, $V_{ON} = 0\text{ V}$, $T_J = -25$ to $75\text{ }^\circ\text{C}$	0.30	0.76	1.20	μA

Switching Characteristics

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit	
t_{on}	Turn-On Time (V_{ON} 50% to V_{OUT} 90%)	$V_{IN}=3\text{ V}$, $V_{ON} = 0\text{ V}$ as Logic LOW and 1.3 V as Logic HIGH, $C_{OUT} = 1\text{ nF}$, $R_L = 30\ \Omega$, $T_J = -25$ to $75\text{ }^\circ\text{C}$		45	150	ns	
t_{don}	Turn-On Delay (V_{ON} 50% to V_{OUT} 10%)			35	100	ns	
t_{rise}	Turn-On Rise Time (V_{OUT} 10% to 90%)			10	50	ns	
t_{off}	Turn-Off Time (V_{ON} 50% to V_{OUT} 10%)			60	150	ns	
t_{doff}	Turn-Off Delay (V_{ON} 50% to V_{OUT} 90%)			25	100	ns	
t_{fall}	Turn-Off Fall Time (V_{OUT} 90% to 10%)			35	65	ns	
$t_{don} - t_{doff}$	Turn-On Turn-Off Delay Delta					50	ns

Typical Performance Characteristics

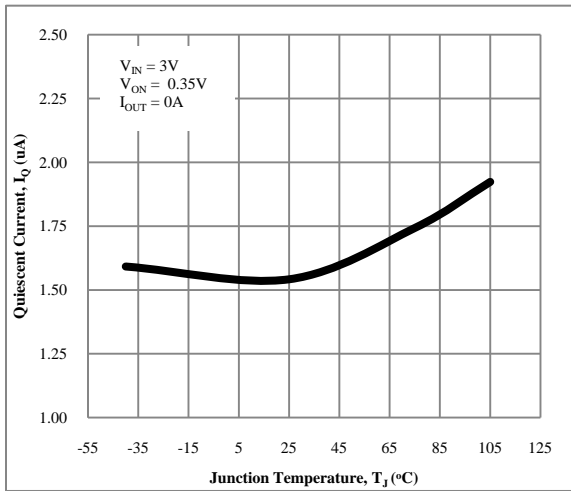


Figure 3. Quiescent Current vs. Temperature

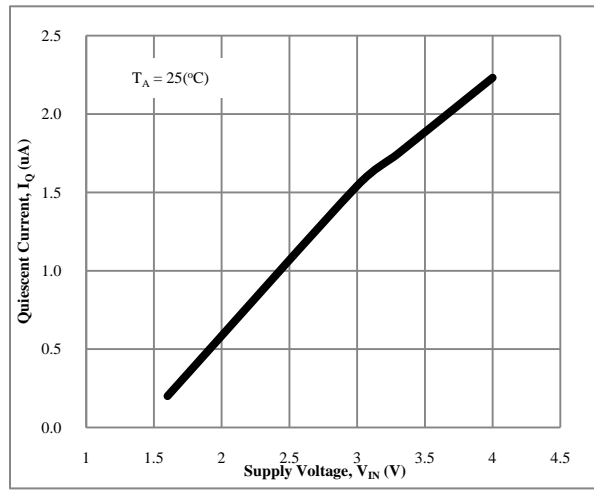


Figure 4. Quiescent Current vs. Supply Voltage

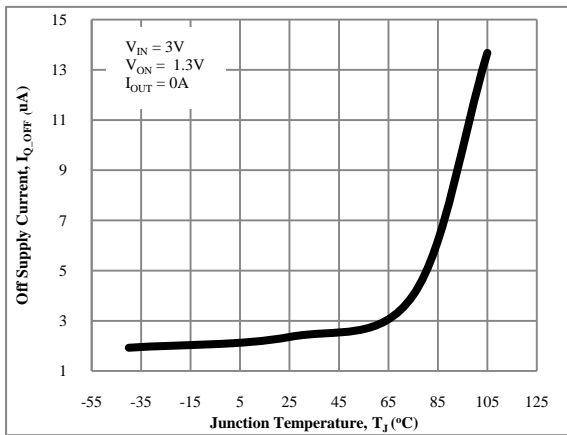


Figure 5. Off Supply Current vs. Temperature

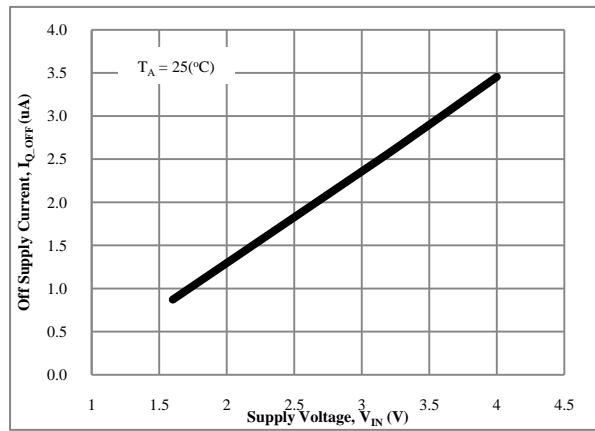


Figure 6. Off Supply Current vs. Supply Voltage

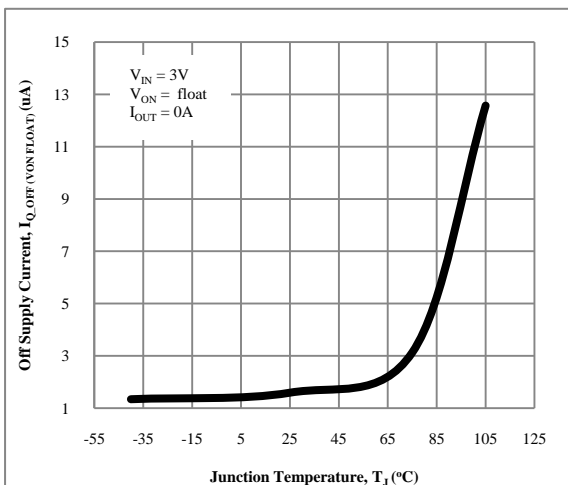


Figure 7. Off Supply Current (V_{ON} Float) vs. Temperature

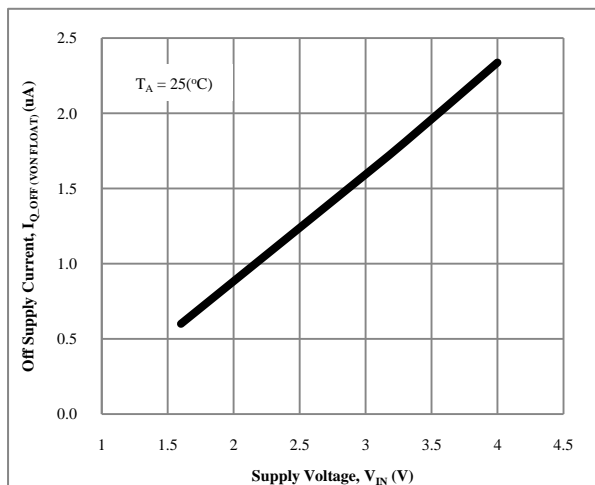


Figure 8. Off Supply Current (V_{ON} Float) vs. Supply Voltage

Typical Performance Characteristics (Continued)

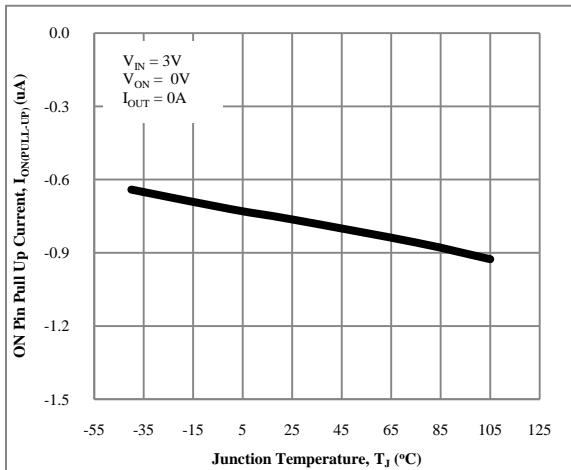


Figure 9. ON Pin Pull-Up Current vs. Temperature

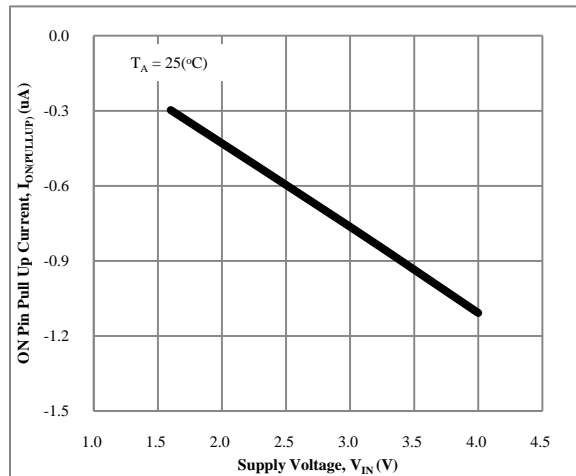


Figure 10. ON Pin Pull-Up Current vs. Supply Voltage

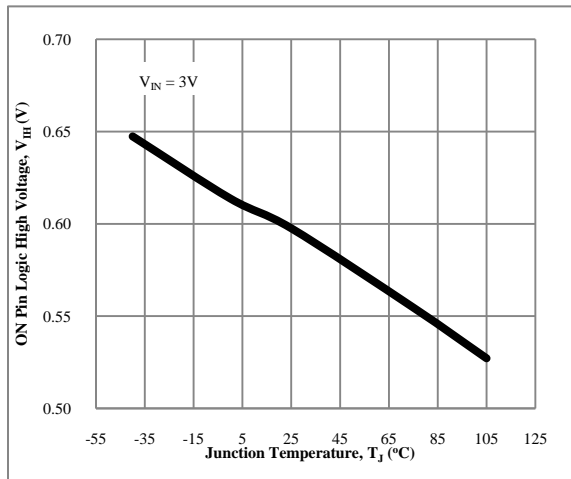


Figure 11. ON Pin Logic HIGH Voltage vs. Temperature

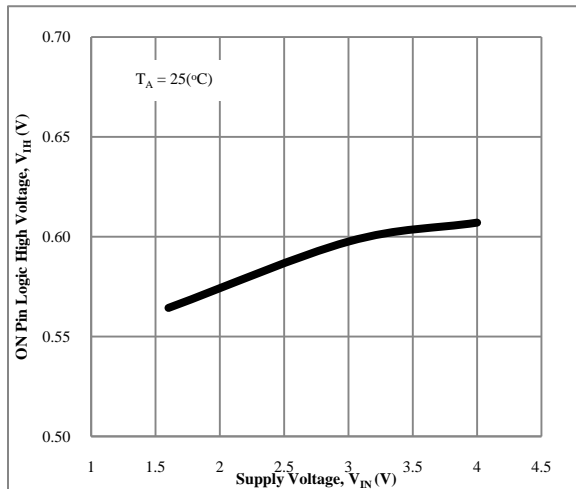


Figure 12. ON Pin Logic HIGH Voltage vs. Supply Voltage

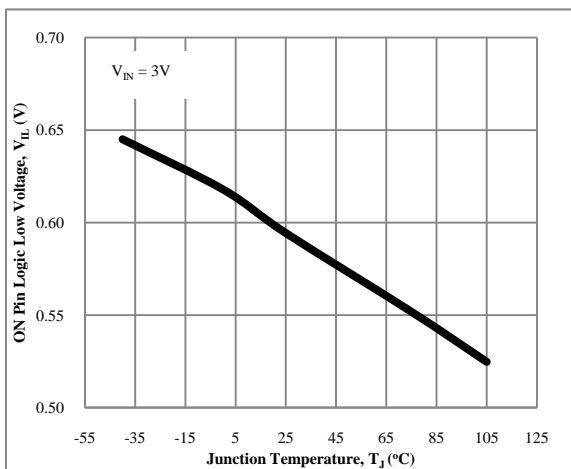


Figure 13. ON Pin Logic LOW Voltage vs. Temperature

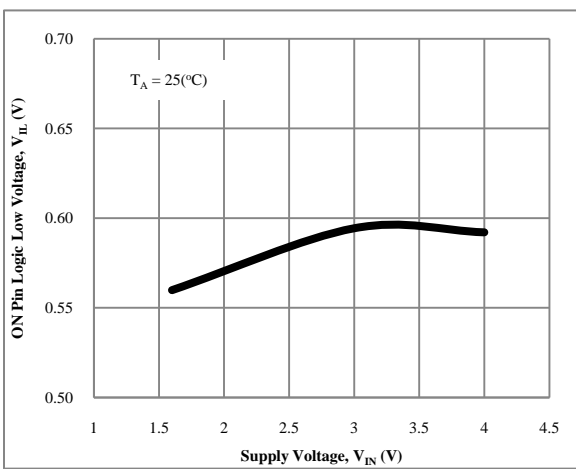


Figure 14. ON Pin Logic LOW Voltage vs. Supply Voltage

Typical Performance Characteristics (Continued)

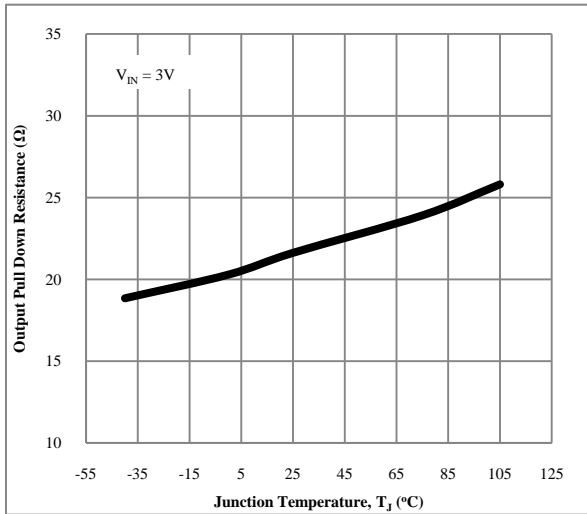


Figure 15. Output Pull-Down Resistance vs. Temperature

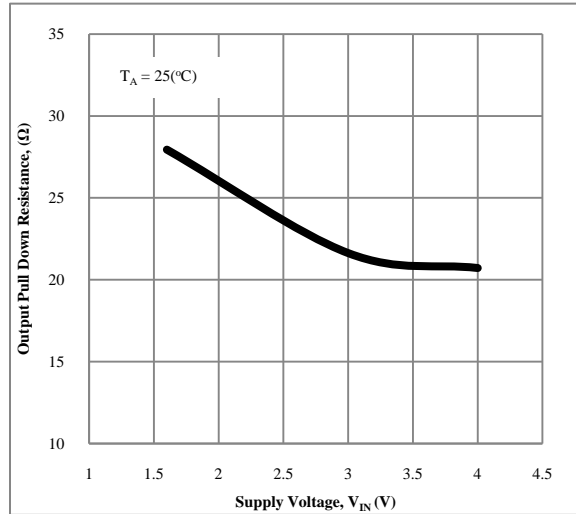


Figure 16. Output Pull-Down Resistance vs. Supply Voltage

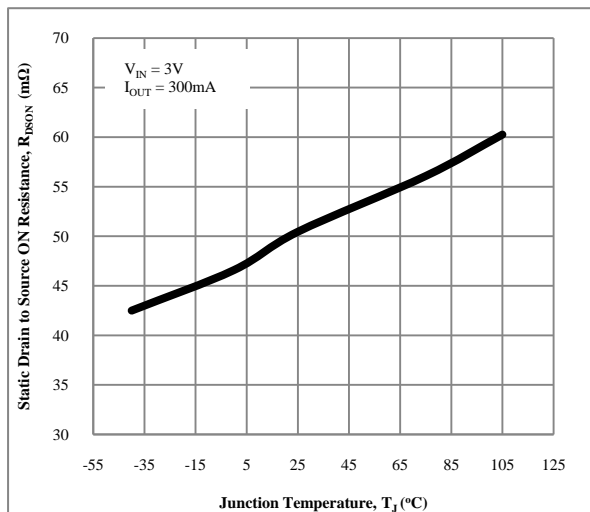


Figure 17. Static Drain-to-Source ON Resistance vs. Temperature

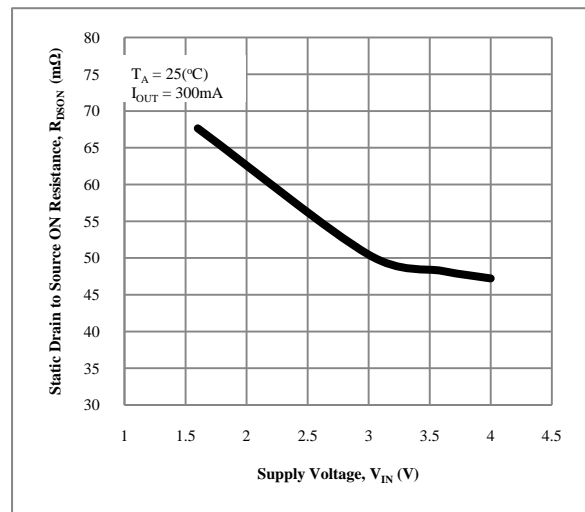
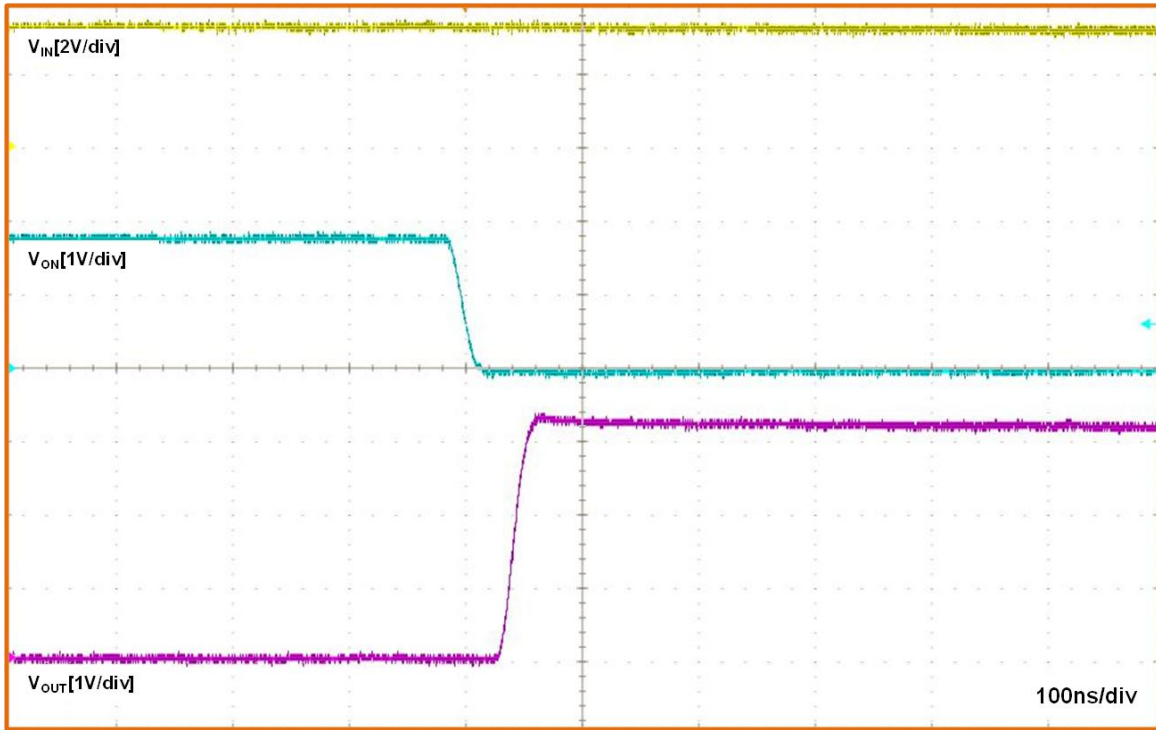


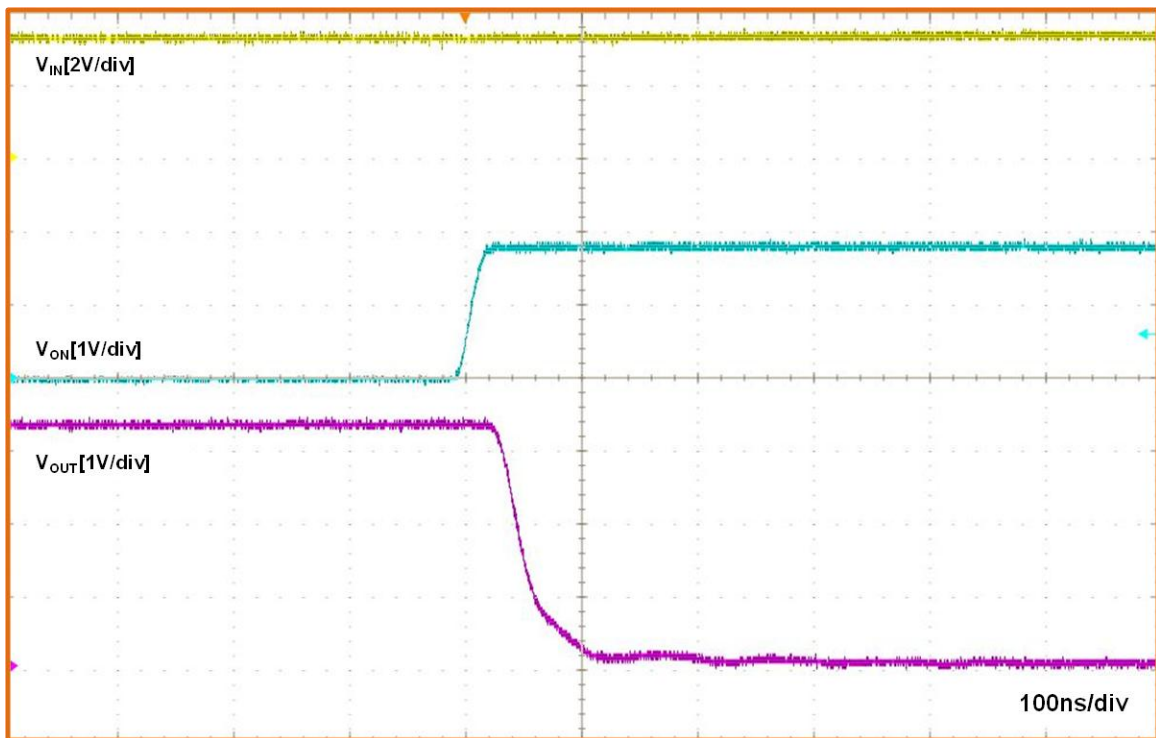
Figure 18. Static Drain-to-Source ON Resistance vs. Supply Voltage

Typical Performance Characteristics (Continued)



$V_{IN} = 3.3 \text{ V}$, $V_{ON} = 0 \text{ V}$, $C_{IN} = 1 \mu\text{F}$, $C_{OUT} = 1 \text{ nF}$, $R_L = 30 \Omega$

Figure 19. t_{ON} Response



$V_{IN} = 3.3 \text{ V}$, $V_{ON} = 0 \text{ V}$, $C_{IN} = 1 \mu\text{F}$, $C_{OUT} = 1 \text{ nF}$, $R_L = 30 \Omega$

Figure 20. t_{OFF} Response

Operation Description

The FDZ2040L is a low- $R_{DS(ON)}$ P-channel load switch packaged in space-saving 0.8 x 0.8 WL-CSP.

The core of the device is an 80m Ω P-channel MOSFET and capable of functioning over a wide input operating range of 1.6 V-4 V.

Applications Information

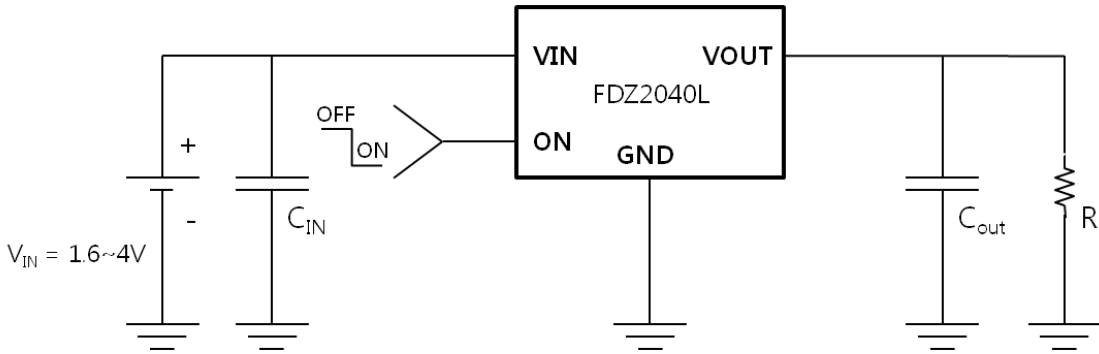


Figure 21. Typical Application

Input Capacitor

To reduce device inrush current effect, a 0.1 μ F ceramic capacitor, C_{IN} is recommended close to the V_{IN} pin. A higher value of C_{IN} can be used to further reduce the voltage drop experienced as the switch is turned on into a large capacitive load.

Output Capacitor

FDZ2040L switch works without an output capacitor. If parasitic board inductance forces V_{OUT} below GND when switching off, a 1 nF capacitor, C_{OUT} , should be placed between V_{OUT} and GND.

Note:

- The intrinsic diode for P-channel load switch would conduct if V_{OUT} is greater than V_{IN} , by a diode drop.

Evaluation Board Layout

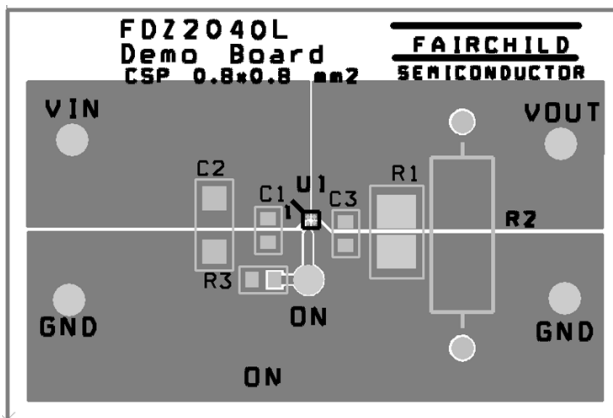


Figure 22. Top View

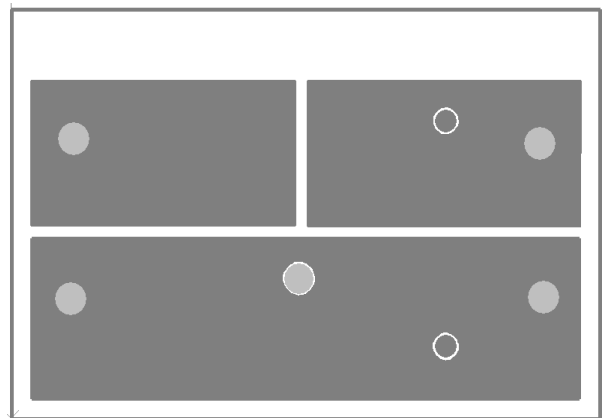
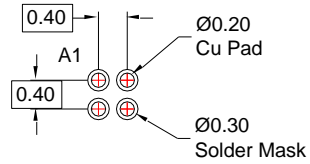
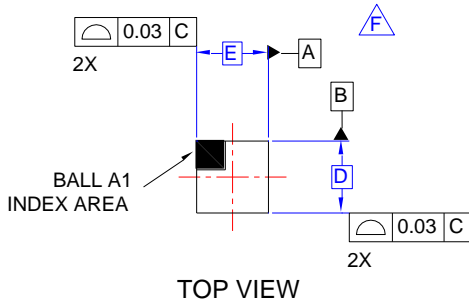
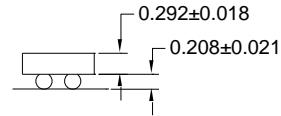
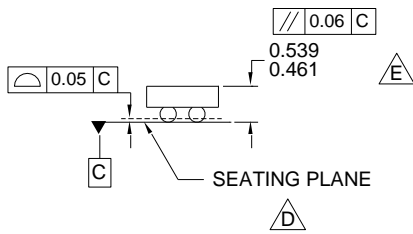


Figure 23. Bottom View

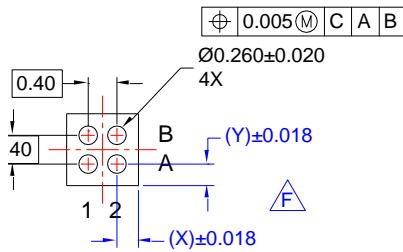
Physical Dimensions



RECOMMENDED LAND PATTERN
(NSMD PAD TYPE)



SIDE VIEWS



BOTTOM VIEW

NOTES:

- A. NO JEDEC REGISTRATION APPLIES.
- B. DIMENSIONS ARE IN MILLIMETERS.
- C. DIMENSIONS AND TOLERANCE PER ASME Y14.5M, 1994.
- D. DATUM C IS DEFINED BY THE SPHERICAL CROWNS OF THE BALLS.
- E. PACKAGE NOMINAL HEIGHT IS 500 MICRONS ±39 MICRONS (461-539 MICRONS).
- F. FOR DIMENSIONS D, E, X, AND Y SEE PRODUCT DATASHEET.
- G. DRAWING FILNAME: MKT-UC004AFrev1.

Figure 24. 4 Ball, WLCSP, 2 X 2 Array, 0.4 mm Pitch, 250 μm Ball

Product-Specific Dimensions





Product	D	E	X	Y
FDZ22040L	0.8 ± 0.03 mm	0.8 ± 0.03 mm	0.21 mm	0.21 mm

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