

# Silicon Carbide Schottky Diode

## 650 V, 8 A

### FFSD0865B

Silicon Carbide (SiC) Schottky Diodes use a completely new technology that provides superior switching performance and higher reliability compared to Silicon. No reverse recovery current, temperature independent switching characteristics, and excellent thermal performance sets Silicon Carbide as the next generation of power semiconductor. System benefits include highest efficiency, faster operating frequency, increased power density, reduced EMI, and reduced system size and cost.

#### Features

- Max Junction Temperature 175°C
- Avalanche Rated 33 mJ
- High Surge Current Capacity
- Positive Temperature Coefficient
- Ease of Paralleling
- No Reverse Recovery/No Forward Recovery
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant

#### Applications

- General Purpose
- SMPS, Solar Inverter, UPS
- Power Switching Circuits

#### MAXIMUM RATINGS (T<sub>J</sub> = 25°C unless otherwise noted)

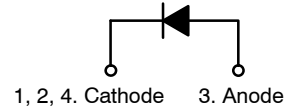
Parameter	Symbol	Value	Unit	
Peak Repetitive Reverse Voltage	V <sub>RRM</sub>	650	V	
Single Pulse Avalanche Energy (T <sub>J</sub> = 25°C, I <sub>L(pk)</sub> = 11.5 A, L = 0.5 mH, V = 50 V)	E <sub>AS</sub>	33	mJ	
Continuous Rectified Forward Current	T <sub>C</sub> < 153	I <sub>F</sub>	8.0	A
	T <sub>C</sub> < 135		11.6	
Non-Replicative Peak Forward Surge Current	T <sub>C</sub> = 25°C, t <sub>p</sub> = 10 μs	I <sub>FM</sub>	577	A
	T <sub>C</sub> = 150°C, t <sub>p</sub> = 10 μs		538	
Non-Replicative Forward Surge Current (Half-Sine Pulse)	T <sub>C</sub> = 25°C, t <sub>p</sub> = 8.3 ms	I <sub>FSM</sub>	42	A
Power Dissipation	T <sub>C</sub> = 25°C	P <sub>tot</sub>	91	W
	T <sub>C</sub> = 150°C		15	
Operating Junction and Storage Temperature Range	T <sub>J</sub> , T <sub>stg</sub>	-55 to +175	°C	

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

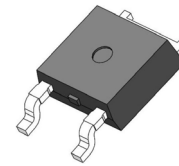


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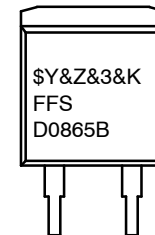


Schottky Diode



DPAK3 (TO-252, 3 LD)  
CASE 369AS

#### MARKING DIAGRAM



\$Y = ON Semiconductor Logo  
 &Z = Assembly Plant Code  
 &3 = Numeric Date Code  
 &K = Lot Code  
 FFSD0865B = Specific Device Code

#### ORDERING INFORMATION

See detailed ordering and shipping information on page 2 of this data sheet.

# FFSD0865B

## THERMAL RESISTANCE

Parameter	Symbol	Value	Unit
Thermal Resistance, Junction-to-Case	$R_{\theta JC}$	1.64	$^{\circ}\text{C}/\text{W}$

## ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
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### ON CHARACTERISTICS

$V_F$	Forward Voltage	$I_F = 8.0 \text{ A}, T_J = 25^{\circ}\text{C}$		1.39	1.7	V
		$I_F = 8.0 \text{ A}, T_J = 125^{\circ}\text{C}$		1.55	2.0	
		$I_F = 8.0 \text{ A}, T_J = 175^{\circ}\text{C}$		1.71	2.4	
$I_R$	Reverse Current	$V_R = 650 \text{ V}, T_J = 25^{\circ}\text{C}$		0.5	40	$\mu\text{A}$
		$V_R = 650 \text{ V}, T_J = 125^{\circ}\text{C}$		1.0	80	
		$V_R = 650 \text{ V}, T_J = 175^{\circ}\text{C}$		2.0	160	

### CHARGES, CAPACITANCES & GATE RESISTANCE

$Q_C$	Total Capacitive Charge	$V_C = 400 \text{ V}$		22		nC
$C_{tot}$		$V_R = 1 \text{ V}, f = 100 \text{ kHz}$		336		pF
		$V_R = 200 \text{ V}, f = 100 \text{ kHz}$		39		
		$V_R = 400 \text{ V}, f = 100 \text{ kHz}$		30		

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

## PART MARKING AND ORDERING INFORMATION

Part Number	Top Mark	Package	Packing Method <sup>†</sup>	Reel Size	Tape Width	Quantity
FFSD0865B	FFSD0865B	DPAK3	Tape & Reel	330 mm	16 mm	2500 units

<sup>†</sup>For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

TYPICAL CHARACTERISTICS

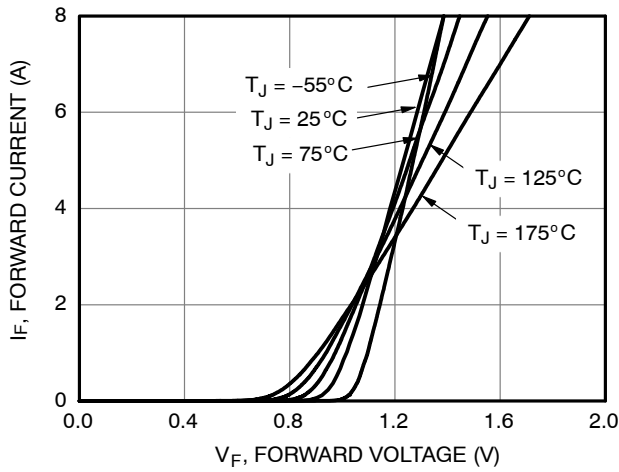


Figure 1. Forward Characteristics

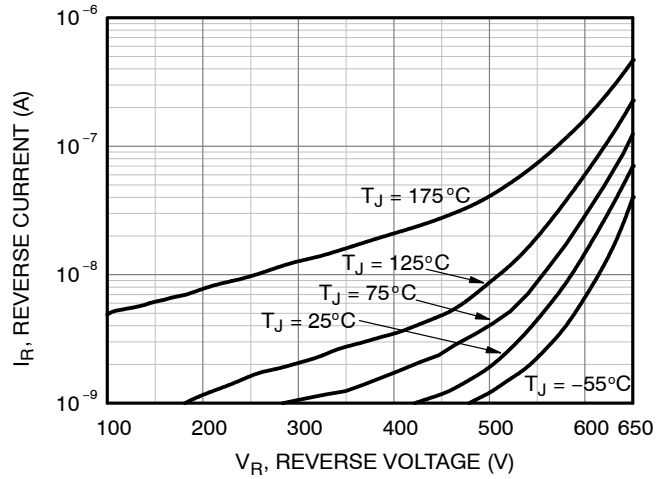


Figure 2. Reverse Characteristics

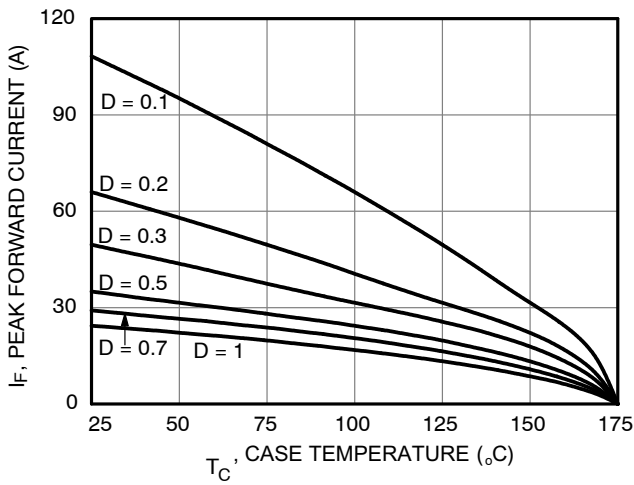


Figure 3. Current Derating

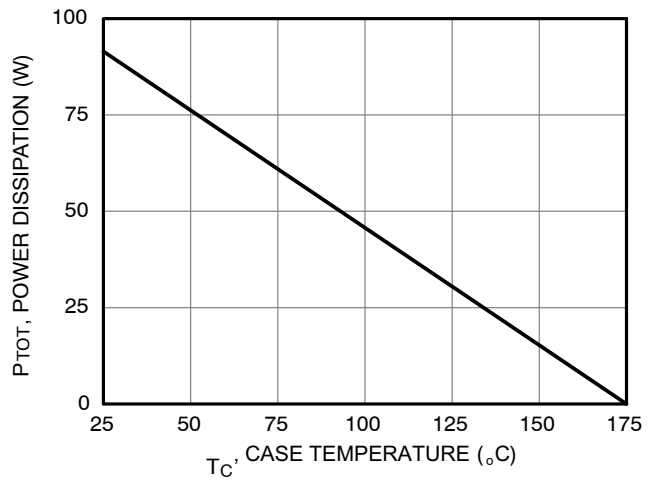


Figure 4. Power Derating

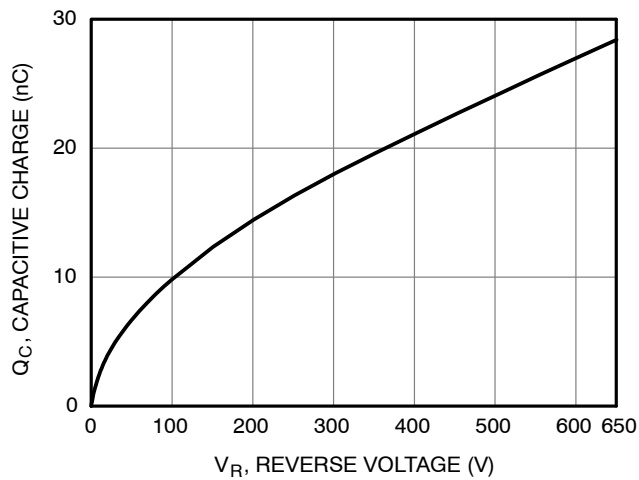


Figure 5. Capacitive Charge vs. Reverse Voltage

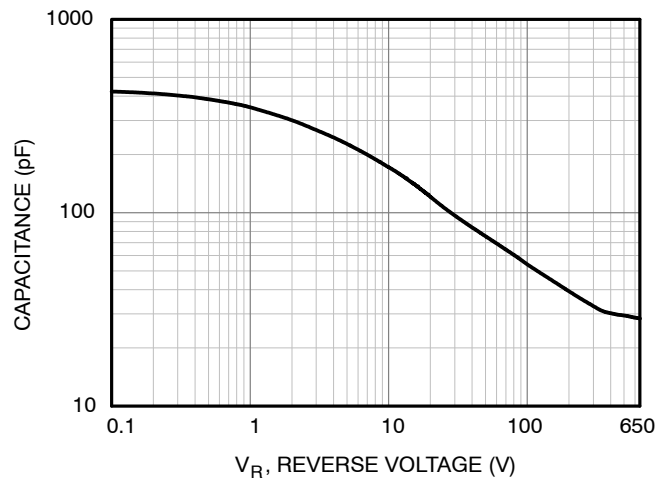


Figure 6. Capacitance vs. Reverse Voltage

TYPICAL CHARACTERISTICS (continued)

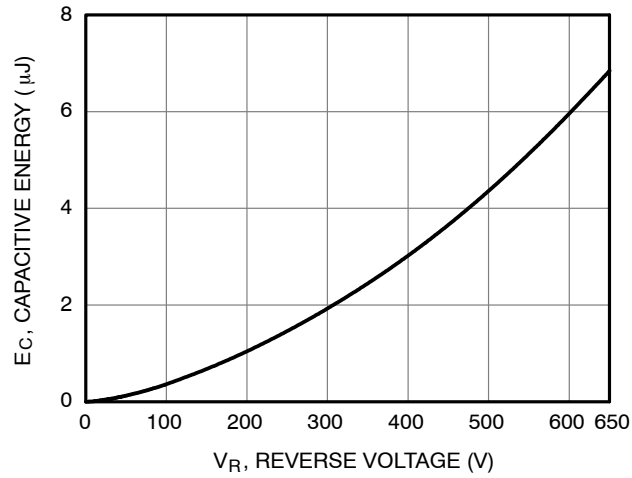


Figure 7. Capacitance Stored Energy

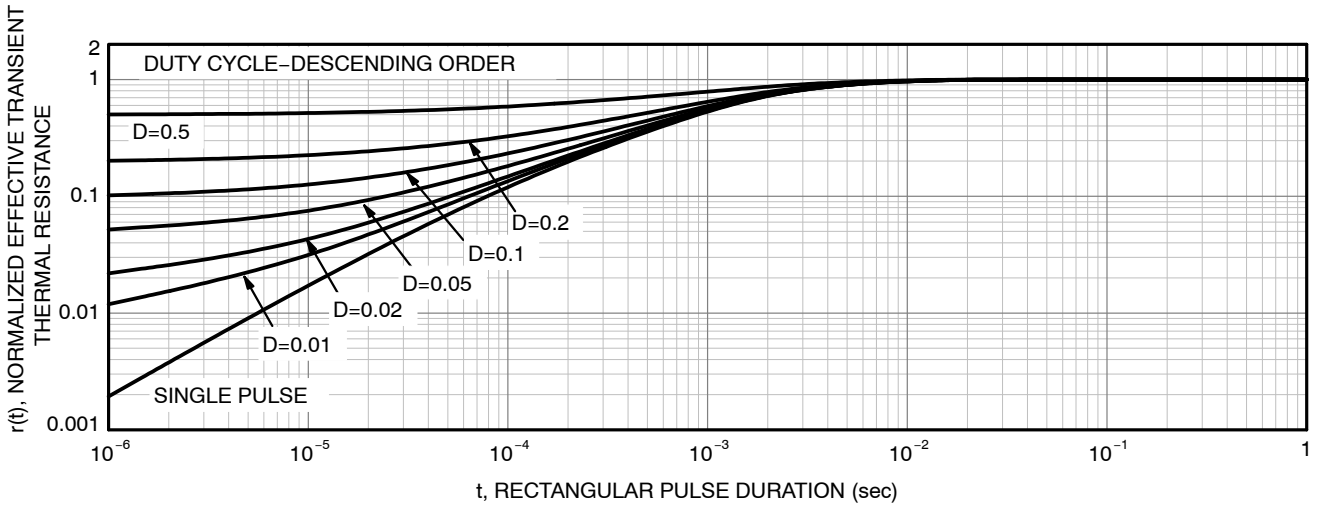


Figure 8. Junction-to-Case Transient Thermal Response

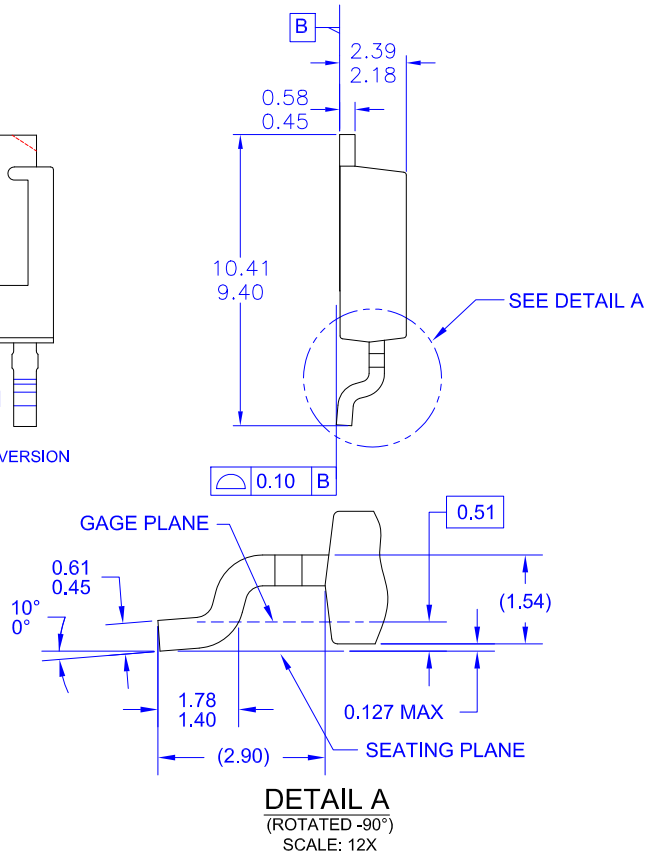
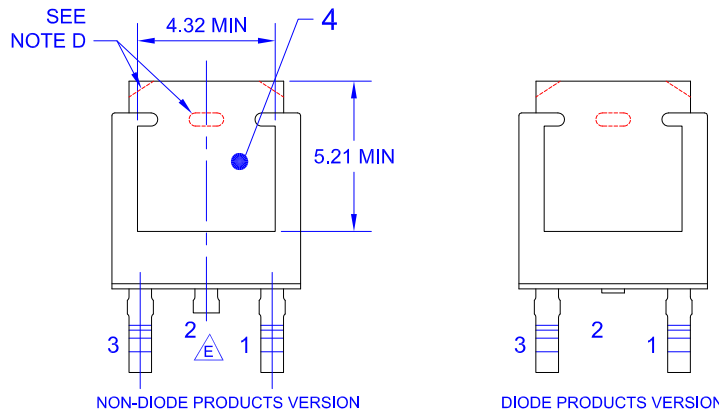
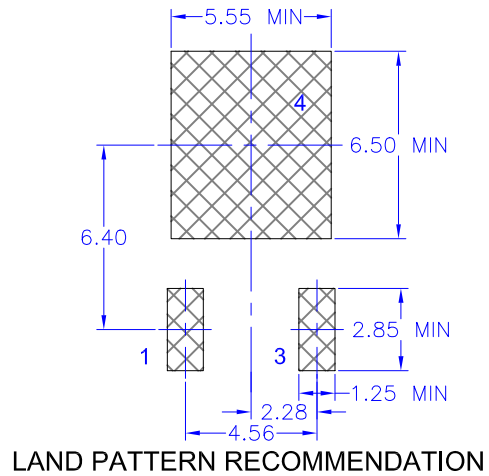
# MECHANICAL CASE OUTLINE PACKAGE DIMENSIONS

ON Semiconductor®



## DPAK3 (TO-252 3 LD) CASE 369AS ISSUE O

DATE 30 SEP 2016



- NOTES: UNLESS OTHERWISE SPECIFIED
- A) THIS PACKAGE CONFORMS TO JEDEC, TO-252, ISSUE C, VARIATION AA.
  - B) ALL DIMENSIONS ARE IN MILLIMETERS.
  - C) DIMENSIONING AND TOLERANCING PER ASME Y14.5M-2009.
  - D) SUPPLIER DEPENDENT MOLD LOCKING HOLES OR CHAMFERED CORNERS OR EDGE PROTRUSION.
  - E) TRIMMED CENTER LEAD IS PRESENT ONLY FOR DIODE PRODUCTS
  - F) DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH AND TIE BAR EXTRUSIONS.
  - G) LAND PATTERN RECOMMENDATION IS BASED ON IPC7351A STD TO228P991X239-3N.

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