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FAIRCHILD SEMICONDUCTOR®

October 2009

µSerDes™ FIN224C
24-Bit Low-Power Serializer/Deserializer

Features

Data & Control Bits	24
Frequency	20MHz
Capability	HVGA
Interface	Microcontroller / RGB
µController Usage	I86 & m68
Dynamic Current	17mA at 10Mhz
Standby Current	10µA
Core Voltage ($V_{DDA/S}$)	2.5V to 3.3V
I/O Voltage (V_{DDP})	1.65V to 3.6V
ESD	15KV (IEC)
Package	MLP-40 (6 x 6mm)
Ordering Information	FIN224CMLX, MLP-40

Related Resources

- For samples and questions, please contact: interface@fairchildsemi.com.

Description

The FIN224C µSerDes™ is a low-power serializer/deserializer (µSerDes™) that can help minimize the cost and power of transferring wide signal paths. Through the use of serialization, the number of signals transferred from one point to another can be significantly reduced. Typical reduction is 5:1 for unidirectional paths. Through the use of differential signaling, shielding and EMI filters can also be minimized, further reducing the cost of serialization.

The differential signaling is also important for providing a noise-insensitive signal that can withstand radio and electrical noise sources. Major reduction in power consumption allows minimal impact on battery life in mobile applications. It is possible to use a single Phase-Locked Loop (PLL) for most applications, including bi-directional operation.

Applications

- Slider, Folder, and Clamshell Mobile Handsets
- GSM and CDMA Phones

Typical Application

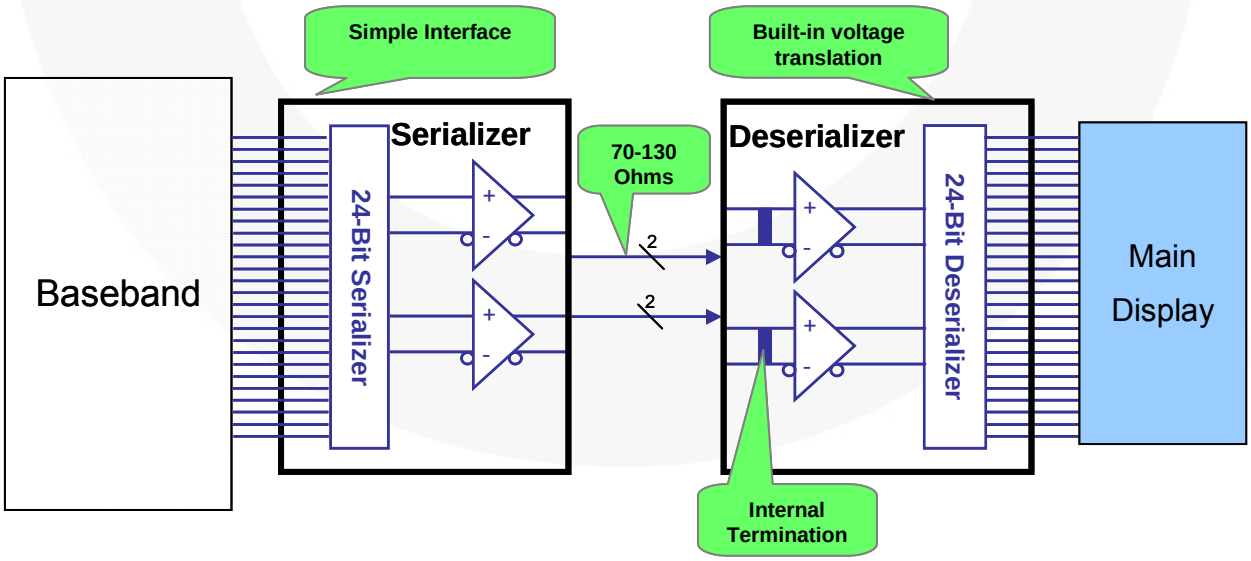


Figure 1. Mobile Phone Example

Pin Configuration

Pin Name	Description		
STROBE	LVCMOS Strobe Signal for Latching Data into the Serializer (On Rising Edge)		
CKREF	LVCMOS Clock Input and PLL Reference		
CKP	LVCMOS Word Clock Output		
DP[24:1]	LVCMOS Data I/O		
/DIRO	LVCMOS Control Output Inversion of DIRI		
S1, S2	LVCMOS Select Pins, Controls the Mode of Operation, *see Table 1*		
DIRI	LVCMOS Control, Selects Serializer or Deserializer Mode	0	Deserializer
		1	Serializer
DSO+ / DSI- DSO- / DSI+	Serial Data I/O		
CKSI+, CKSI-	Serial Clock Input		
CKSO+, CKSO-	Serial Clock Output		
VDDP	Power Supply for Parallel I/O and Internal Circuitry		
VDDS	Power Supply for Serial I/O		
VDDA	Power Supply for Core		
GND	Ground Pins		

Note:
1. 0 = V_{IL}; 1 = V_{IH}.

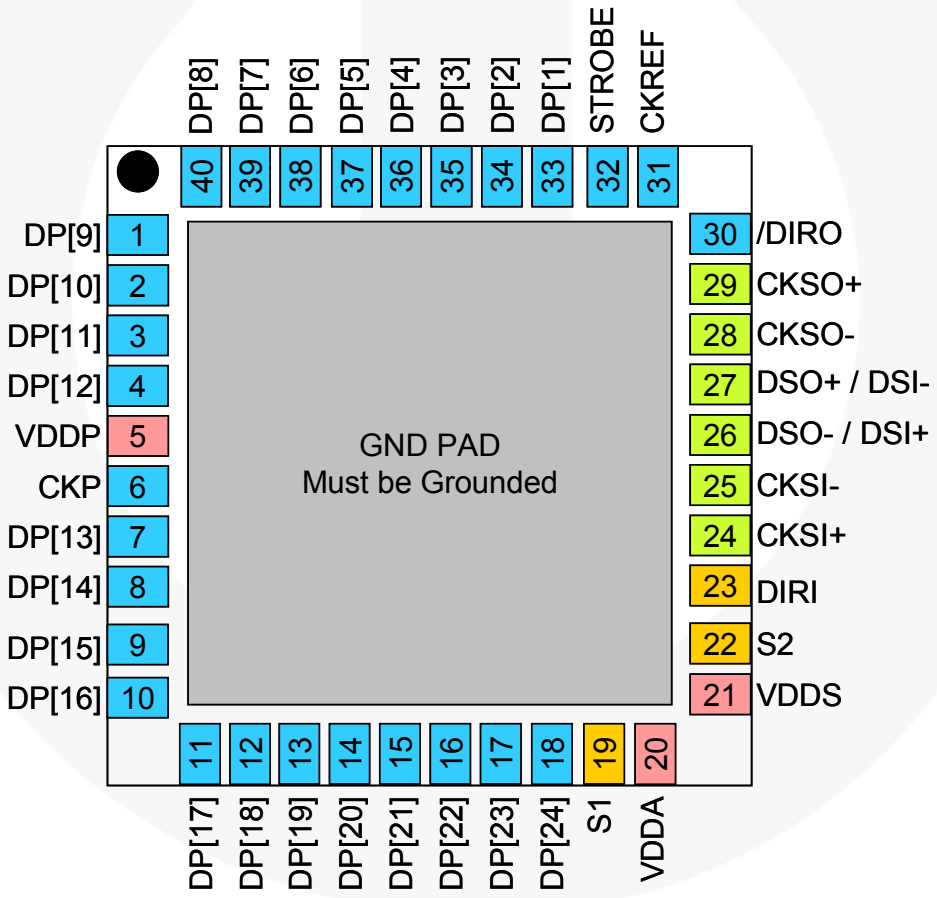


Figure 2. MLP-40 Pinout (Through View)

Table 1. Serializer / Deserializer, Operation, and Reset Modes

DIRI	S1	S2	Mode of Operation
X	0	0	Reset Mode LVCMOS Outputs = High Impedance LVCMOS Inputs = Known State
1	0	1	Serializer Mode
0	1	0	Deserializer Mode

Application Diagrams

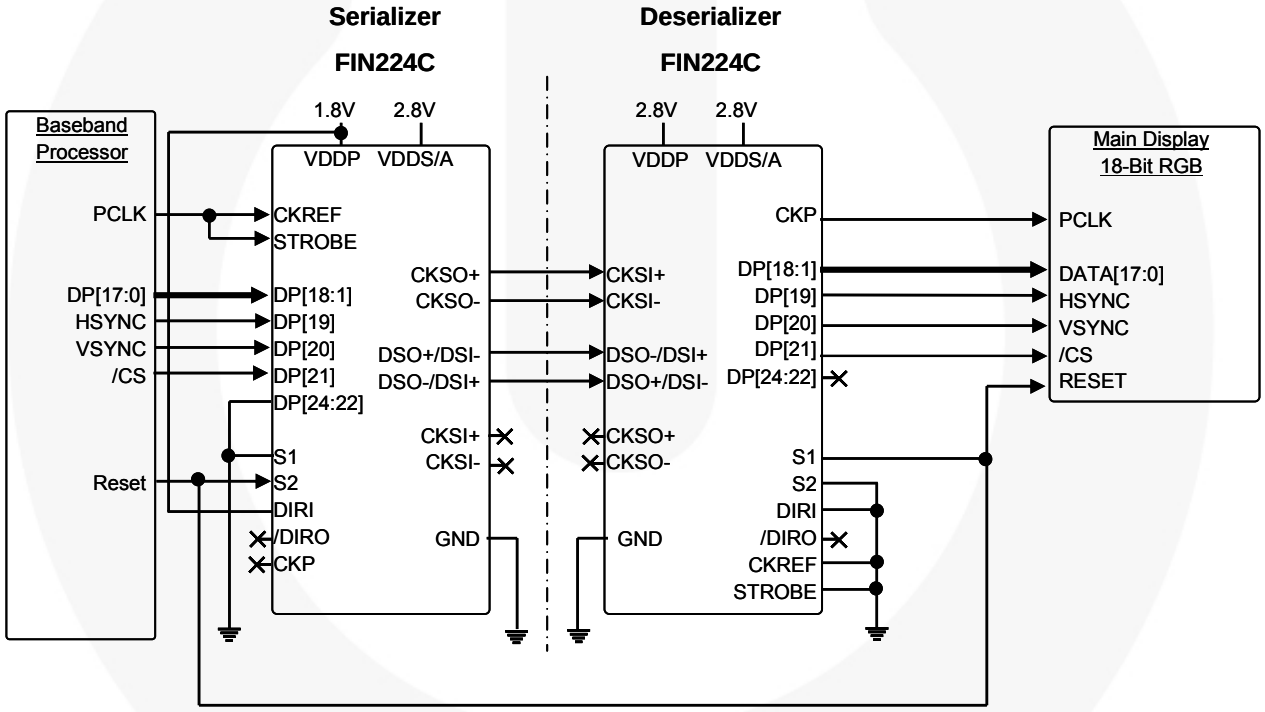


Figure 3. 18-Bit RGB Interface Block Diagram

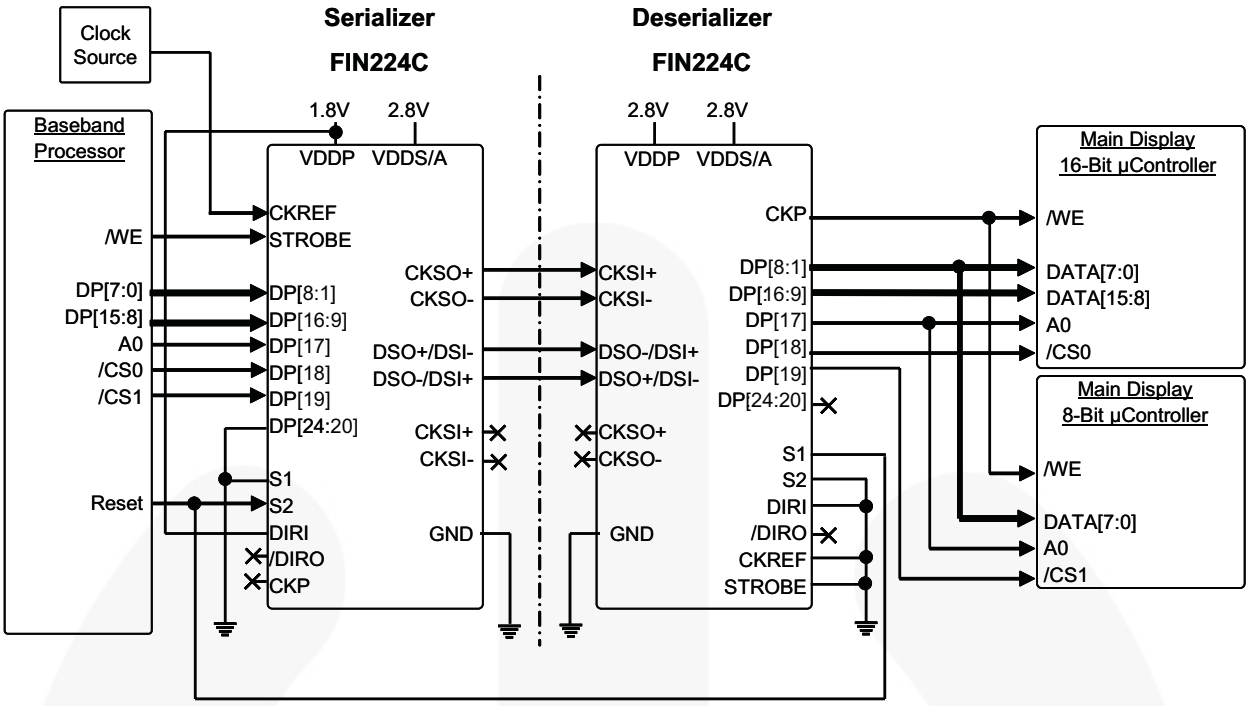


Figure 4. Dual-Display µController Interface Block Diagram

Additional Application Information

Flex Cabling: The serial I/O information is transmitted at a high serial rate. Care must be taken implementing this serial I/O flex cable. The following best practices should be used when developing the flex cabling or Flex PCB.

- Keep all four differential serial wires the same length.
- Do not allow noisy signals over or near differential serial wires. Example: No CMOS traces over differential serial wires.
- Design goal of 70 to 130Ω differential characteristic impedance.
- Do not place test points on differential serial wires.
- Design differential serial wires a minimum of 2cm away from the antenna.
- Visit Fairchild's website at http://www.fairchildsemi.com/products/interface/userdes.html, contact your sales representative, or contact Fairchild directly at interface@fairchildsemi.com for applications notes or flex guidelines.

Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Parameter		Min.	Max.	Unit
V_{DD}	Supply Voltage		-0.5	+4.6	V
	All Input/Output Voltage		-0.5	+4.6	V
T_{STG}	Storage Temperature Range		-65	+150	°C
T_J	Maximum Junction Temperature			+150	°C
T_L	Lead Temperature (Soldering, 4 Seconds)			+260	°C
ESD	IEC 61000 Board Level			15.0	kV
	Human Body Model, JESD22-A114	All Pins		2.5	
		Serial I/0, /RES, PAR/SPI to GND		8.0	

Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to absolute maximum ratings.

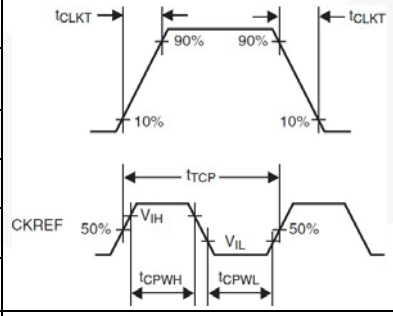
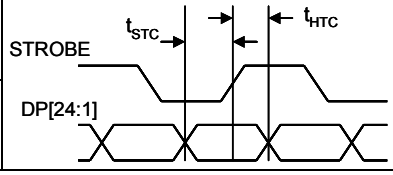
Symbol	Parameter	Min.	Max.	Unit
V_{DDA}, V_{DDS}[1]	Supply Voltage	2.5	3.3	V
V_{DDP}	Supply Voltage	1.65	3.60	V
T_A	Operating Temperature	-30	+70	°C

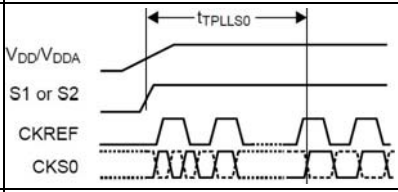
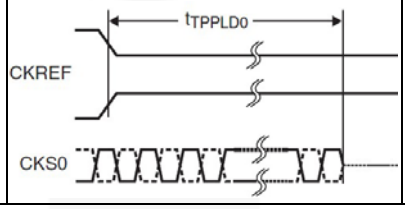
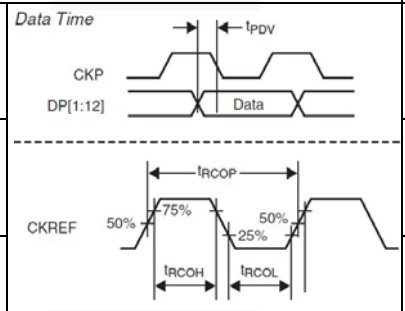
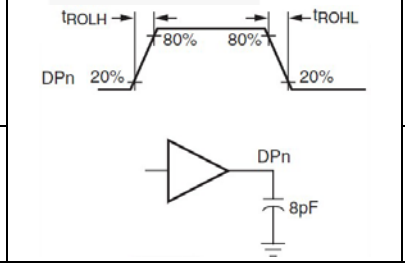
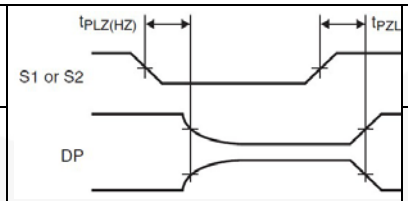
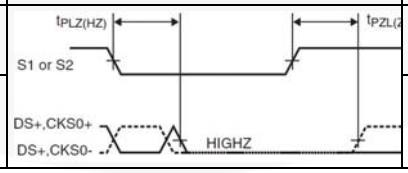
Note:

1. V_{DDA} and V_{DDS} supplies must be hardwired together to the same power supply.

Electrical Specifications

Values valid for over supply voltage and operating temperature ranges unless otherwise specified. Typical values are tested at T_A = 25°C and V_{DD} = 2.775V.

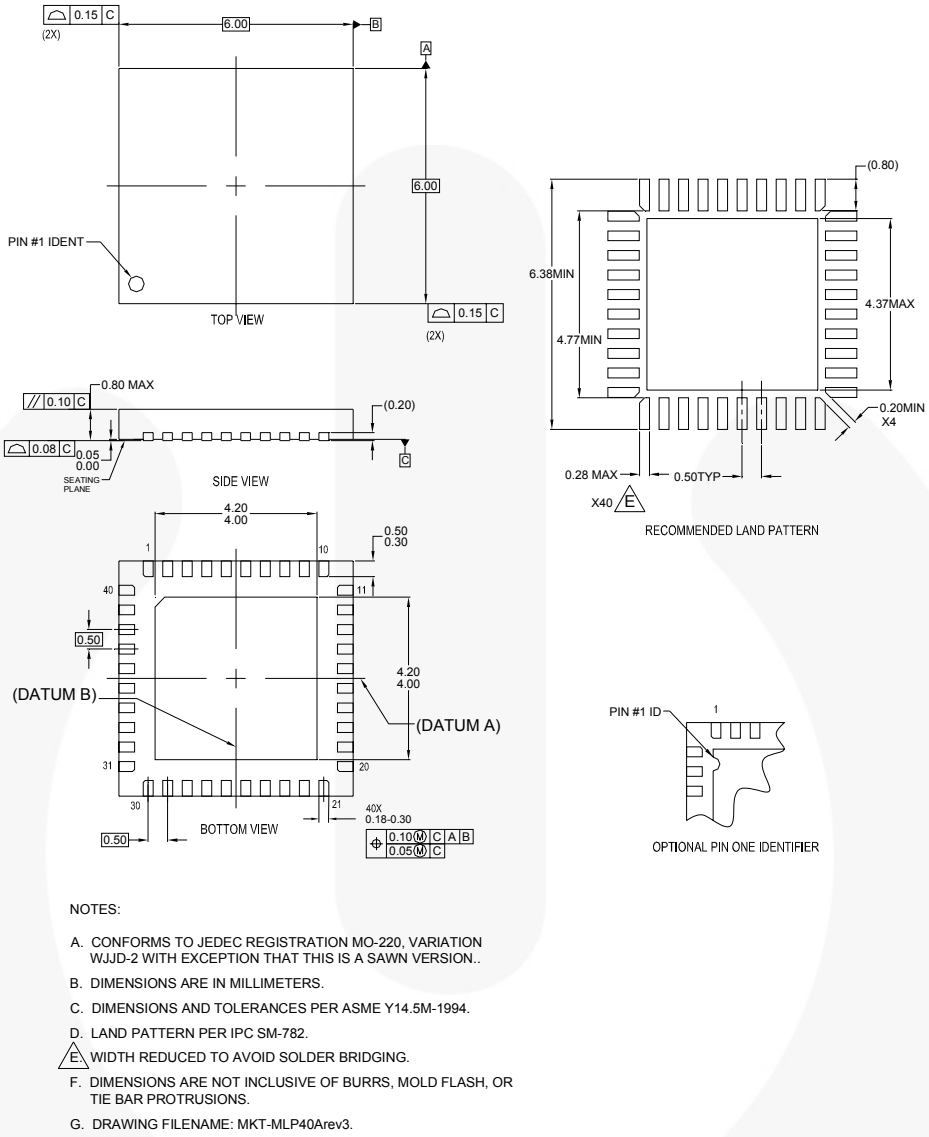
Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
DC Parallel I/O Characteristics							
V_{IH}	Input High Voltage			0.65 x V_{DDP}		V_{DDP}	V
V_{IL}	Input Low Voltage			GND		0.35 x V_{DDP}	V
V_{OH}	Output High Voltage	I_{OH} = -2.0mA	V_{DDP} = 3.3±0.30V	0.75 x V_{DDP}			V
			V_{DDP} = 2.5±0.20V				
			V_{DDP} = 1.8±0.18V				
V_{OL}	Output Low Voltage	I_{OH} = -2.0mA	V_{DDP} = 3.3±0.30V			0.25 x V_{DDP}	V
			V_{DDP} = 2.5±0.20V				
			V_{DDP} = 1.8±0.18V				
I_{IN}	Input Current			-5		5	µA
DC Serial Characteristics							
I_{ODH}	Output High Source Current				-1.75		mA
I_{ODL}	Output Low Source Current				0.95		mA
I_{OZ}	Disabled Output Leakage Current	CKSO, DSO = 0V to V_{DDS}, S2 = S1 = 0V			±1	±5	µA
I_{IZ}	Disabled Input Leakage Current	CKSO, DSO = 0V to V_{DDS}, S2 = S1 = 0V			±1	±5	
R_{TRM}	CKSI, DS Internal Receiver Termination Resistor				100		Ω
Z	Serial Transmission Line Impedance			70	100	130	Ω
Power Characteristics							
IDDA/S_{SER}	V_{DDA}, V_{DDS} Serializer Static Current	All DP and Control Inputs at 0V or No CKREF, DIRI = 1			4.5		mA
IDDA/S_{DES}	V_{DDA}, V_{DDS} Derializer Static Current	All DP and Control Inputs at 0V or No CKREF, DIRI = 0			5		mA
IDD_{SER}	Dynamic Serializer Current IDD_{SER} = IDDA + IDDS + IDDP	CKREF = STROBE, DIRI = 1	10MHz		11		mA
			20MHz		15		mA
IDD_{DES}	Dynamic Deserializer Current IDD_{SER} = IDDA + IDDS + IDDP	CKREF = STROBE, DIRI = 0	10MHz		7		mA
			20MHz		10		mA
IDD_PD	V_{DD} Power-Down Current IDD_PD = IDDA + IDDS + IDDP	S1 = S2 = 0 All Inputs at GND or V_{DD}			0.1		µA
AC Serializer, DIRI = 1 Specifications							
f_{MAX}	Maximum CKREF Frequency			2		20	MHz
f_{REF}	CKREF Frequency Relative to STROBE			1.1 x f_{STROBE}		20	MHz
t_{CPWH}	CKREF Clock HIGH Time			0.2	0.5		T
t_{CPWL}	CKREF Clock LOW Time			0.2	0.5		T
t_{CLKT}	LVCMOS Input Transition Time					90	ns
t_{SPWH}	STROBE Pulse Width HIGH/LOW			(Tx4) / 26		(Tx22) / 26	ns
t_{STC}	DP[n] Setup to STROBE			2.5			ns
t_{HTC}	DP[n] Hold to STROBE			2.0			ns

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
t_{TPLLS0}	Phase Lock Loop Stabilization Time				200	µs
t_{TPLLD0}	PLL Disable Time Loss of Clock				30	µs
AC Deserializer, DIRI = 0 Specifications						
t_{SKEW_DS-CKS}	Allowed DS-CKS Input Signal Skew		-150		150	ps
t_{RCOH}	CKP Out Low Time	 CKREF = STROBE, a = (1/f)/13	13a-3		13a+3	ns
t_{RCOH}	CKP Out High Time		13a-3		13a+13	ns
t_{PDV}	Data Valid to CKP Low		8a-6		8a+1	ns
t_{ROLH}	Output Rise Time (20% to 80%)			18		ns
t_{ROLH}	Output Fall Time (20% to 80%)			18		ns
AC Enable and Disable Timing						
$t_{PLZ(HZ)}$	Deserializer Disable Time				25	ns
$t_{PZL(ZH)}$	Deserializer Enable Time				2	µs
$t_{PLZ(HZ)}$	Serializer Disable Time				25	ns
$t_{PZL(ZH)}$	Serializer Enable Time				65	ns

Notes:

2. Skew is measured from either the rising or falling edge of CKSO clock to the rising or falling edge of DSO. Signals are edge aligned. Both outputs should have identical load condtions for this test to be valid.
3. If CKREF is not equal to STROBE for the serializer, the CKP signal does not maintain a 50% duty cycle. The low time of CKP remains 13 bit times.

Physical Dimensions



NOTES:

A. CONFORMS TO JEDEC REGISTRATION MO-220, VARIATION WJJD-2 WITH EXCEPTION THAT THIS IS A SAWN VERSION..

B. DIMENSIONS ARE IN MILLIMETERS.

C. DIMENSIONS AND TOLERANCES PER ASME Y14.5M-1994.

D. LAND PATTERN PER IPC SM-782.

E. WIDTH REDUCED TO AVOID SOLDER BRIDGING.

F. DIMENSIONS ARE NOT INCLUSIVE OF BURRS, MOLD FLASH, OR TIE BAR PROTRUSIONS.

G. DRAWING FILENAME: MKT-MLP40Arev3.

Figure 6. 40-Lead, Molded Leadless Package (MLP), Quad, JEDEC MO-220, 6mm Square

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Ordering Information

Part Number	Operating Temperature Range	Eco Status	Package	Packing Method
FIN224CMLX	-30 to +70°C	Green	40-Lead, Molded Leadless Package (MLP), Quad, JEDEC MO-220, 6mm Square	Tape & Reel

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Definition of Terms

Datasheet Identification	Product Status	Definition
Advance Information	Formative / In Design	Datasheet contains the design specifications for product development. Specifications may change in any manner without notice.
Preliminary	First Production	Datasheet contains preliminary data; supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve design.
No Identification Needed	Full Production	Datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve the design.
Obsolete	Not In Production	Datasheet contains specifications on a product that is discontinued by Fairchild Semiconductor. The datasheet is for reference information only.

Rev. I43

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