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FAIRCHILD SEMICONDUCTOR®

November 2009

µSerDes™ FIN424C / FIN425C
20-Bit Ultra-Low-Power Serializer / Deserializer for µController and RGB Displays

Features

Data & Control Bits	20
Frequency	10MHz
Capability	QVGA
Interface	Microcontroller / RGB
µController Usage	I86 & m68
Selectable Edge Rates	Yes
Dynamic Current	9mA / Pair
Standby Current	10µA
Core Voltage ($V_{DDA/S}$)	2.5 to 3.0V
I/O Voltage (V_{DDP})	1.6V to $V_{DDA/S}$
ESD	15KV (IEC)
Package	MLP-32 (5 x 5mm)
Ordering Information	FIN424CMLX
	FIN425CMLX

Applications

- Slider, Folder, and Clamshell Mobile Handsets
- GSM and CDMA Phones

Description

The FIN424C and FIN425C µSerDes™ are a low-power serializer/ deserializer pair that can help minimize the cost and power of an LCD interface. They are designed to operate transparently between the baseband processor and LCD. /WE and chip-select timing is maintained from the serializer to the deserializer. Through the use of serialization, the number of signals transferred from one point to another can be significantly reduced. Typical reduction is 5:1. Through the use of differential signaling, shielding, and EMI filters can also be minimized, further reducing the cost of serialization. Differential signaling is important for providing a noise-insensitive signal that can withstand radio and electrical noise sources. Major reduction in power consumption allows minimal impact on battery life in mobile applications.

Related Resources

For more information, please visit:
http://www.fairchildsemi.com/products/interface/userdes.html

Typical Application

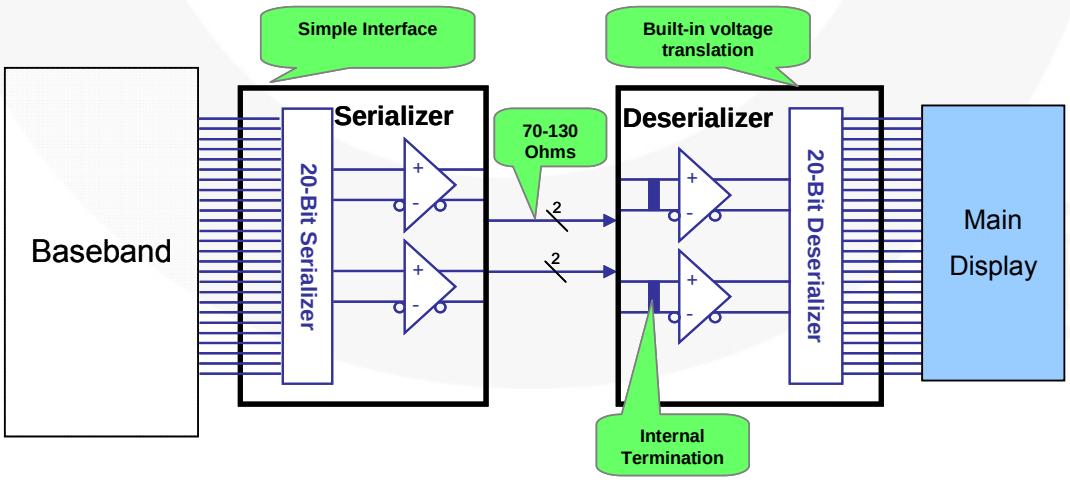


Figure 1. Mobile Phone Example

FIN424C Serializer Pin Descriptions

Pin Name	Description		
STRB	LVCMOS Strobe Signal for Latching Data into the Serializer (On Rising Edge)		
DP[19:0]	LVCMOS Data Input		
/RES	Low-Power Mode	0	Serializer Low Power
		1	Serializer Enabled
/STBY	SerDes Standby	0	Serializer and Deserializer in Low Power
		1	Serializer and Deserializer Enabled
Test	Internal Use (Should be GND)		
DS+, DS-	Serial Data Output		
CKS+, CKS-	Serial Clock Output		
VDDP	Power Supply for Parallel I/O and Internal Circuitry		
VDDS	Power Supply for Serial I/O		
VDDA	Power Supply for Core		
GND	Ground Pins		

Notes:
1. 0 = V_{IL}; 1 = V_{IH}.
2. All GND and VDDP pins must be connected to ground and VDDP, respectively.

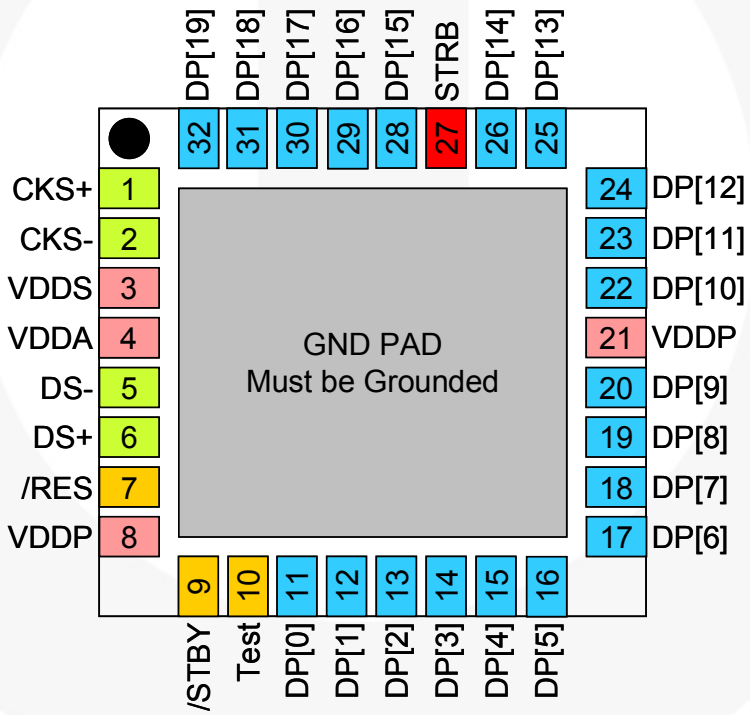


Figure 2. FIN424CMLX MLP-32 Pinout (Top Through View)

FIN425C Deserializer Pin Descriptions

Pin Name	Description		
WCLK	LVCMOS STRB Output		
DP[19:0]	LVCMOS Data Output		
/RES	Low-Power Mode	0	Deserializer Low Power
		1	Deserializer Enabled
SLEW	Parallel Output Edge Rate Control	0	Slow Output Edge Rates
		1	Fast Output Edge Rates
Test	Internal Use (Should be GND)		
DS+, DS-	Serial Data Input		
CKS+, CKS-	Serial Clock Input		
VDDP	Power Supply for Parallel I/O and internal circuitry		
VDDS	Power Supply for Serial I/O		
VDDA	Power Supply for Core		
GND	Ground Pins		

Notes:

3. 0 = V_{IL}; 1 = V_{IH}.
4. All GND and VDDP pins must be connected to ground and VDDP, respectively.

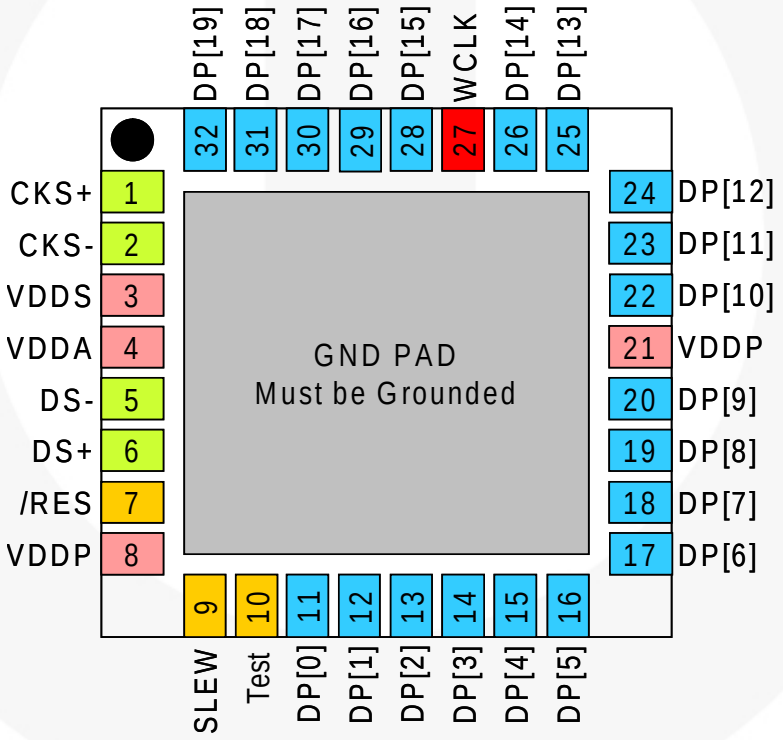


Figure 3. FIN425CMLX MLP-32 Pinout (Top Through View)

Table 1. Reset and Standby Modes / States

/RES FIN424C FIN425C	/STBY FIN424C	Mode	Pins	FIN424C Parallel Input State	FIN425C Parallel Output State
0	X	Reset Mode	DP[19:0]	Disabled	LOW
			STRB / WCLK	Disabled	HIGH
1	0	Standby Mode	DP[19:0]	Disabled	LAST STATE
			STRB / WCLK	Disabled	HIGH
1	1	Operating Mode	DP[19:0]	Enabled	ENABLED
			STRB / WCLK	Enabled	ENABLED

Application Diagram

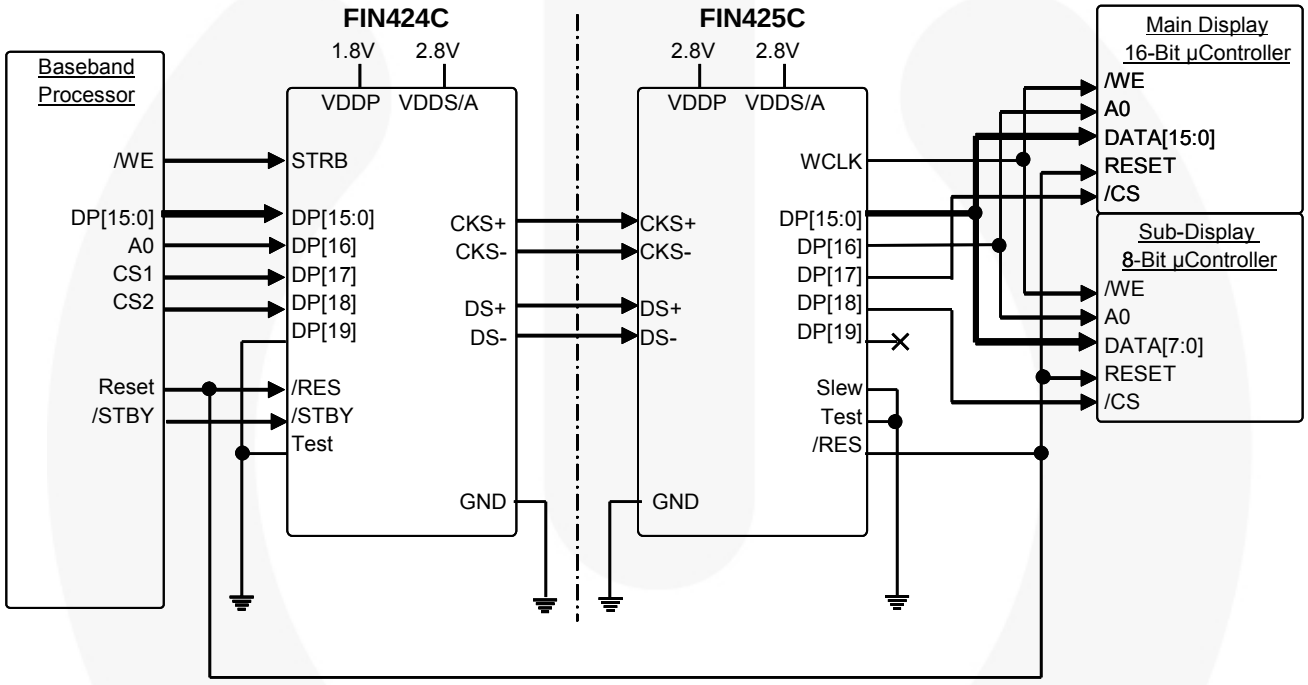


Figure 4. Dual-Display, 16-Bit, µController Interface

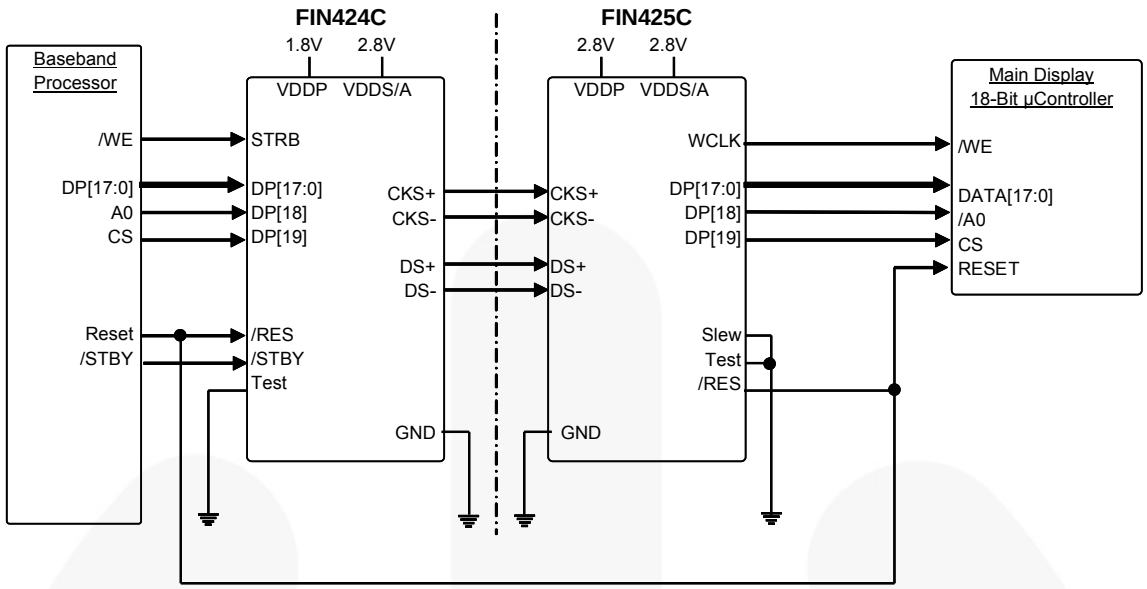


Figure 5. Single–Display, 18-Bit, µController Interface

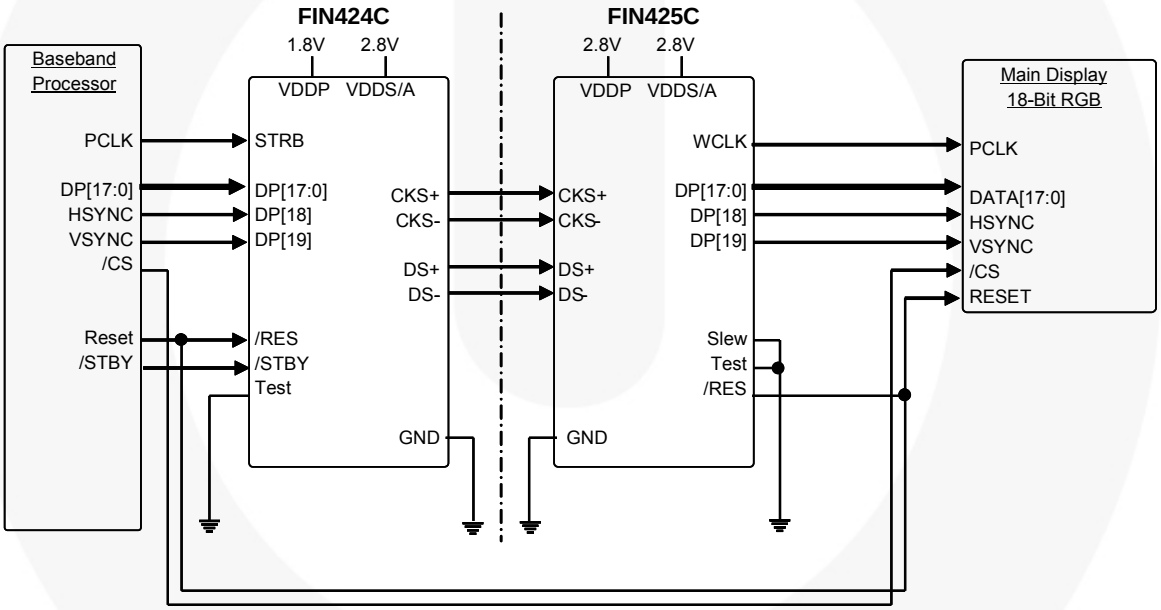


Figure 6. Single-Display, 18-Bit, RGB Interface

Additional Application Information

Flex Cabling: The serial I/O information is transmitted at a high serial rate. Care must be taken implementing this serial I/O flex cable. The following best practices should be used when developing the flex cabling or Flex PCB.

- Keep all four differential serial wires the same length.
- Do not allow noisy signals over or near differential serial wires. Example: No CMOS traces over differential serial wires.
- Use a design goal of 70 to 130Ω differential characteristic impedance.
- Do not place test points on differential serial wires.
- Design differential serial wires a minimum of 2cm away from the antenna.
- Visit Fairchild's website at http://www.fairchildsemi.com/products/interface/userdes.html, contact your sales representative, or contact Fairchild directly at interface@fairchildsemi.com for applications notes or flex guidelines.

Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Parameter		Min.	Max.	Unit
V_{DD}	Supply Voltage		-0.5	+3.6	V
V_{IO}	All Input / Output Voltage		-0.5	V_{DDP}+0.5	V
T_{STG}	Storage Temperature Range		-65	+150	°C
T_J	Maximum Junction Temperature			+150	°C
T_L	Lead Temperature (Soldering, Four Seconds)			+260	°C
ESD	IEC 61000 Board Level			15.0	kV
	Human Body Model, JESD22-A114	All Pins		7.5	
		Serial I/O, /RES, PAR/SPI to GND		14.0	

Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to absolute maximum ratings.

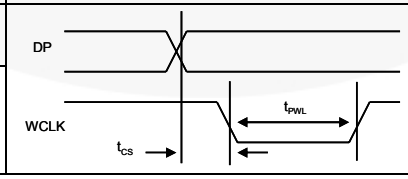
Symbol	Parameter	Min.	Max.	Unit
V_{DDA}, V_{DDS}[5]	Supply Voltage	2.5	3.0	V
V_{DDP}	Supply Voltage	1.6	$V_{DDA/S}$	V
T_A	Operating Temperature	-30	+85	°C

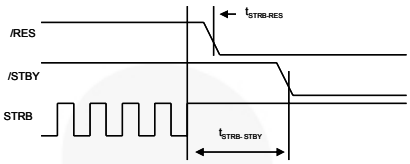
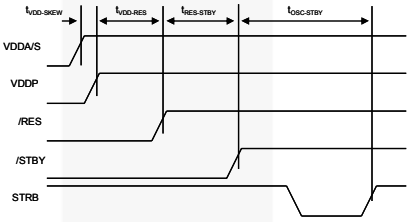
Notes:

5. V_{DDA} and V_{DDS} supplies must be hardwired together to the same power supply. V_{DDP} must be less than or equal to V_{DDA}/V_{DDS}.
6. Typical values are tested at T_A=25°C and 2.75V.

Electrical Specifications

Values valid for over-supply voltage and operating temperature ranges unless otherwise specified.

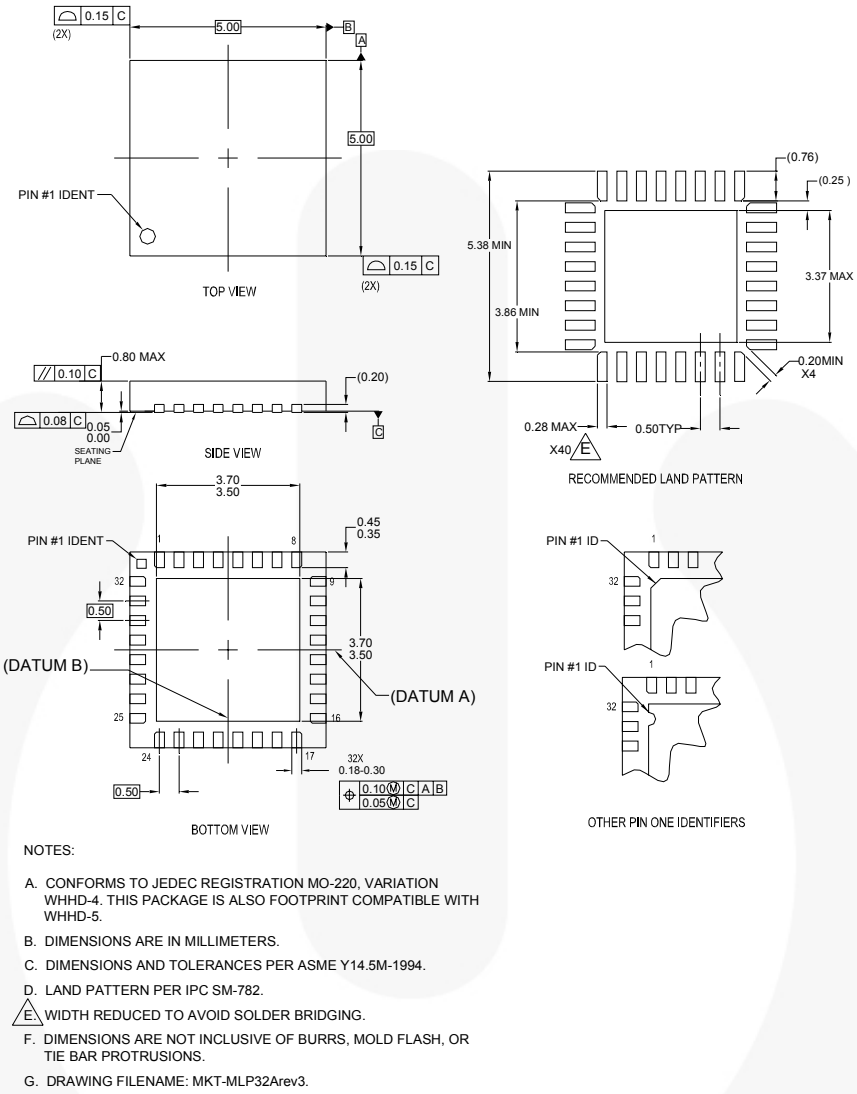
Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
DC Parallel I/O and Serial Characteristics						
V_{IH}	Input High Voltage		0.7 x V_{DDP}		V_{DDP}	V
V_{IL}	Input Low Voltage		GND		0.3 x V_{DDP}	V
V_{OH}	Output High Voltage	SLEW=0 I_{OH}=-250µA	0.8 x V_{DDP}			V
		SLEW=1 I_{OH}=-1mA				
V_{OL}	Output Low Voltage	SLEW=0 I_{OL}=250µA			0.2 x V_{DDP}	V
		SLEW=1 I_{OL}=1mA				
I_{IN}	Input Current		-5		5	µA
V_{GO}	Serial Input Voltage Ground Offset	FIN425C to FIN424C		0		V
Z	Serial Transmission Line Impedance		70	100	130	Ω
Power Characteristics						
$I_{DYN\_FIN424C}$	Dynamic Current FIN424C	$V_{DDA/S}$=2.75V, V_{DDP}=1.8V, /STBY=1, /RES=1, 5.44MHz		4		mA
$I_{DYN\_FIN425C}$	Dynamic Current FIN425C	$V_{DDA/S}$=2.75V V_{DDP}=1.8V, /STBY=1, /RES=1, C_L=0pF, 5.44MHz		5		mA
$I_{BRST\_FIN424C}$	Burst Standby Current FIN424C	$V_{DDA/S}$=2.75V, V_{DDP}=1.8V, /STBY=1, /RST=1, No STROBE Signal,		1.3		mA
$I_{BRST\_FIN425C}$	Burst Standby Current FIN425C	$V_{DDA/S}$=2.75V, V_{DDP}=1.8V, /STBY=1, /RST=1, No STROBE Signal, C_L=0pF		1.8		mA
I_{STBY}	Standby Current	FIN424C / FIN425C $V_{DDS/A}$=V_{DDP}=3.0V, /STBY=0, /RST=1			10	µA
I_{RES}	Reset Current	FIN424C / FIN425C $V_{DDS/A}$=V_{DDP}=3.0V, /RST=0			10	µA
AC FIN424C Specifications						
f_{WSTRB0}	Strobe Frequency		0		10	MHz
t_R, t_F	Input Edge Rates				40	ns
t_{S1}	DP Setup Time	DP Before STRBn ↑(7)	5			ns
t_{H1}	DP Hold Time	DP After STRBn ↑(7)	15			ns
AC FIN425C Specifications						
t_{R0}, t_{F0}	Output Edge Rates of WCLK	SLEW=0, CL=5pF 20% to 80%(7)	8		17	ns
		SLEW=1, C_L=5pF 20% to 80%(7)			10	
t_{R1}, t_{F1}	Output Edge Rates of DP[19:0]	SLEW=0, C_L=5pF 20% to 80%(7)	8		22	ns
		SLEW=1, C_L=5pF 20% to 80%(7)			17	
tcs	DP[19:0] to Falling edge of WCLK C_L=5pF 20% to 80%		0	4		
t_{PWL}	WCLK Output Pulse Width Low, Measured 30% to 30%(7)		50	56		ns
AC Oscillator Specifications						
f_{OSC}	Serial Operating Frequency		240	275	310	MHz
$t_{OSC-STBY}$	Oscillator Stabilization Time After Standby	V_{DDA}=V_{DDS}=2.75V /RES=1, /STBY ↑ Transition		15	30	µs

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{OSC-RES}$	Oscillator Stabilization Time After Reset	V_{DDA}=V_{DDS}=2.75V /STBY=1, /RES ↑ Transition		30	50	µs
AC Reset and Standby Timing						
$t_{STRB-RES}$	/RES after last STRBn ↑		0			ns
$t_{STRB-STBY}$	Standby Time After Last Strobe		200			ns
$t_{VDD-SKEW}$	Allowed Power up Skew between V_{DDP} and $V_{DDA/S}$		-∞		+∞	ms
$t_{VDD-RES}$	Minimum Reset Low Time After V_{DD} Stable		20			µs
$t_{RES-STBY}$	/STBY Wait Time After /RES ↑		20			µs

Note:

7. Characterized, but not production tested.

Physical Dimensions



NOTES:

A. CONFORMS TO JEDEC REGISTRATION MO-220, VARIATION WHHD-4. THIS PACKAGE IS ALSO FOOTPRINT COMPATIBLE WITH WHHD-5.

B. DIMENSIONS ARE IN MILLIMETERS.

C. DIMENSIONS AND TOLERANCES PER ASME Y14.5M-1994.

D. LAND PATTERN PER IPC SM-782.

E. WIDTH REDUCED TO AVOID SOLDER BRIDGING.

F. DIMENSIONS ARE NOT INCLUSIVE OF BURRS, MOLD FLASH, OR TIE BAR PROTRUSIONS.

G. DRAWING FILENAME: MKT-MLP32Arev3.

Figure 7. 32-Lead, Molded Leadless Package (MLP), QUAD, JEDEC MO-220, Variation WHHD-4, 5mm Square

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Always visit Fairchild Semiconductor's online packaging area for the most recent package drawings:
http://www.fairchildsemi.com/packaging/.

Ordering Information

Part Number	Operating Temperature Range	Eco Status	Package	Packing Method
FIN424CMLX	-30 to +85°C	Green	32-Lead, Molded Leadless Package (MLP), QUAD, JEDEC MO-220, Variation WHHD-4, 5mm Square	Tape and Reel
FIN425CMLX	-30 to +85°C	Green	32-Lead, Molded Leadless Package (MLP), QUAD, JEDEC MO-220, Variation WHHD-4, 5mm Square	Tape and Reel

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PRODUCT STATUS DEFINITIONS

Definition of Terms

Datasheet Identification	Product Status	Definition
Advance Information	Formative / In Design	Datasheet contains the design specifications for product development. Specifications may change in any manner without notice.
Preliminary	First Production	Datasheet contains preliminary data; supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve design.
No Identification Needed	Full Production	Datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve the design.
Obsolete	Not In Production	Datasheet contains specifications on a product that is discontinued by Fairchild Semiconductor. The datasheet is for reference information only.

Rev. I43

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