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Please note: As part of the Fairchild Semiconductor integration, some of the Fairchild orderable part numbers will need to change in order to meet ON Semiconductor's system requirements. Since the ON Semiconductor product management systems do not have the ability to manage part nomenclature that utilizes an underscore (_), the underscore (_) in the Fairchild part numbers will be changed to a dash (-). This document may contain device numbers with an underscore (_). Please check the ON Semiconductor website to verify the updated device numbers. The most current and up-to-date ordering information can be found at www.onsemi.com. Please email any questions regarding the system integration to Fairchild_questions@onsemi.com.

FAIRCHILD SEMICONDUCTOR®

June 2013

FJD5555

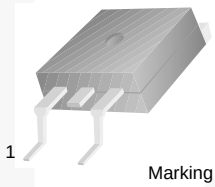
NPN Silicon Transistor

Features

- Fast Speed Switching
- Wide Safe Operating Area
- High Voltage Capability

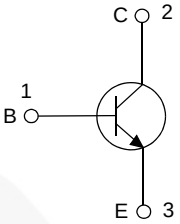
Application

- Electronic Ballast
- Switch Mode Power Supplies



Marking : J5555

1. Base 2. Collector 3. Emitter



Ordering Information

Part Number	Marking	Package	Packing Method
FJD5555TM	J5555	D-PAK	Tape & Reel

Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only. Values are at T_A = 25°C unless otherwise noted.

Symbol	Parameter	Value	Units
BV_{CBO}	Collector-Base Voltage	1050	V
BV_{CEO}	Collector-Emitter Voltage	400	V
BV_{EBO}	Emitter-Base Voltage	14	V
I_C	Collector Current (DC)	5	A
I_{CP}	Collector Current (Pulse)	10	A
I_B	Base Current (DC)	2	A
I_{BP}	Base Current (Pulse)	4	A
T_J	Junction Temperature	150	°C
T_{STG}	Storage Junction Temperature Range	- 55 to +150	°C

Thermal Characteristics

Values are at T_A = 25°C unless otherwise noted.

Symbol	Parameter		Value	Units
P_D	Total Device Dissipation	T_A = 25°C	1.34	W
		T_C = 25°C	100	W
$R_{\theta ja}$ (1)	Thermal Resistance, Junction to Ambient		95	°C/W
$R_{\theta jc}$ (2)	Thermal Resistance, Junction to Case		1.25	°C/W

Notes:

1. $R_{\theta ja}$ test board and fixture under natural convection; JESD51-3 recommended thermal test board.
2. $R_{\theta jc}$ test fixture under infinite cooling condition.

Electrical Characteristics[3]

Values are at T_A = 25°C unless otherwise noted.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
BV_{CBO}	Collector-Base Breakdown Voltage	I_C = 500 μA, I_E = 0	1050			V
BV_{CEO}	Collector-Emitter Breakdown Voltage	I_C = 5 mA, I_B = 0	400			V
BV_{EBO}	Emitter-Base Breakdown Voltage	I_E = 500 μA, I_C = 0	14			V
h_{FE}	DC Current Gain	V_{CE} = 5 V, I_C = 10 mA	10			
		V_{CE} = 3 V, I_C = 0.8 A	20		40	
V_{CE}(sat)	Collector-Emitter Saturation Voltage	I_C = 1 A, I_B = 0.2 A		0.17	0.50	V
		I_C = 3.5 A, I_B = 1.0 A			1.5	V
V_{BE}(sat)	Base-Emitter Saturation Voltage	I_C = 3.5 A, I_B = 1.0 A			1.2	V
C_{ob}	Output Capacitance	V_{CB} = 10 V, f = 1 MHz		45		pF
t_{ON}	Turn-On Time	V_{CC} = 125 V, I_C = 0.5 A, I_{B1} = 45 mA, I_{B2} = -0.5 A, R_L = 250 Ω			1.0	μs
t_{STG}	Storage Time				1.2	μs
t_F	Fall Time			0.3		μs
t_{ON}	Turn-On Time	V_{CC} = 250 V, I_C = 2.5 A, I_{B1} = 0.5 A, I_{B2} = -1.0 A, R_L = 100 Ω			2.0	μs
t_{STG}	Storage Time				2.5	μs
t_F	Fall Time				0.3	μs
EAS	Avalanche Energy	L = 2 mH	6			mJ

Note:

3. Pulse test: pulse width ≤ 300 μs, duty cycle ≤ 2%.

Typical Performance Characteristics

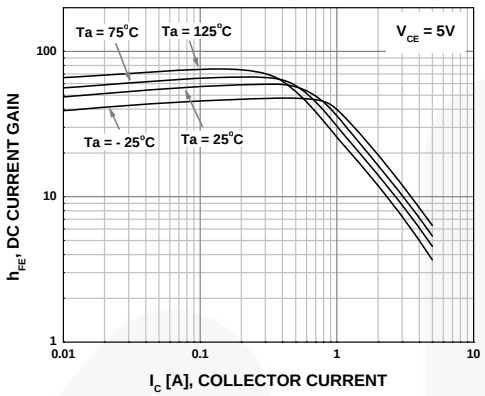


Figure 1. DC Current Gain

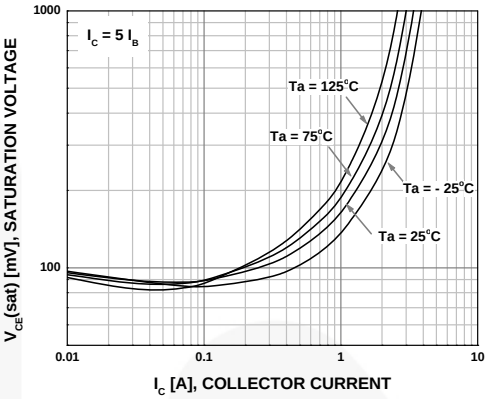


Figure 2. Saturation Voltage

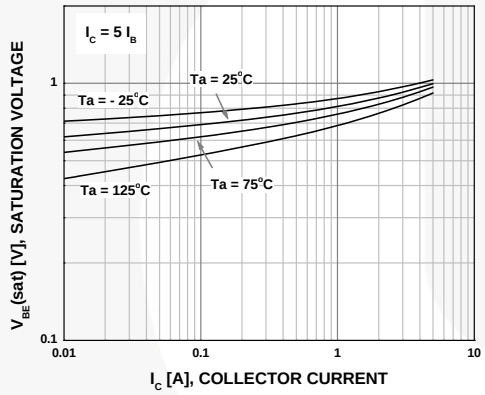


Figure 3. Saturation Voltage

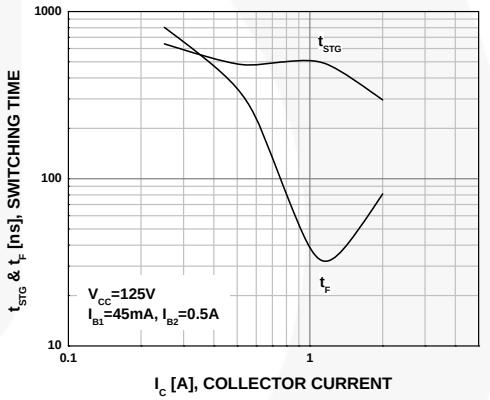


Figure 4. Resistive Load Switching

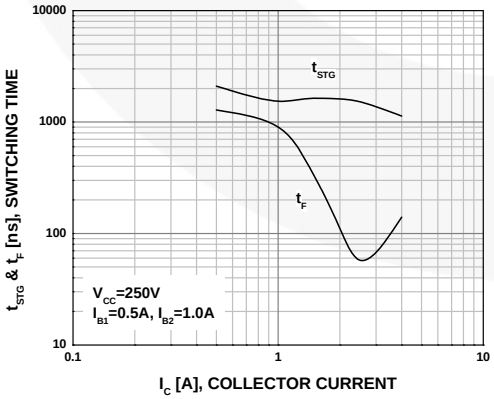


Figure 5. Resistive Load Switching

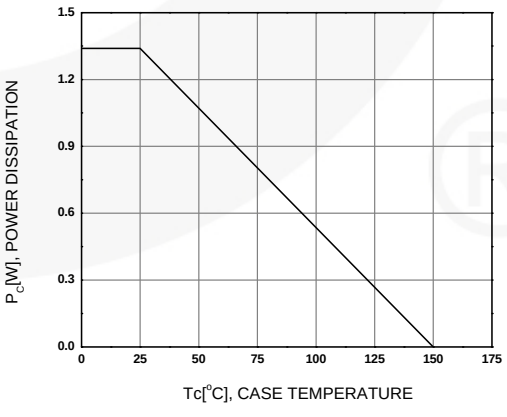


Figure 6. Power Derating

Typical Performance Characteristics (Continued)

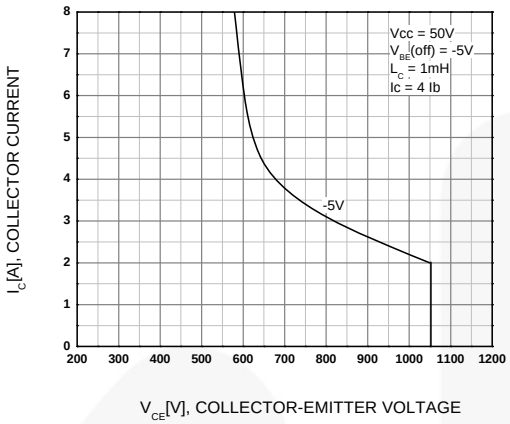


Figure 7. Reverse Bias Safe Operating

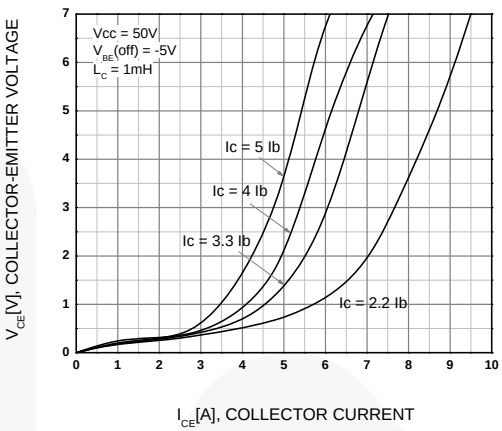
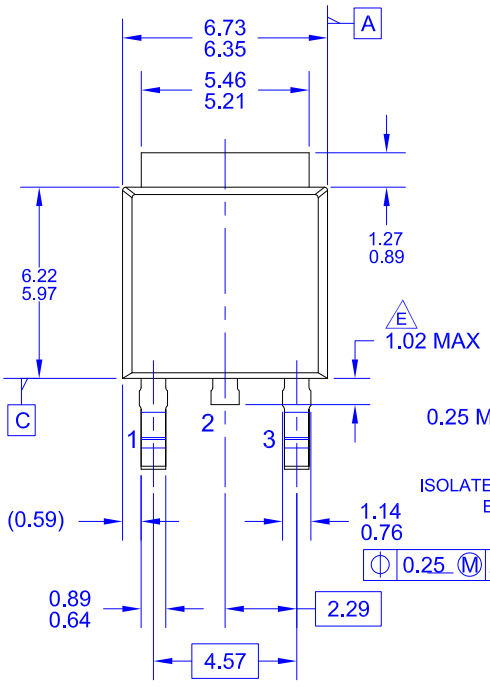
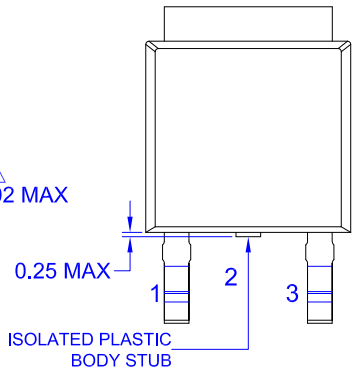


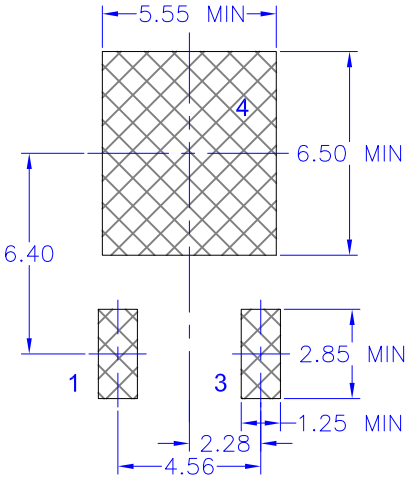
Figure 8. V_{CE} Saturation vs. h_{FE}



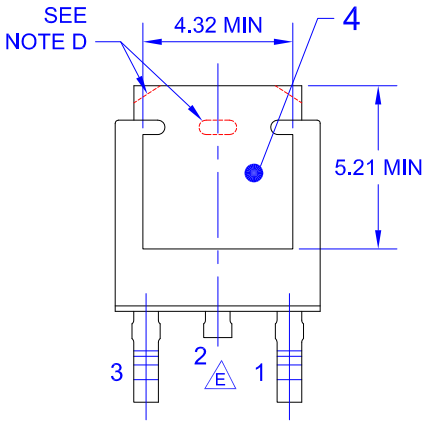
NON-DIODE PRODUCTS VERSION



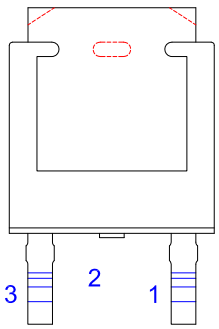
DIODE PRODUCTS VERSION



LAND PATTERN RECOMMENDATION



NON-DIODE PRODUCTS VERSION



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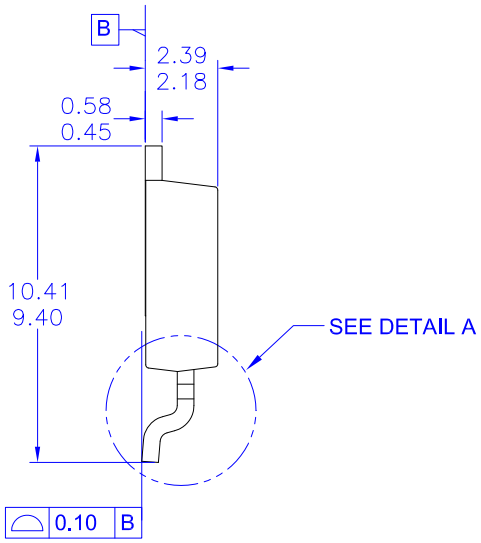
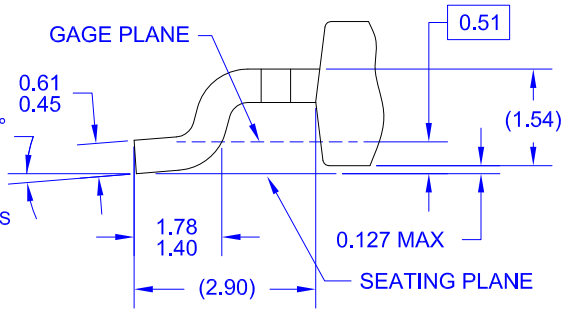


NOTES: UNLESS OTHERWISE SPECIFIED

A) THIS PACKAGE CONFORMS TO JEDEC, TO-252, ISSUE C, VARIATION AA.
B) ALL DIMENSIONS ARE IN MILLIMETERS.
C) DIMENSIONING AND TOLERANCING PER ASME Y14.5M-2009.
D) SUPPLIER DEPENDENT MOLD LOCKING HOLES OR CHAMFERED CORNERS OR EDGE PROTRUSION.
E) TRIMMED METAL CENTER LEAD IS PRESENT ON FOR NON-DIODE PRODUCTS
F) DIMENSIONS ARE EXCLUSIVE OF BURS, MOLD FLASH AND TIE BAR EXTRUSIONS.
G) LAND PATTERN RECOMMENDATION IS BASED ON IPC7351A STD TO228P991X239-3N.
H) DRAWING NUMBER AND REVISION: MKT-TO252A03REV11



DETAIL A
(ROTATED -90°)
SCALE: 12X

FAIRCHILD

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