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September 2014

FOD8321
2.5A Output Current, Gate Drive Optocoupler in Optoplanar® Wide Body SOP 5-Pin

Features

- Fairchild's Optoplanar® Packaging Technology Provides Reliable and High-Voltage Insulation with Greater than 8 mm Creepage and Clearance Distance, and 0.5 mm Internal Insulation Distance While Still Offering a Compact Footprint
- 2.5 A Output Current Driving Capability for Medium-Power IGBT/MOSFET
  - P-Channel MOSFETs at Output Stage Enables Output Voltage Swing Close to Supply Rail
- 20 kV/µs Minimum Common Mode Rejection
- Wide Supply Voltage Range: 15 V to 30 V
- Fast Switching Speed Over Full Operating Temperature Range:
  - 500 ns Maximum Propagation Delay
  - 300 ns Maximum Pulse Width Distortion
- Under-Voltage Lockout (UVLO) with Hysteresis
- Extended Industrial Temperate Range: -40°C to 100°C
- Safety and Regulatory Approvals:
  - UL1577, 5,000 V_{RMS} for 1 Minute
  - DIN EN/IEC60747-5-5, 1,414 V Peak Working Insulation Voltage

Applications

- AC and Brushless DC Motor Drives
- Industrial Inverter
- Uninterruptible Power Supply
- Induction Heating
- Isolated IGBT/Power MOSFET Gate Drive

Related Resources

- *FOD3120, High Noise Immunity, 2.5 A Output Current, Gate Drive Optocoupler Datasheet*
- *www.fairchildsemi.com/products/opto/*

Description

The FOD8321 is a 2.5 A output current gate drive optocoupler, capable of driving medium-power IGBT/MOSFETs. It is ideally suited for fast-switching driving of power IGBT and MOSFET used in motor-control inverter applications and high-performance power systems.

The FOD8321 utilizes Fairchild's Optoplanar® coplanar packaging technology and optimized IC design to achieve reliable high-insulation voltage and high-noise immunity.

It consists of an Aluminum Gallium Arsenide (AlGaAs) Light-Emitting Diode (LED) optically coupled to an integrated circuit with a high-speed driver for push-pull MOSFET output stage. The device is housed in a wide body, 5-pin, small-outline, plastic package.

Functional Schematic

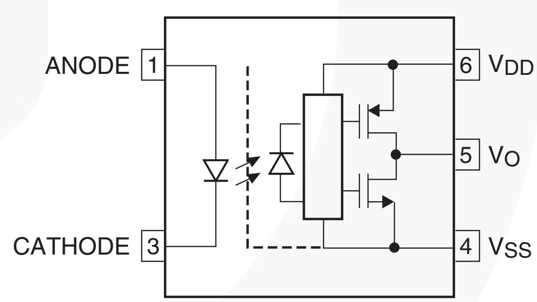


Figure 1. Schematic

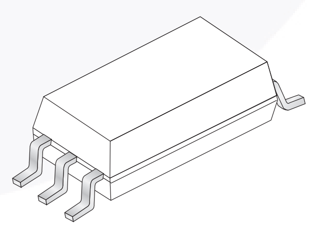


Figure 2. Package Outline

Truth Table

LED	$V_{DD} - V_{SS}$ "Positive Going" (Turn-on)	$V_{DD} - V_{SS}$ "Positive Going" (Turn-off)	V_O
Off	0 V to 30 V	0 V to 30 V	LOW
On	0 V to 11.5 V	0 V to 10 V	LOW
On	11.5 V to 14.5 V	10 V to 13 V	Transition
On	14.5 V to 30 V	13 V to 30 V	HIGH

Pin Configuration

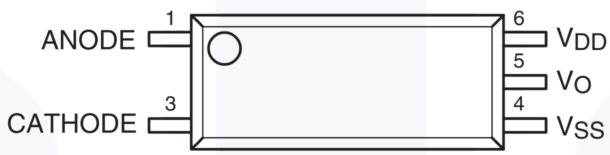


Figure 3. Pin Configuration

Pin Definitions

Pin #	Name	Description
1	Anode	LED Anode
3	Cathode	LED Cathode
4	V_{SS}	Negative Supply Voltage
5	V_O	Output Voltage
6	V_{DD}	Positive Supply Voltage

Safety and Insulation Ratings

As per DIN EN/IEC60747-5-5, this optocoupler is suitable for “safe electrical insulation” only within the safety limit data. Compliance with the safety ratings shall be ensured by means of protective circuits.

Symbol	Parameter	Min.	Typ.	Max.	Unit
	Installation Classifications per DIN VDE 0110/1.89 Table 1				
	For Rated Mains Voltage < 150 V_{RMS}		I–IV		
	For Rated Mains Voltage < 300 V_{RMS}		I–IV		
	For Rated Mains Voltage < 450 V_{RMS}		I–IIII		
	For Rated Mains Voltage < 600 V_{RMS}		I–III		
	Climatic Classification		40/100/21		
	Pollution Degree (DIN VDE 0110/1.89)		2		
CTI	Comparative Tracking Index	175			
V_{PR}	Input-to-Output Test Voltage, Method b, V_{IORM} x 1.875 = V_{PR}, 100% Production Test with t_m = 1 s, Partial Discharge < 5 pC	2651			V_{peak}
	Input-to-Output Test Voltage, Method a, V_{IORM} x 1.6 = V_{PR}, Type and Sample Test with t_m = 10 s, Partial Discharge < 5 pC	2262			V_{peak}
V_{IORM}	Maximum Working Insulation Voltage	1414			V_{peak}
V_{IOTM}	Highest Allowable Over Voltage	8000			V_{peak}
	External Creepage	8.0			mm
	External Clearance	8.0			mm
	Insulation Thickness	0.5			mm
	Safety Limit Values – Maximum Values Allowed in the Event of a Failure				
T_S	Case Temperature	150			°C
$I_{S,INPUT}$	Input Current	200			mA
$P_{S,OUTPUT}$	Output Power	600			mW
R_{IO}	Insulation Resistance at T_S, V_{IO} = 500 V	10^9			Ω

Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only. T_A = 25ºC unless otherwise specified.

Symbol	Parameter	Value	Units
T_{STG}	Storage Temperature	-40 to +125	°C
T_{OPR}	Operating Temperature	-40 to +100	°C
T_J	Junction Temperature	-40 to +125	°C
T_{SOL}	Lead Solder Temperature *Refer to Reflow Temperature Profile on page 15.*	260 for 10 s	°C
$I_{F(AVG)}$	Average Input Current	25	mA
F	Operating Frequency	50	kHz
V_R	Reverse Input Voltage	5.0	V
$I_{O(PEAK)}$	Peak Output Current(1)	3.0	A
V_{DD}	Supply Voltage	0 to 35	V
$V_{O(PEAK)}$	Peak Output Voltage	0 to V_{DD}	V
$t_{R(IN)}$, $t_{F(IN)}$	Input Signal Rise and Fall Time	500	ns
PD_I	Input Power Dissipation(2)(4)	45	mW
PD_O	Output Power Dissipation(3)(4)	500	mW

Notes:
1. Maximum pulse width = 10 µs, maximum duty cycle = 0.2%.
2. No derating required across operating temperature range.
3. Derate linearly from 25°C at a rate of 5.2 mW/°C
4. Functional operation under these conditions is not implied. Permanent damage may occur if the device is subjected to conditions outside these ratings.

Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to absolute maximum ratings.

Symbol	Parameter	Min.	Max.	Unit
T_A	Ambient Operating Temperature	-40	100	°C
$V_{DD} – V_{SS}$	Supply Voltage	16	30	V
$I_{F(ON)}$	Input Current (ON)	10	16	mA
$V_{F(OFF)}$	Input Voltage (OFF)	0	0.8	V

Isolation Characteristics

Apply over all recommended conditions, typical value is measured at T_A = 25ºC

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
V_{ISO}	Input-Output Isolation Voltage	T_A = 25ºC, R.H. < 50%, t = 60 s, $I_{I-O} \leq$ 20 µA, 50 Hz(5)(6)	5,000			V_{RMS}
R_{ISO}	Isolation Resistance	V_{I-O} = 500 V(5)		10^{11}		Ω
C_{ISO}	Isolation Capacitance	V_{I-O} = 0V , Frequency = 1.0 MHz(6)		1		pF

Notes:

5. Device is considered a two terminal device: pins 1 and 3 are shorted together and pins 4, 5 and 6 are shorted together.
6. 5,000 VAC_{RMS} for 1 minute duration is equivalent to 6,000 VAC_{RMS} for 1 second duration.

Electrical Characteristics

Apply over all recommended conditions, typical value is measured at V_{DD} = 30 V, V_{SS} = Ground, T_A = 25°C unless otherwise specified.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units	Figure
V_F	Input Forward Voltage	I_F = 10 mA	1.1	1.5	1.8	V	19
$\Delta(V_F / T_A)$	Temperature Coefficient of Forward Voltage			-1.8		mV/°C	
BV_R	Input Reverse Breakdown Voltage	I_R = 10 µA	5			V	
C_{IN}	Input Capacitance	f = 1 MHz, V_F = 0 V		60		pF	
I_{OH}	High Level Output Current(1)	$V_{OH} = V_{DD}$ – 3 V	1.0	2.0	2.5	A	4, 6
		$V_{OH} = V_{DD}$ – 6 V	2.0		2.5	A	4, 6, 22
I_{OL}	Low Level Output Current(1)	$V_{OL} = V_{SS}$ + 3 V	1.0	2.0	2.5	A	7, 9
		$V_{OL} = V_{SS}$+ 6 V	2.0		2.5	A	7, 9, 21
V_{OH}	High Level Output Voltage(7)(8)	I_F = 10 mA, I_O = -2.5 A	V_{DD} – 6.25	V_{DD} – 2.5		V	4
		I_F = 10 mA, I_O = -100 mA	V_{DD} – 0.5	V_{DD} – 0.1		V	4, 5, 23
V_{OL}	Low Level Output Voltage(7)(8)	I_F = 10 mA, I_O = 2.5 A		V_{SS} + 2.5	V_{SS} + 6.25	V	7
		I_F = 0 mA, I_O = 100 mA		V_{SS} + 0.1	V_{SS} + 0.5	V	8, 24
I_{DDH}	High Level Supply Current	V_O Open, I_F = 10 to 16 mA		2.9	5	mA	10, 11, 25
I_{DDL}	Low Level Supply Current	V_O Open, V_F = 0 to 0.8 V		2.8	5	mA	10, 11, 26
I_{FLH}	Threshold Input Current Low to High	I_O = 0 mA, V_O > 5 V		2.4	7.5	mA	12, 18, 27
V_{FHL}	Threshold Input Voltage High to Low	I_O = 0 mA, V_O < 5 V	0.8			V	28
V_{UVLO+}	UnderVoltage Lockout Threshold	I_F = 10 mA, V_O > 5 V	11.5	12.7	14.5	V	20, 29
V_{UVLO-}		I_F = 10 mA, V_O < 5 V	10.0	11.2	13.0	V	20, 29
$UVLO_{HYS}$	UnderVoltage Lockout Threshold Hysteresis			1.5		V	

Notes:

7. In this test, V_{OH} is measured with a dc load current of 100 mA. When driving capacitive load V_{OH} will approach V_{DD} as I_{OH} approaches 0 A.
8. Maximum pulse width = 1 ms, maximum duty cycle = 20%.

Switching Characteristics

Apply over all recommended conditions, typical value is measured at V_{DD} = 30V, V_{SS} = Ground, T_A = 25°C unless otherwise specified.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units	Figure
t_{PHL}	Propagation Delay Time to Logic Low Output[9]	I_F = 10 mA to 16 mA, R_g = 10 Ω, C_g = 10 nF, f = 10 kHz, Duty Cycle = 50%	100	285	500	ns	13, 14, 15, 16, 17, 30
t_{PLH}	Propagation Delay Time to Logic High Output[10]		100	260	500	ns	13, 14, 15, 16, 17, 20
PWD	Pulse Width Distortion[11] $\lvert t_{PHL} - t_{PLH} \rvert$			25	300	ns	
PDD (Skew)	Propagation Delay Difference Between Any Two Parts[12]		-350		350		
t_R	Output Rise Time (10% to 90%)			60		ns	30
t_F	Output Fall Time (90% to 10%)			60		ns	30
$t_{ULVO\ ON}$	ULVO Turn On Delay	I_F = 10 mA, V_O > 5 V		0.8		µs	
$t_{ULVO\ OFF}$	ULVO Turn Off Delay	I_F = 10 mA, V_O < 5 V		0.4		µs	
$\lvert CM_H \rvert$	Common Mode Transient Immunity at Output High	T_A = 25°C, V_{DD} = 30 V, I_F = 10 mA to 16 mA, V_{CM} = 2000 V[13]	20	50		kV/µs	31
$\lvert CM_L \rvert$	Common Mode Transient Immunity at Output Low	T_A = 25°C, V_{DD} = 30 V, V_F = 0 V, V_{CM} = 2000 V[14]	20	50		kV/µs	31

Notes:

9. Propagation delay t_{PHL} is measured from the 50% level on the falling edge of the input pulse to the 50% level of the falling edge of the V_O signal.
10. Propagation delay t_{PLH} is measured from the 50% level on the rising edge of the input pulse to the 50% level of the rising edge of the V_O signal.
11. PWD is defined as $\lvert t_{PHL} - t_{PLH} \rvert$ for any given device.
12. The difference between t_{PHL} and t_{PLH} between any two FOD8321 parts under the same operating conditions, with equal loads.
13. Common mode transient immunity at output high is the maximum tolerable negative dVcm/dt on the trailing edge of the common mode impulse signal, V_{CM}, to ensure that the output remains high (i.e., V_O > 15.0 V).
14. Common mode transient immunity at output low is the maximum tolerable positive dVcm/dt on the leading edge of the common pulse signal, V_{CM}, to ensure that the output remains low (i.e., V_O < 1.0 V).

Typical Performance Characteristics

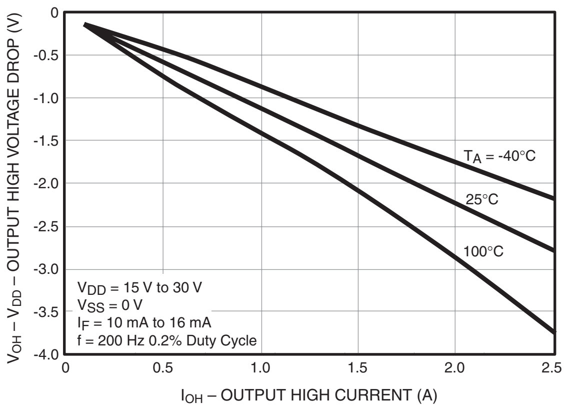


Figure 4. Output High Voltage Drop vs. Output High Current

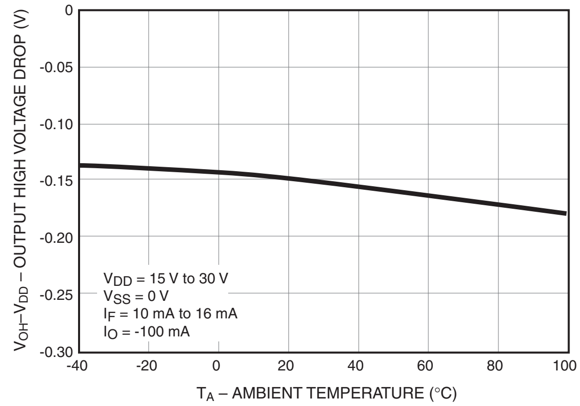


Figure 5. Output High Voltage Drop vs. Ambient Temperature

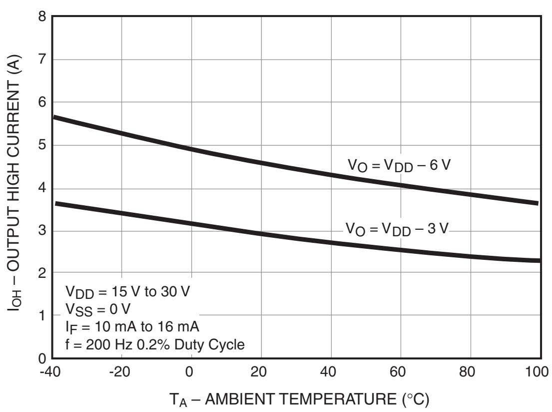


Figure 6. Output High Current vs. Ambient Temperature

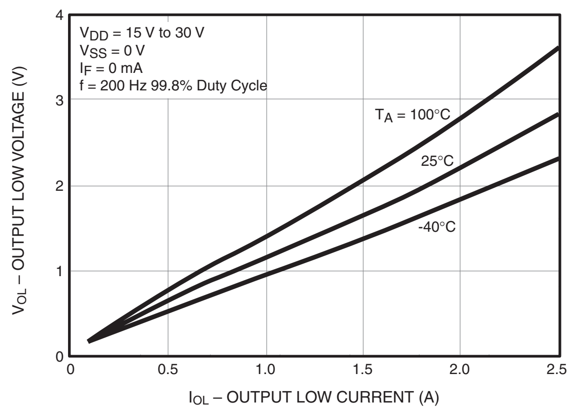


Figure 7. Output Low Voltage vs. Output Low Current

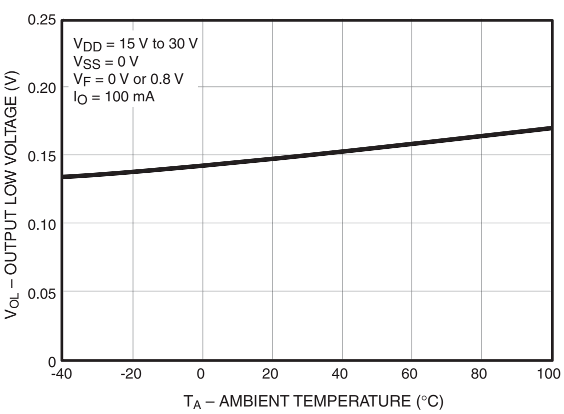


Figure 8. Output Low Voltage vs. Ambient Temperature

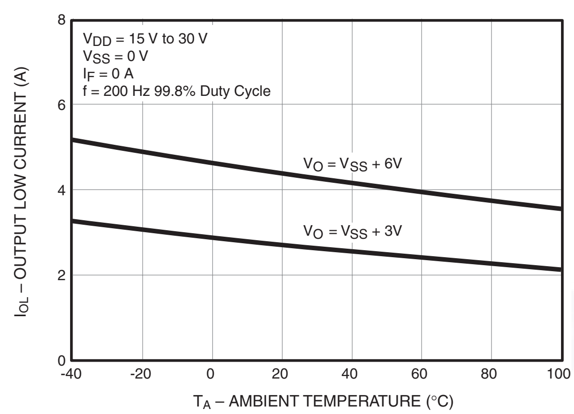


Figure 9. Output Low Current vs. Ambient Temperature

Typical Performance Characteristics (Continued)

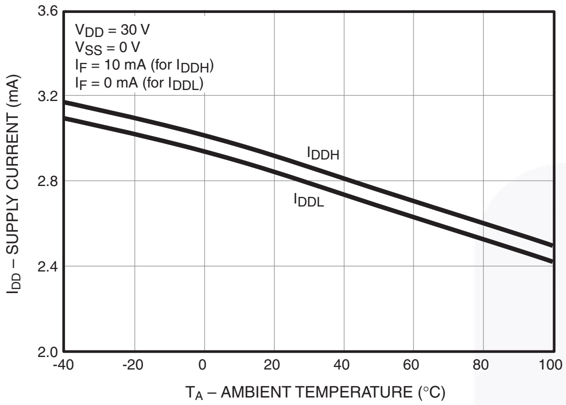


Figure 10. Supply Current vs. Ambient Temperature

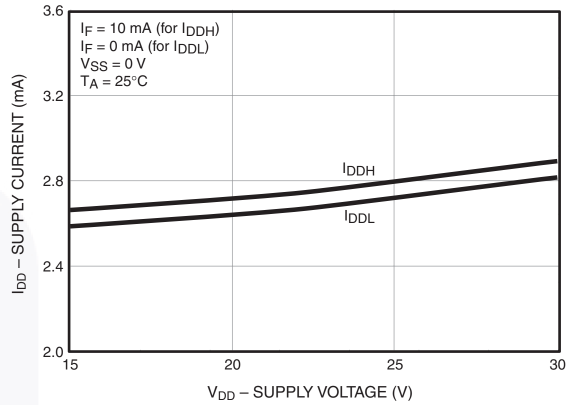


Figure 11. Supply Current vs. Supply Voltage

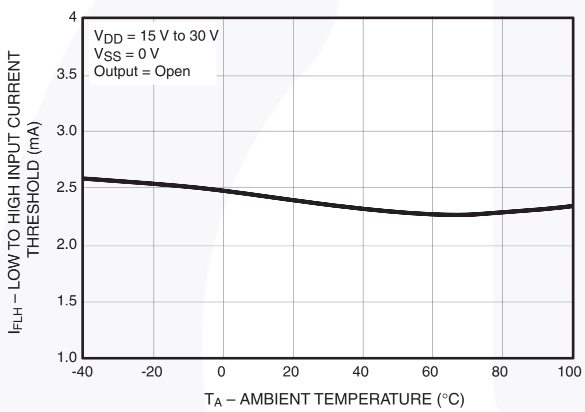


Figure 12. Low to High Input Current Threshold vs. Ambient Temperature

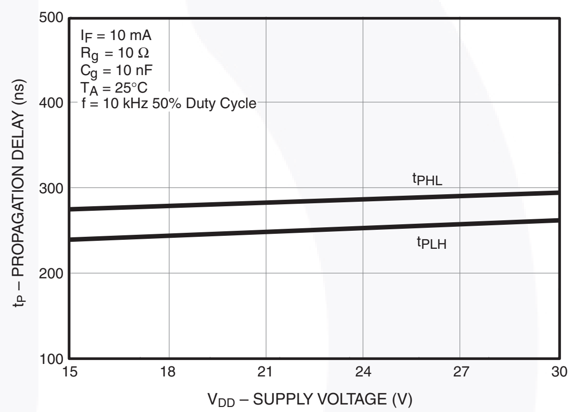


Figure 13. Propagation Delay vs. Supply Voltage

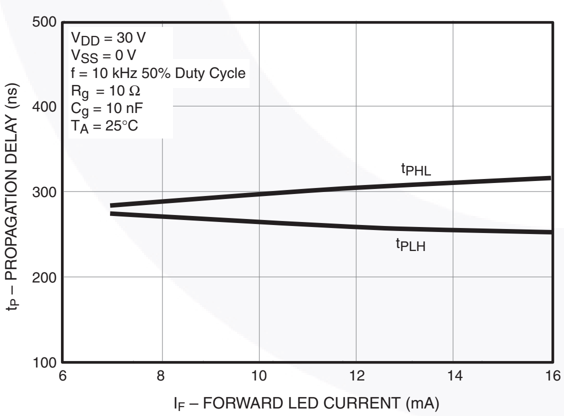


Figure 14. Propagation Delay vs. LED Forward Current

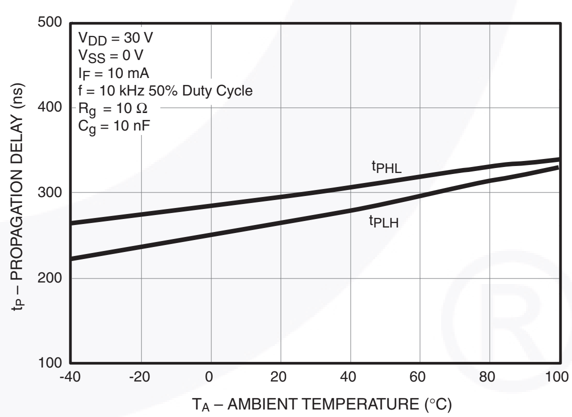


Figure 15. Propagation Delay vs. Ambient Temperature

Typical Performance Characteristics (Continued)

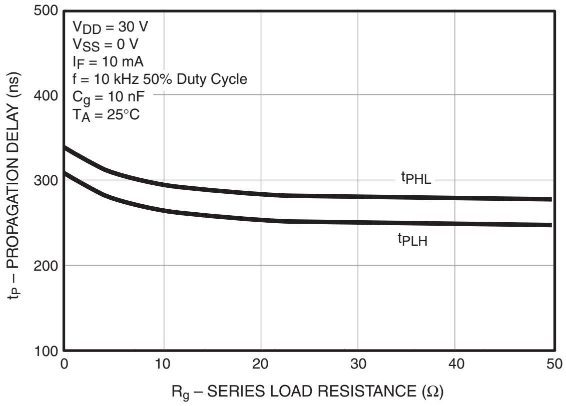


Figure 16. Propagation Delay vs. Series Load Resistance

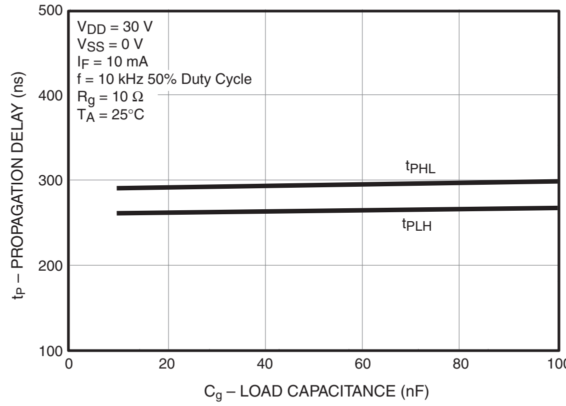


Figure 17. Propagation Delay vs. Load Capacitance

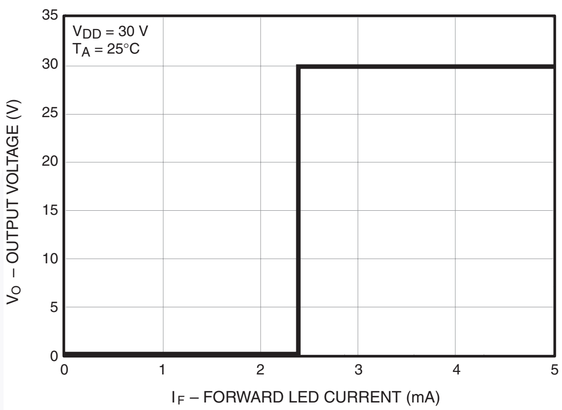


Figure 18. Transfer Characteristics

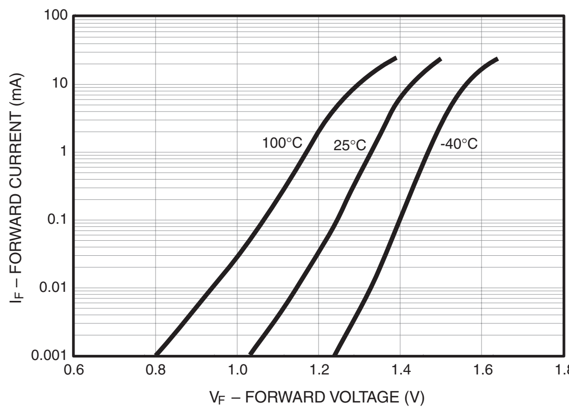


Figure 19. Input Forward Current vs. Forward Voltage

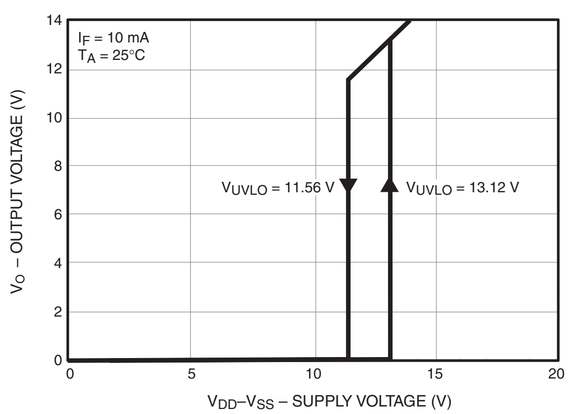


Figure 20. Under Voltage Lockout

Test Circuit

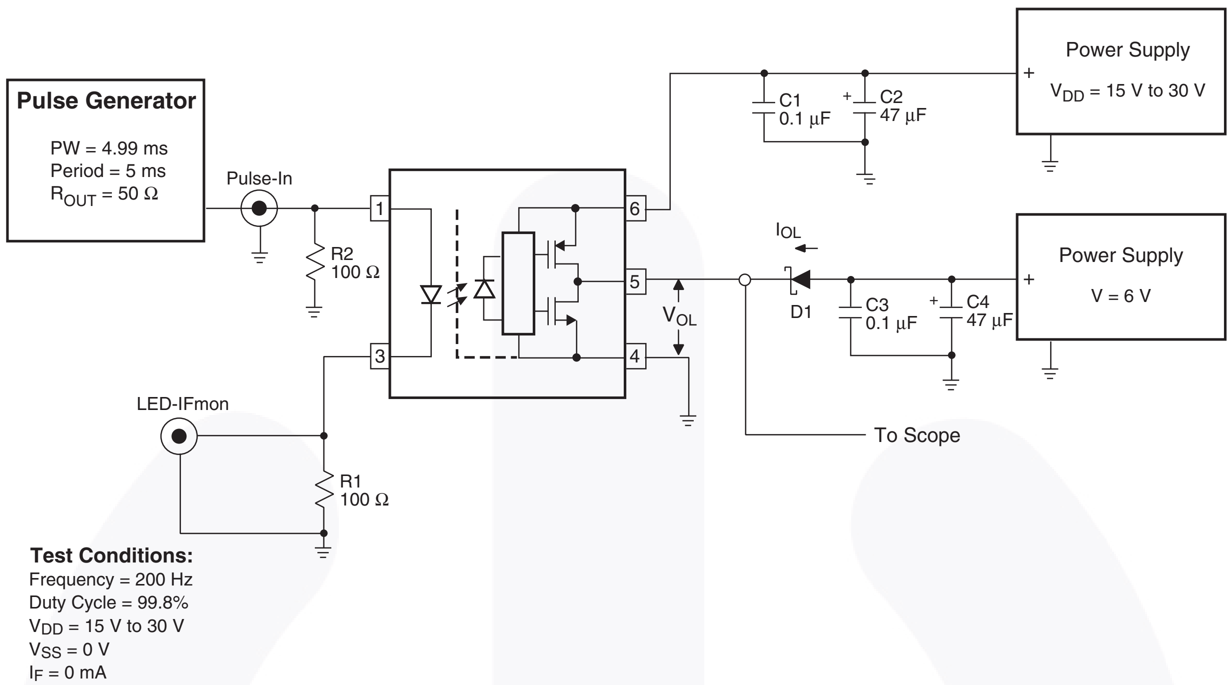


Figure 21. I_{OL} Test Circuit

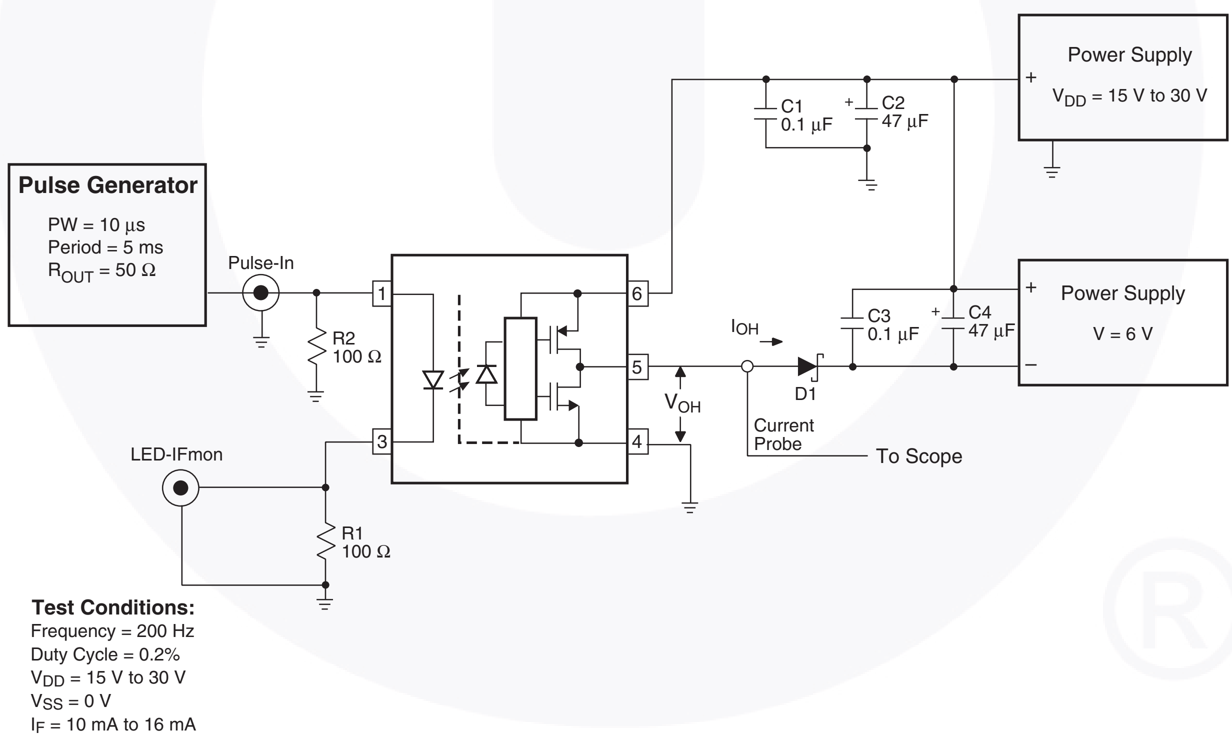


Figure 22. I_{OH} Test Circuit

Test Circuit (Continued)

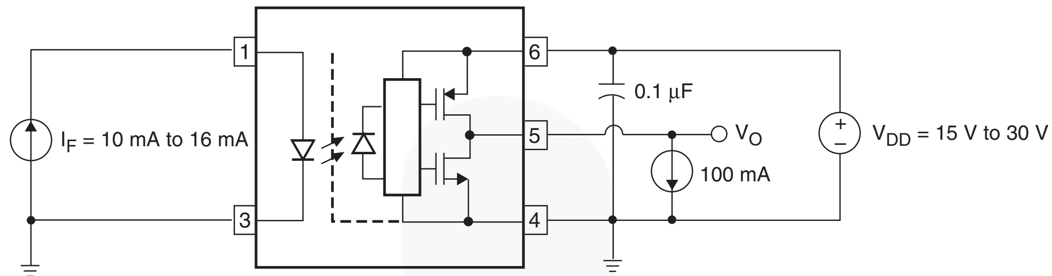


Figure 23. V_{OH} Test Circuit

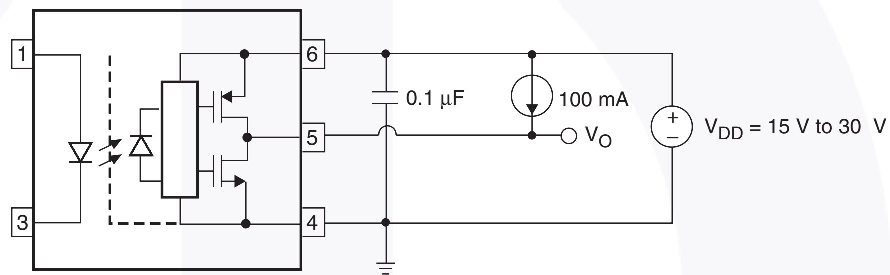


Figure 24. V_{OL} Test Circuit

Test Circuit (Continued)

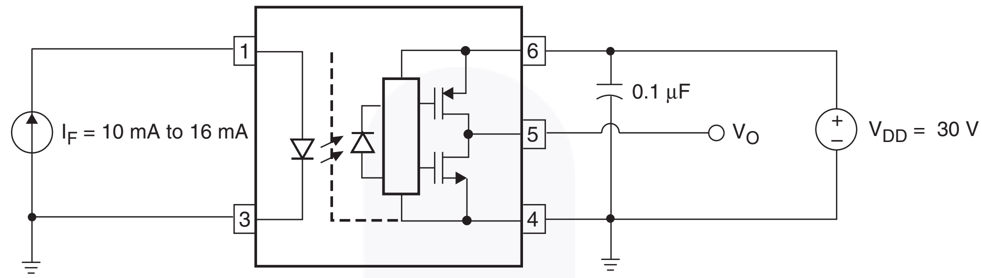


Figure 25. I_{DDH} Test Circuit

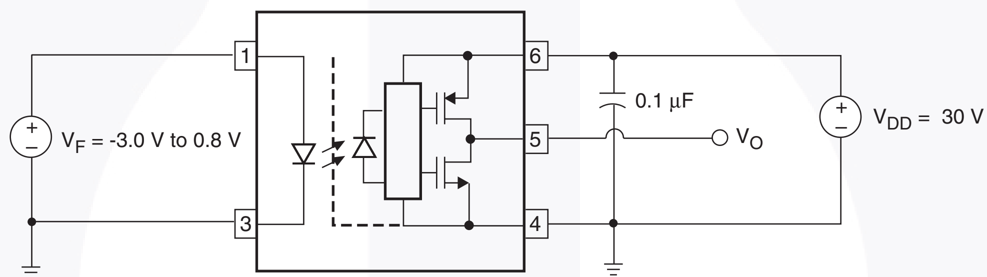


Figure 26. I_{DDL} Test Circuit

Test Circuit (Continued)

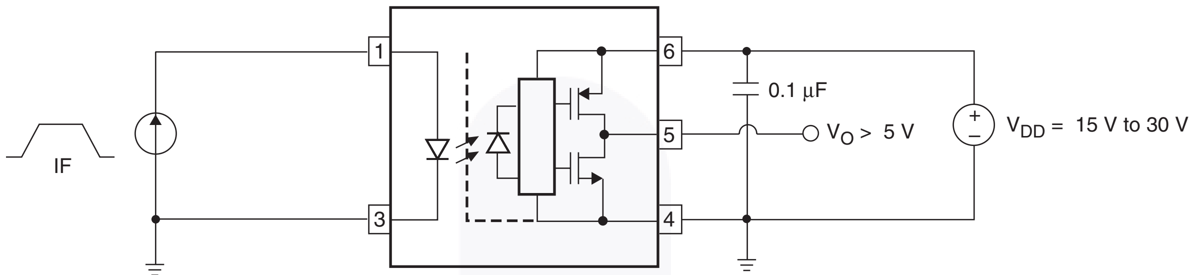


Figure 27. I_{FLH} Test Circuit

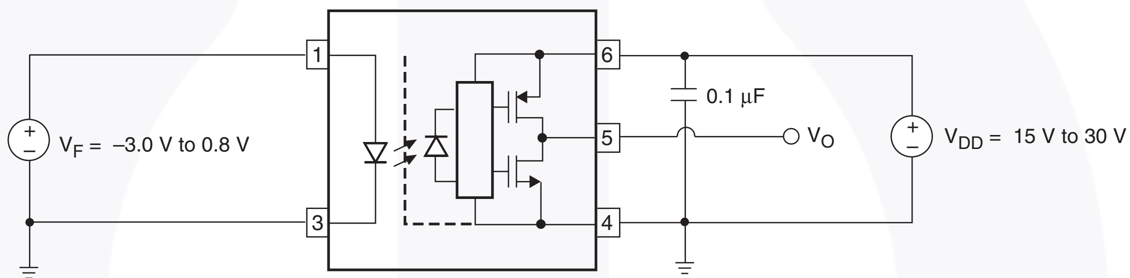


Figure 28. V_{FHL} Test Circuit

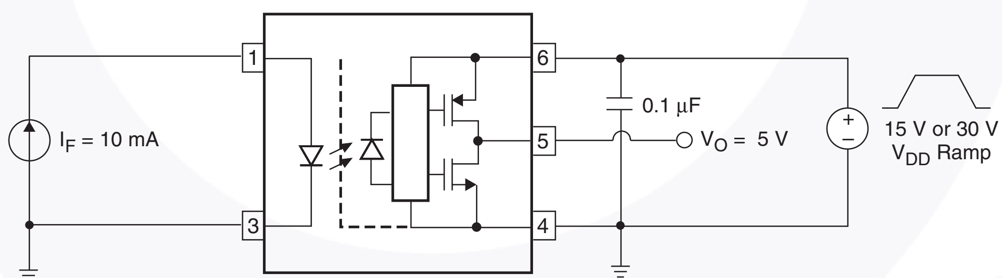


Figure 29. UVLO Test Circuit

Test Circuit (Continued)

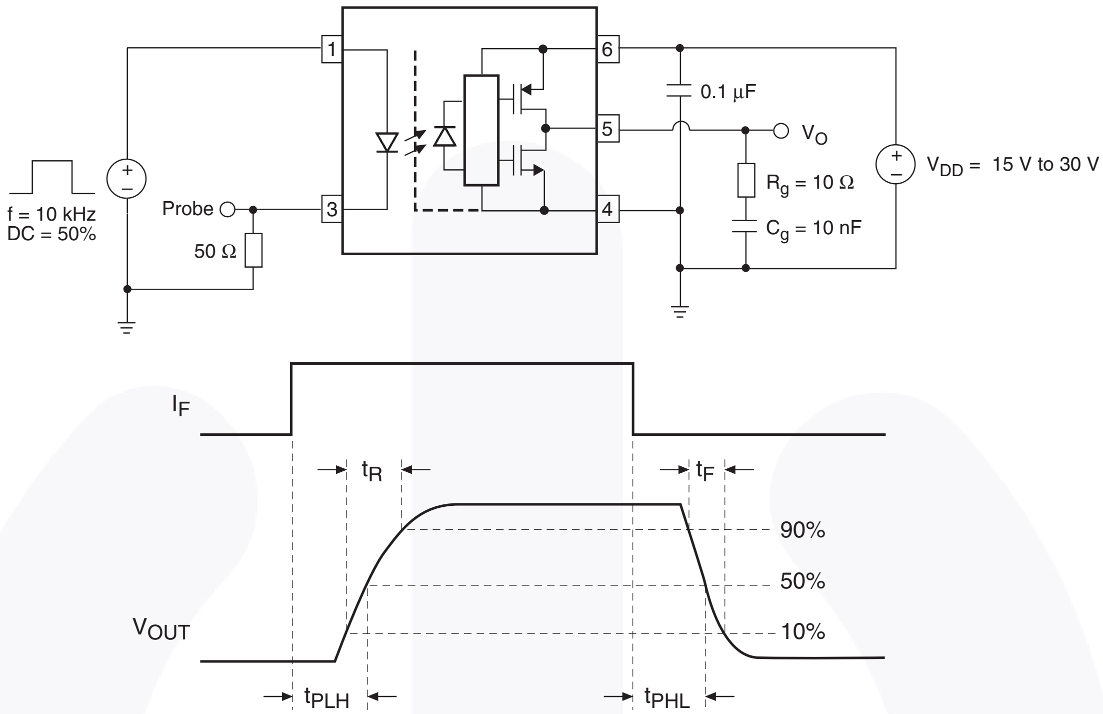


Figure 30. t_{PHL}, t_{PLH}, t_R and t_F Test Circuit and Waveforms

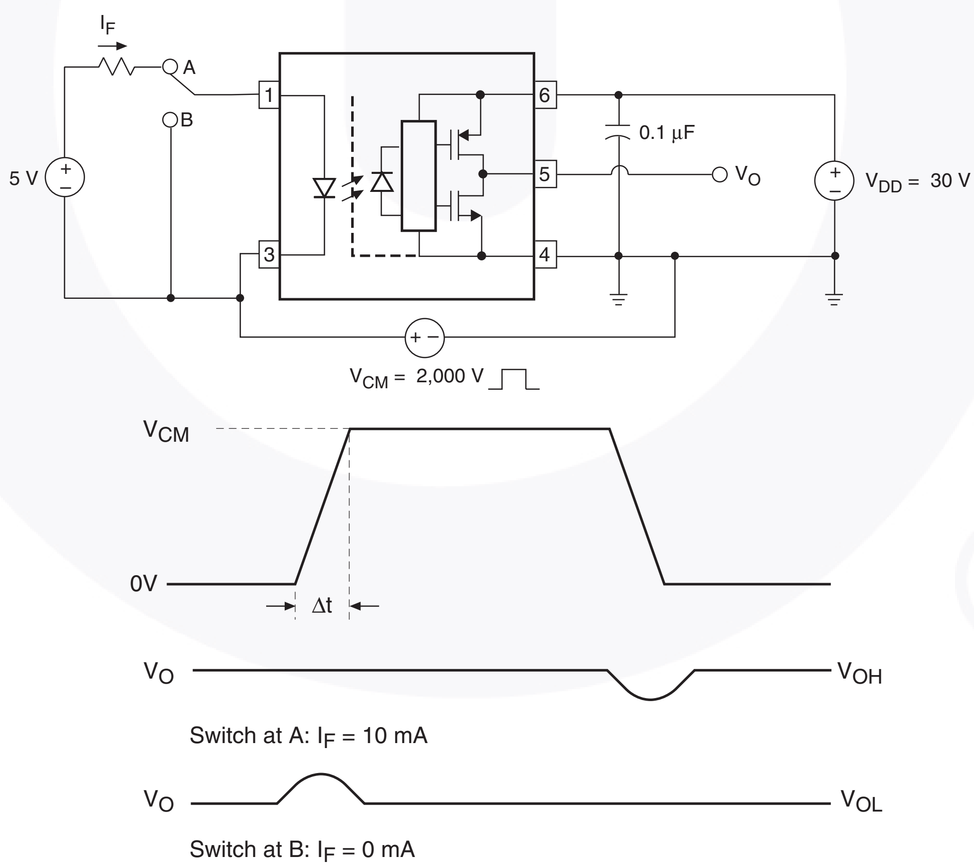
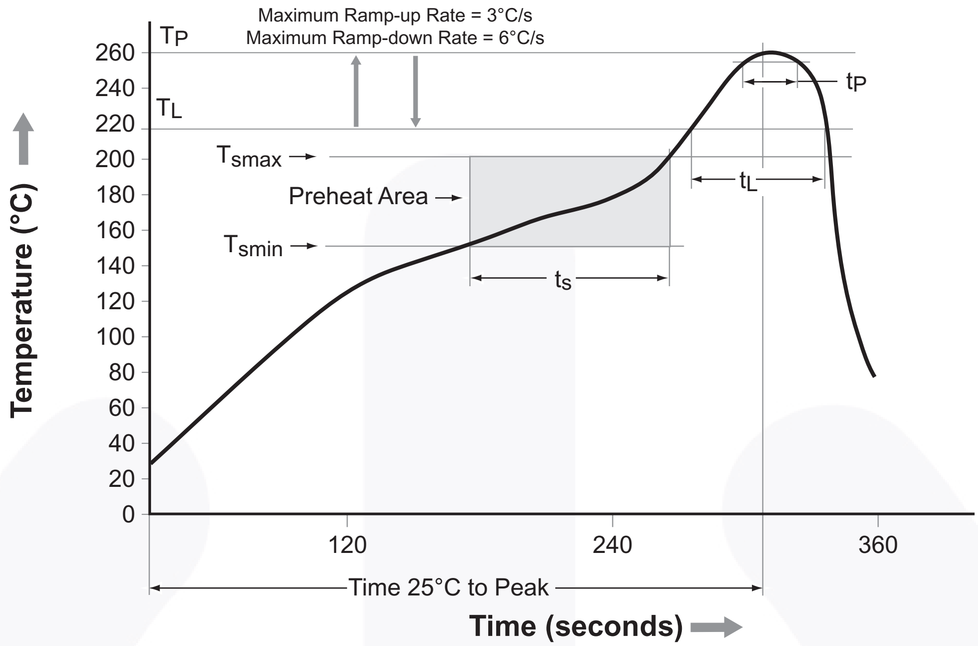


Figure 31. CMR Test Circuit and Waveforms

Reflow Profile



Profile Freature	Pb-Free Assembly Profile
Temperature Minimum (T_{smin})	150°C
Temperature Maximum (T_{smax})	200°C
Time (t_S) from (T_{smin} to T_{smax})	60 s to 120 s
Ramp-up Rate (t_L to t_P)	3°C/second maximum
Liquidous Temperature (T_L)	217°C
Time (t_L) Maintained Above (T_L)	60 s to 150 s
Peak Body Package Temperature	260°C +0°C / –5°C
Time (t_P) within 5°C of 260°C	30 s
Ramp-Down Rate (T_P to T_L)	6°C/s maximum
Time 25°C to Peak Temperature	8 minutes maximum

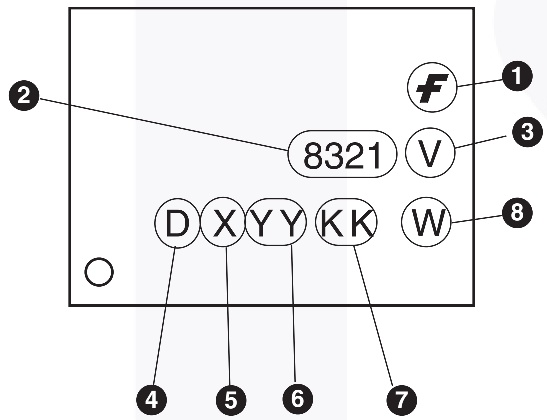
Figure 32. Reflow Profile

Ordering Information

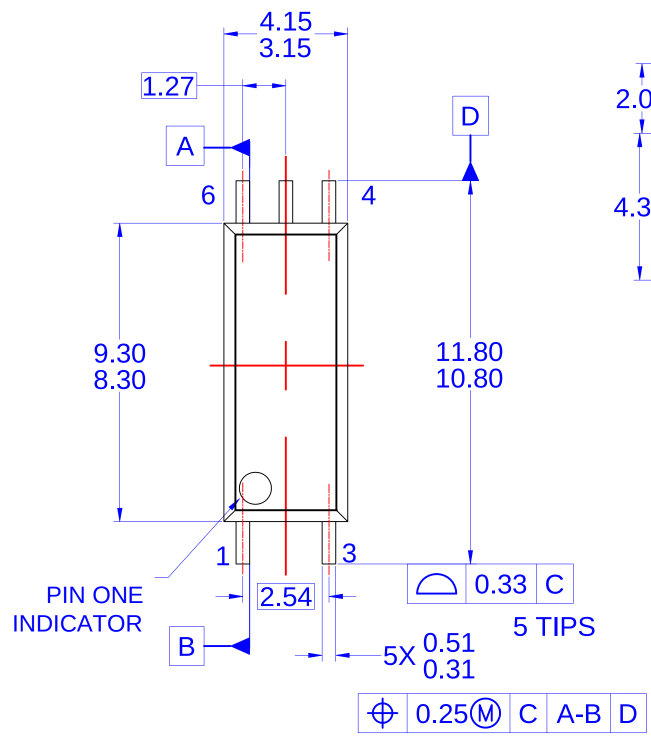
Part Number	Package	Packing Method
FOD8321	Wide Body SOP 5-Pin	Tube (100 units per tube)
FOD8321R2	Wide Body SOP 5-Pin	Tape and Reel (1,000 units per reel)
FOD8321V	Wide Body SOP 5-Pin, DIN EN/IEC60747-5-5 Option	Tube (100 units per tube)
FOD8321R2V	Wide Body SOP 5-Pin, DIN EN/ IEC60747-5-5 Option	Tape and Reel (1,000 units per reel)

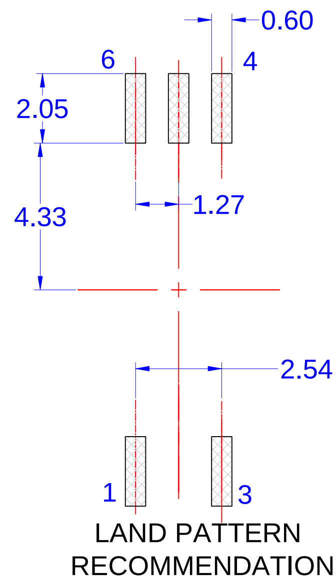
All packages are lead free per JEDEC: J-STD-020B standard.

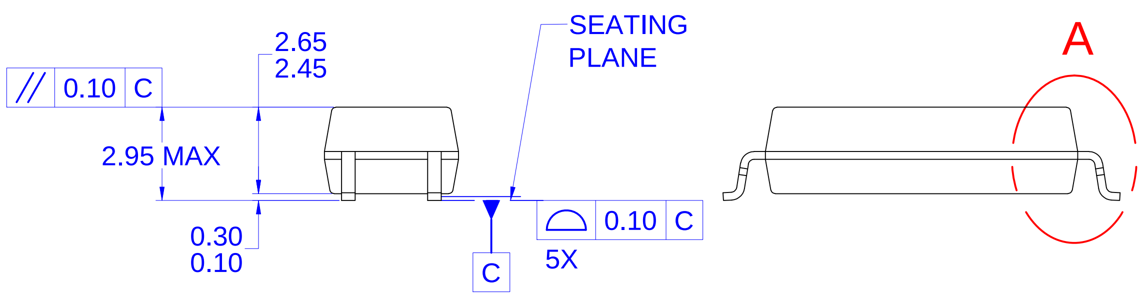
Marking Information

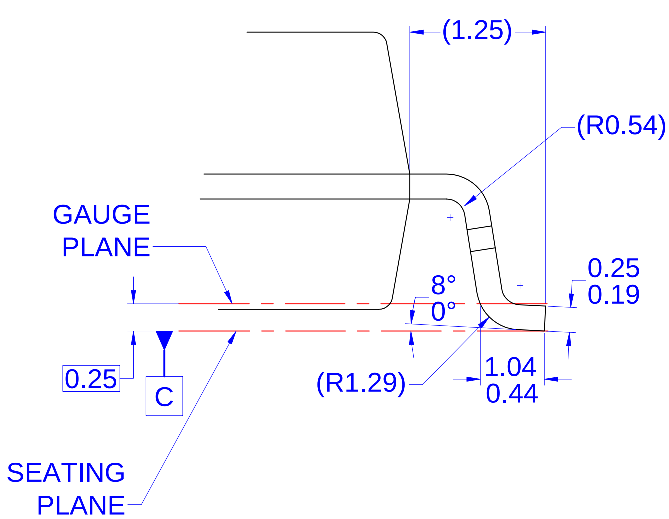


Definitions	
1	Fairchild logo
2	Device number, e.g., ‘8321’ for FOD8321
3	DIN EN/IEC60747-5-5 Option (only appears on component ordered with this option)
4	Plant code, e.g., ‘D’
5	Last digit year code, e.g., ‘C’ for 2012
6	Two digit work week ranging from ‘01’ to ‘53’
7	Lot traceability code
8	Package assembly code, W









DETAIL A
SCALE: 3.2:1

NOTES: UNLESS OTHERWISE SPECIFIED

A) THIS PACKAGE DOES NOT CONFORM TO ANY STANDARD.
B) ALL DIMENSIONS ARE IN MILLIMETERS.
C) DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH AND TIE BAR PROTRUSIONS
D) DRAWING CONFORMS TO ASME Y14.5M-1994
E) DRAWING FILE NAME: MKT-M05BREV2

PUBLICATION ORDERING INFORMATION

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