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FPF2290 Over-Voltage Protection Load Switch

Features

- Surge Protection
 - IEC 61000-4-5: ±100 V
- Selectable Over-Voltage Protection (OVP) with OV1 and OV2 Logic inputs
 - 5.9 V ±100 mV
 - 10 V ±100 mV
 - 14 V ±280 mV
 - 23 V ±460 mV
- Over-Temperature Protection (OTP)
- Ultra-Low On-Resistance: Typ. 33 mΩ
- ESD Protection

Human Body Model (HBM): > 2 kV
 Charged Device Model (CDM): > 1 kV
 IEC 61000-4-2 Air Discharge: > 15 kV

Applications

- Mobile Handsets and Tablets
- Portable Media Players
- MP3 Players

Description

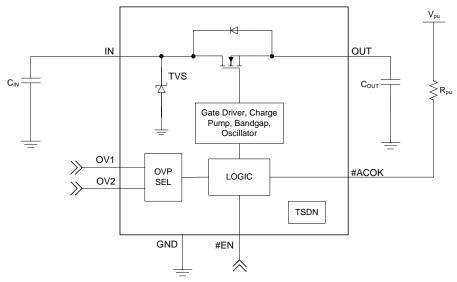
The FPF2290 features a low-RoN internal FET and an operating voltage range of $2.5\,\mathrm{V}$ to $23\,\mathrm{V}$. An internal clamping circuit is capable of shunting surge voltages of $\pm 100\,\mathrm{V}$, protecting downstream components and enhancing system robustness. The FPF2290 features over-voltage protection that powers down the internal FET if the input voltage exceeds the OVP threshold. The OVP threshold is selectable via Logic select pins (OV1 and OV2). Over-temperature protection also powers down the device at $130\,\mathrm{^{\circ}C}$ (typical).

The FPF2290 is available in a fully "green" compliant 1.3 mm × 1.8 mm Wafer-Level Chip-Scale Package (WLCSP) with backside laminate.

Ordering Information

Part Number	Operating Temperature Range	Top Mark	Package	Packing Method
FPF2290BUCX-F130	-40°C – +85°C	HR	12-Ball, 0.4 mm Pitch WLCSP	Tape & Reel

Block Diagram



Functional Block Diagram Figure 1.

Note:

1. Setting OV1 and OV2 logic level are recommended before IN is applied.

Pin Configuration

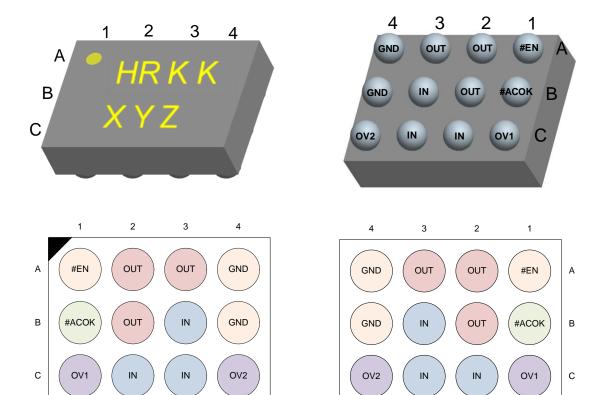


Figure 2. Pin Configuration (Top View)

Figure 3. Pin Configuration (Bottom View)

Pin Definitions

Name	Bump	Туре	Description				
IN	B3, C2, C3	Input/Supply	Switch Input and Device Supply				
OUT	A2, A3, B2	Output	Sw itch Output to Load				
#ACOK	B1	Output	Pow er Good (Open-Drain Output)		Hi-Z: V _{IN} < V _{IN_MIN} OR V _{IN} > V _{OVLO}		
#/1001		Output			LOW: Voltage Stable		
#EN	A1	Input	Device Enable (Active LOW)				
OV 1/2	C1, C4	Input	OVLO Selection Input (see Table 1) Note: Appy OV1 and OV2 Logic levels before VIN is applied.				
GND	A4, B4	Supply	Device Ground				

Table 1. OVLO Selection

OV1	OV2	OVP Trip Level
LOW	LOW	5.9 V ±100 mV
HIGH	LOW	10 V ±100 mV
LOW	HIGH	14 V ±280 mV
HIGH	HIGH	23 V ±460 mV

Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Parameter			Max.	Unit	
V _{IN}	V_IN to GND & V_IN to V_OUT = GND or Float			29.0	V	
V _{OUT}	V_OUT to GND		-0.3	V _{IN} + 0.3	V	
V_{OVn}	OV1 and OV2 to GND		-0.3	6.0	V	
V _{EN_ACOK}	Maximum DC Voltage Allowed on #EN or #ACOK Pin			6	V	
I _{IN}	Switch I/O Current (Continuous)			4.5	Α	
t _{PD}	Total Power Dissipation at T _A = 25°C		1.48	W		
T _{STG}	Storage Temperature Range	-65	+150	°C		
TJ	Maximum Junction Temperature		+150	°C		
TL	Lead Temperature (Soldering, 10 Seconds)			+260	°C	
ΘЈА	Thermal Resistance, Junction-to-Ambient (2) (1-in. Pad of 2		84.1	°C/W		
	IEC 64000 4.2 System Loyal ESD	Air Discharge	15			
ESD	IEC 61000-4-2 System Level ESD	Contact Discharge	8		kV	
E3D	Human Body Model, ANSI/ESDA/JEDEC JS-001-2012	All Pins	2		KV	
	Charged Device Model, JESD22-C101 All Pins					
Surge	IEC 61000-4-5, Surge Protection V _{IN}				V	

Note:

2. Measured using 2S2P JEDEC std. PCB.

Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. ON Semiconductor does not recommend exceeding them or designing to Absolute Maximum Ratings.

Symbol	Parameter		Max.	Unit
V _{IN}	Supply Voltage	2.5	23.0	V
T _A	Operating Temperature	-40	+85	°C

Electrical Characteristics

 T_A = -40°C to 85°C, V_{IN} = 2.5 to 23 V, unless otherwise indicated. Typical values are V_{IN} = 5.0 V, I_{IN} ≤ 3 A, C_{IN} = 0.1 μF and T_A = 25°C.

Symbol	Parameter	Conditions		Min.	Тур.	Max.	Unit
Basic Operat	tion					<u>.</u>	1
V _{IN_CLAMP}	Input Clamping Voltage	I _{IN} = 10 mA			35		V
lQ	Input Quiescent Current	V _{IN} = 5 V, #EN = 0 V			80	115	μΑ
l _{IN_Q}	OVLO Supply Current	OV1 = LOW V _{IN} = 6.5 V	OV1 = LOW, OV2 = LOW V _{IN} = 6.5 V, V _{OUT} = 0 V		63	90	μA
		V _{IN} Rising	OV1 = LOW,	5.80	5.90	6.00	
		V _{IN} Falling	OV2 = LOW	5.75			
		V _{IN} Rising	OV1 = HIGH,	9.90	10.00	10.10	1
.,	O con Maltana Tria I accel	V _{IN} Falling	OV2 = LOW	9.85			1 ,,
V _{IN_OVLO}	Over-Voltage Trip Level	V _{IN} Rising	OV1 = LOW,	13.72	14.0	14.28	V
		V _{IN} Falling	OV2 = HIGH	13.52			
		V _{IN} Rising	OV1 = HIGH,	22.54	23.0	23.46	
		V _{IN} Falling	OV2 = HIGH	22.34			
Ron	Resistance from V _{IN} to V _{OUT}	V _{IN} = 5 V, l _{OUT} = 1 A, T _A = 25°C			33	40	mΩ
C _{OUT}	OUT Load Capacitance ⁽³⁾	V _{IN} = 5 V		0.1		1000.0	μF
T _{SDN}	Thermal Shutdow n ⁽³⁾				130		°C
T _{SDN_HYS}	Thermal Shutdown Hysteresis (3)				20		°C
Digital Signa	ls					ı	
V _{OL}	#ACOK Output Low Voltage	I _{SINK} = 1 mA				0.4	V
Іасок	#ACOK Leakage Current	V _{I/O} = 3.0 V, #ACOK Deasserted				0.5	μΑ
V _{IH}	Input HIGH Voltage (#EN, OVx)	V _{IN} = 2.5 V to V _{OVLO}		1.2			V
V _{IL}	Input LOW Voltage (#EN, OVx)	V _{IN} = 2.5 V to V _{OVLO}				0.5	V
I _{IN}	Input Leakage Current (#EN, OVx)	V _{IN} = 5.0 V, V _{OUT} = Float				1.0	μA
Timing Chara	acteristics	•		L		ı	J.
t _{DEB}	Debounce Time	Time from 2.5 V < V_{IN} < V_{IN_OVLO} to V_{OUT} = 0.1 × V_{IN}		10	15	20	ms
tstart	Soft-Start Time	Time from $V_{IN} = V_{IN_min}$ to 0.2 × #ACOK, $V_{IO} = 1.8$ V w ith 10 k Ω Pull-up Resistor		20	30	40	ms
ton	Sw itch Turn-On Time	R_L = 100 Ω , C_L = 22 μ F, V_{OUT} from 0.1 \times V_{IN} to 0.9 \times V_{IN}		1	3	5	ms
toff	Sw itch Turn-Off Time ⁽³⁾	$\begin{aligned} R_L &= 100~\Omega,~C_L = 0~\mu\text{F},~V_{IN} > V_{OVLO} \\ to~V_{OUT} &= 0.8 \times V_{IN} \end{aligned}$				150	ns

Note:

3. Guaranteed by characterization and design.

Timing Diagrams

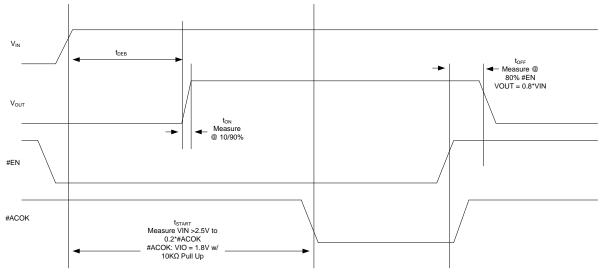


Figure 4. Timing for Power Up and Normal Operation

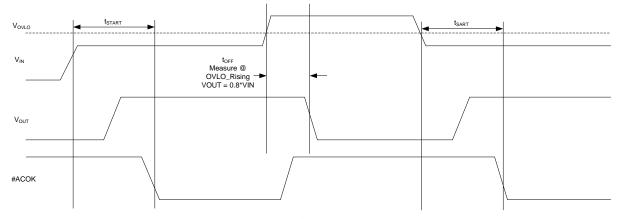
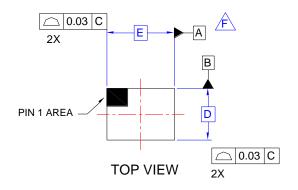


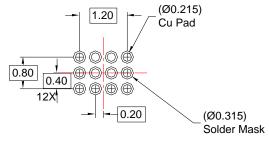
Figure 5. Timing for OVLO Trip

Product-Specific Dimensions

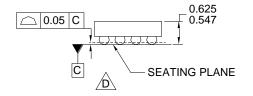
D	Е	Х	Υ
1288 μm ±30 μm	1828 μm ±30 μm	314 μm ±18 μm	244 μm ±18 μm

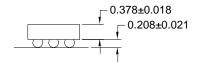
Physical Dimensions





RECOMMENDED LAND PATTERN (NSMD PAD TYPE)





SIDE VIEWS

⊕ 0.005(M) C A B

Ø0.260±0.02

_(Y)±0.018

12X

NOTES:

- A. NO JEDEC REGISTRATION APPLIES.
- B. DIMENSIONS ARE IN MILLIMETERS.
- C. DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 2009.
- D. DATUM C IS DEFINED BY THE SPHERICAL CROWNS OF THE BALLS.
- E. PACKAGE NOMINAL HEIGHT IS 586 MICRONS ±39 MICRONS (547-625 MICRONS).
- F. FOR DIMENSIONS D, E, X, AND Y SEE PRODUCT DATASHEET.
- G. DRAWING FILENAME: MKT-UC012ZCrev2.
- H. ON SEMICONDUCTOR RECOMMENDS THAT LANDS IN THE LANDPATTERN ARE AT LEAST .215MM DIAMETER AS MEASURED AT THE BOTTOM OF THE LAND, NOT THE TOP EDGE.



- 1.20

 $\bigcirc \bigcirc \bigcirc \bigcirc \bigcirc B$

 $\oplus \bigcirc \oplus \oplus$

2 3

0.20

0.80

0.40

Figure 6. 12-Ball, 3x4 Array, 0.4 mm Pitch, Wafer-Level Chip-Scale Package (WLCSP)

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