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November 2014

FPF3040
IntelliMAX™ 18 V-Rated Dual Input Single Output Power-Source-Selector Switch

Features

- Dual-Input, Single-Output Load Switch
- Input Supply Operating Range:
  - 4~10.5 V at V_{IN}
  - 4~6.5 V at V_{BUS}
- Typical R_{ON}:
  - 95 mΩ at V_{IN}=5 V
  - 70 mΩ at V_{BUS}=5 V
- Bi-Directional Switch for V_{IN} and V_{BUS}
- Slew Rate Controlled:
  - 50 µs at V_{IN} for < 4.7 µF C_{OUT}
  - 90 µs at V_{BUS} for < 4.7 µF C_{OUT}
- Maximum I_{SW}: 2 A Per Channel
- Break-Before-Make Transition
- Under-Voltage Lockout (UVLO)
- Over-Voltage Lockout (OVLO)
- Thermal Shutdown
- Logic CMOS IO Meets JESD76 Standard for GPIO Interface and Related Power Supply Requirements
- ESD Protected:
  - Human Body Model: >3 kV
  - Charged Device Model: >1.5 kV
  - IEC 61000-4-2 Air Discharge: >15 kV
  - IEC61000-4-2 Contact Discharge: >8 kV

Description

The FPF3040 is a 18 V-rated Dual-Input Single-Output (DISO) load switch consisting of two channels of slew-rate-controlled, low-on-resistance, N-channel MOSFET switches with protection features. The slew-rate-controlled turn-on characteristic prevents inrush current and the resulting excessive voltage droop on the input power rails. The input voltage range operates from 4 V to 6.5 V at V_{BUS} and from 4 V to 10.5 V at V_{IN} to align with the needs of low-voltage portable device power rails.

V_{IN} and V_{BUS} have the over-voltage protection functionality of typical 12 V and 7.5 V, respectively, to avoid unwanted damage to system.

V_{IN} and V_{BUS} bi-directional switching allows reverse current from V_{OUT} to V_{IN} or V_{BUS} for On-The-Go, (OTG) Mode. The switching is controlled by logic input EN and V_{IN_SEL} is capable of interfacing directly with low-voltage control signal General-Purpose Input / Output (GPIO).

FPF3040 is available in 1.8 mm x 2.0 mm Wafer-Level Chip-Scale Package (WLCSP), 16-bump, 0.4 mm pitch.

Applications

- Input Power Selection Block Supporting USB and Wireless Charging
- Smartphone / Tablet PC

Ordering Information

Part Number	Top Mark	Channel	Typical R_{ON} per Channel at $5V_{IN}$	Rise Time (t_R)	Package
FPF3040UCX	QY	DISO	95 mΩ for V_{IN}	50 µs for V_{IN}	1.8 mm x 2.0 mm Wafer-Level Chip-Scale Package (WLCSP), 16-Bump, 0.4 mm Pitch
			70 mΩ for V_{BUS}	90 µs for V_{BUS}	

Application Diagram

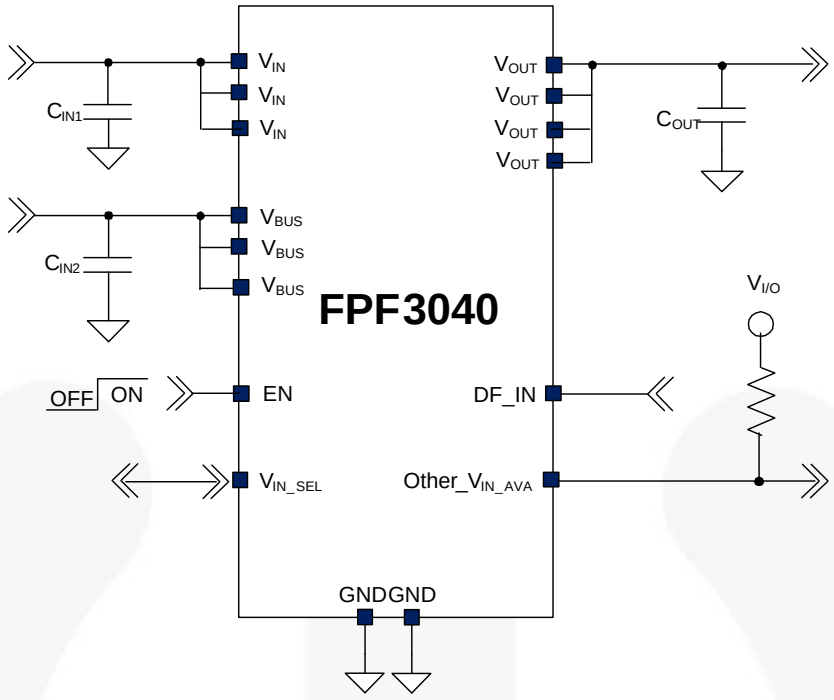


Figure 1. Typical Application

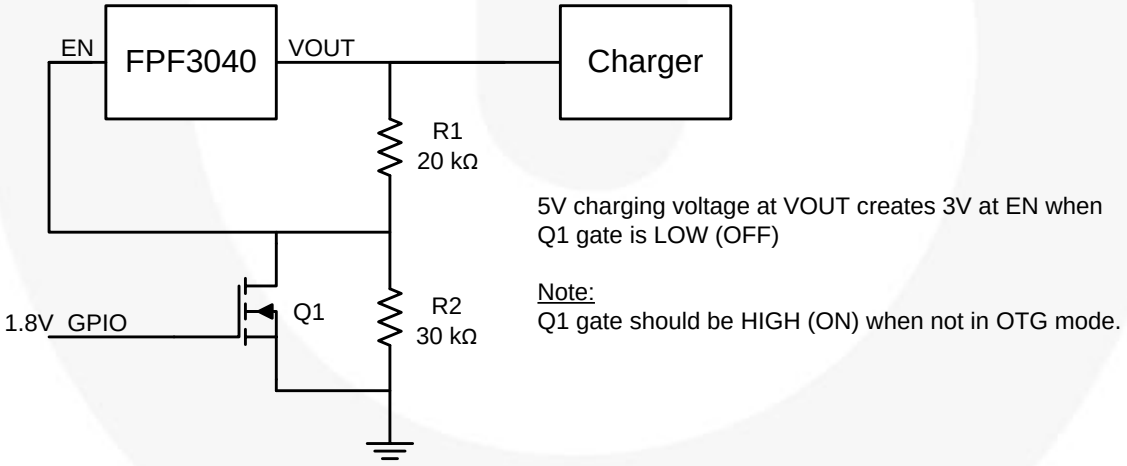


Figure 2. Example Circuit for OTG Operation with Low-Voltage GPIO

Block Diagram

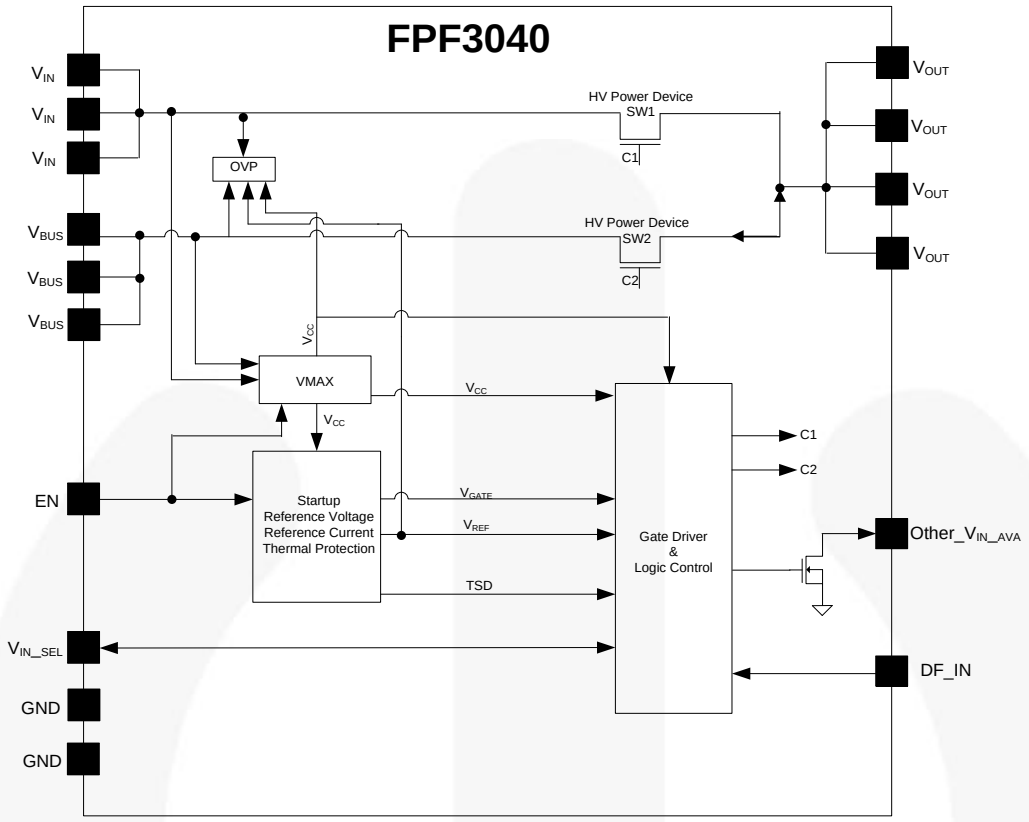


Figure 3. Functional Block Diagram

Pin Configuration

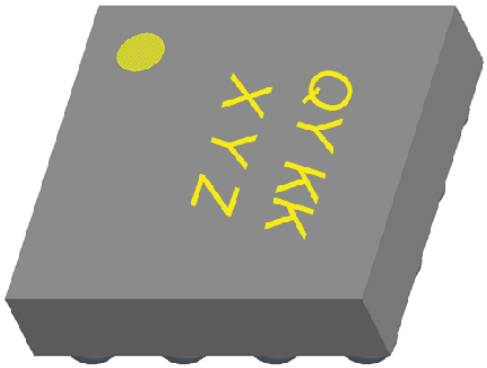


Figure 4. Pin Assignment (Top View)

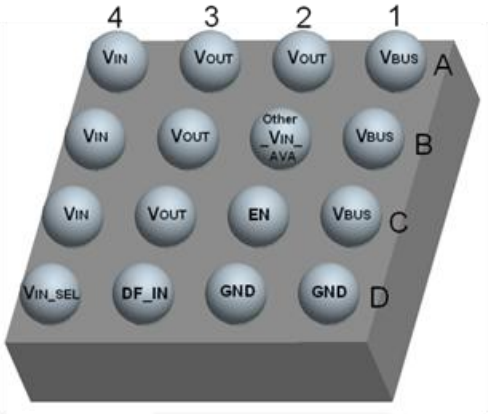


Figure 5. Pin Assignment (Bottom View)

Pin Description

Pin #	Name	Input / Output	Description
A1, B1, C1	V_{BUS}	Input / Output	**V_{BUS} at USB**: Power input / output. bi-directional switch when V_{IN_SEL} = LOW.
A4, B4, C4	V_{IN}	Input / Output	**V_{IN} Supply Input**: Power input / output. bi-directional switch when V_{IN_SEL} = HIGH.
A2, A3, B3, C3	V_{OUT}	Input / Output	**Switch Output**: Power input / output.
C2	EN	Input	**Enable**: Active HIGH. EN voltage ≥ 2.5 V can power internal circuit when V_{IN} and V_{BUS} are absent. 1 MΩ pull-down resistor is included.
D4	V_{IN_SEL}	Input / Output	**Supply Selector & Status**: Input power source selection input and status output. This signal is ignored during EN=LOW. Selector input during EN=HIGH: HIGH = switch V_{IN} to V_{OUT} / LOW = switch V_{BUS} to V_{OUT}. Status output during EN=LOW: HIGH = V_{IN} is used for V_{OUT} / LOW = V_{BUS} is used for V_{OUT}.
D3	DF_IN	Input	**Default Supply Selector during EN=LOW**: Input. Floating = VBUS connects to V_{OUT}. LOW means V_{IN} connects to V_{OUT}. This signal is ignored during EN=HIGH. 1 µA pull-up current source is included.
B2	Other_V_{IN_AVA}	Output	**Other Supply Input Status**: Open-drain output. HI-Z = both V_{IN} and V_{BUS} are valid. LOW = the other power source is not valid.
D1, D2	GND		**Ground**

Table 1. Truth Table

EN	V_{IN}>UVLO	V_{BUS}>UVLO	V_{IN_SEL}	DF_IN	Other_V_{IN_AVA}	V_{OUT}	Comment
HIGH	X	X	LOW	X	HI-Z if V_{IN} & V_{BUS} >UVLO LOW if V_{IN} or V_{BUS} <UVLO	V_{BUS}	V_{OUT} is selected by V_{IN_SEL} Bi-directional channel
HIGH	X	X	HIGH	X	HI-Z if V_{IN} & V_{BUS} >UVLO LOW if V_{IN} or V_{BUS} <UVLO	V_{IN}	
LOW	YES	NO	HIGH	X	LOW	V_{IN}	Automatic selection to valid input V_{IN_SEL} is output.
LOW	NO	YES	LOW	X	LOW	V_{BUS}	
LOW	YES	YES	LOW	Floating	HIGH	V_{BUS}	V_{OUT} is selected by DF_IN V_{IN_SEL} is output.
LOW	YES	YES	HIGH	LOW	HIGH	V_{IN}	
LOW	NO	NO	X	X	LOW	Floating	OFF

Notes:
1. Internal pull-down at EN.
2. 1 µA pull-up current source at DF_IN.

Absolute Maximum Ratings

Stresses exceeding the Absolute Maximum Ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Parameters			Min.	Max.	Unit
V_{PIN}	$V_{IN,}$ V_{BUS} to GND	Continuous		-1.4	18	V
		Pulsed, 100 ms Maximum Non-Repetitive		-2.0		
	V_{OUT} to GND[3]			-0.3	16.0	
	EN, DF_IN, V_{IN_SEL}, Other_V_{IN_AVA} to GND			-0.3	6.0	
I_{SW}	Maximum Continuous Switch Current per Channel				2	A
t_{PD}	Total Power Dissipation at T_A=25°C				2.25	W
T_J	Operating Junction Temperature			-40	+150	°C
T_{STG}	Storage Junction Temperature			-65	+150	°C
Θ_{JA}	Thermal Resistance, Junction-to-Ambient (1in. Square Pad of 2 oz. Copper)				55[4]	°C/W
ESD	Electrostatic Discharge Capability	Human Body Model, JESD22-A114		3		kV
		Charged Device Model, JESD22-C101		1.5		
		IEC61000-4-2 System Level[5]	Air Discharge ($V_{IN,}$ V_{BUS} to GND)	15		
			Contact Discharge ($V_{IN,}$ V_{BUS} to GND)	8		

Notes:
3. If external voltage of more than 10.5 V is applied to V_{OUT}, the slew rate should be less than 1 V/ms from 10.5 V.
4. Measured using 2S2P JEDEC standard PCB.
5. System level ESD can be guaranteed by design.

Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to Absolute Maximum Ratings.

Symbol	Parameters	Min.	Max.	Unit
V_{PIN}	V_{IN}	4.0	10.5	V
	V_{BUS}	4.0	6.5	
T_A	Ambient Operating Temperature	-40	+85	°C

Electrical Characteristics

V_{IN}=4 to 10.5 V, V_{BUS}=4 to 6.5 V, T_A=-40 to 85°C unless otherwise noted. Typical values are at V_{IN}=V_{BUS}=5 V, EN=HIGH and T_A=25°C unless otherwise noted.

Symbol	Parameters	Condition	Min.	Typ.	Max.	Unit
Basic Operation						
V_{IN}	Input Voltage		4.0		10.5	V
V_{BUS}			4.0		6.5	V
I_Q	Quiescent Current	I_{OUT}=0 mA, EN=HIGH, V_{IN} or V_{BUS}=5 V		55	120	µA
		I_{OUT}=0 mA, EN=5 V, V_{IN} and V_{BUS}=GND		33	70	µA
R_{ON}	On Resistance for V_{IN}	V_{IN}=8 V, I_{OUT}=200 mA, T_A=25°C		95		mΩ
		V_{IN}=5 V, I_{OUT}=200 mA, T_A=25°C		95	150	
		V_{IN}=5 V, I_{OUT}=200 mA, T_A=25°C to 85°C[6]			200	
	On Resistance for V_{BUS}	V_{BUS}=6 V, I_{OUT}=200 mA, T_A=25°C		70		mΩ
		V_{BUS}=5 V, I_{OUT}=200 mA, T_A=25°C		70	100	
		V_{BUS}=5 V, I_{OUT}=200 mA, T_A=25°C to 85°C[6]			140	
V_{IH}	Input Logic High Voltage	V_{IN}=4 V~10.5 V, V_{BUS}=4 V ~ 6.5 V	1.15			V
V_{IL}	Input Logic Low Voltage	V_{IN}=4 V~10.5 V, V_{BUS}=4 V ~ 6.5 V			0.52	V
$V_{EN(OTG)}$	EN Voltage in OTG Mode[6]	V_{IN} & V_{BUS}=Float or V_{IN} & V_{BUS} <V_{UVLO}	2.5			V
R_{EN_PD}	Pull-Down Resistance at EN		707	1000	1360	kΩ
Protection						
V_{UVLO}	Under-Voltage Lockout Threshold	V_{IN} or V_{BUS} Rising	3.05	3.50	4.00	V
		V_{IN} or V_{BUS} Falling	2.55	3.00	3.55	V
V_{UVHYS}	Under-Voltage Lockout Hysteresis			0.5		V
V_{OVLO}	Over-Voltage Lockout Threshold	V_{IN} Rising Threshold	10.85	12.00	13.45	V
		V_{IN} Falling Threshold		11.5		V
		V_{BUS} Rising Threshold	6.52	7.50	8.32	V
		V_{BUS} Falling Threshold		7		V
V_{OVHYS}	Over-Voltage Lockout Hysteresis	V_{IN}		0.5		V
		V_{BUS}		0.5		V
T_{SDN}	Thermal Shutdown Threshold			150		°C
T_{SDNHYS}	Thermal Shutdown Hysteresis			20		°C
Reverse Current Blocking						
I_{RCB}	V_{IN} or V_{BUS} Current During RCB	V_{OUT}=8 V, V_{IN} or V_{BUS}=GND			30	µA
Dynamic Characteristics						
t_R	V_{OUT} Rise Time, V_{BUS}[6,7]	V_{IN}=V_{BUS}=5 V, R_L=150 Ω, C_L=4.7 µF, T_A=25°C		90		µs
	V_{OUT} Rise Time, V_{IN}[6,7]			50		
t_F	V_{OUT} Fall Time[6,7]			1.4		ms
t_{TRAN}	Transition Delay[6,7]		50	100		ms
t_{SD}	Selection Delay[6,7]			50		µs

Notes:

6. This parameter is guaranteed by characterization and/or design; not production tested.
7. t_{SD}/t_{TRAN}/t_R/t_F are defined in Figure 6.

Timing Diagram

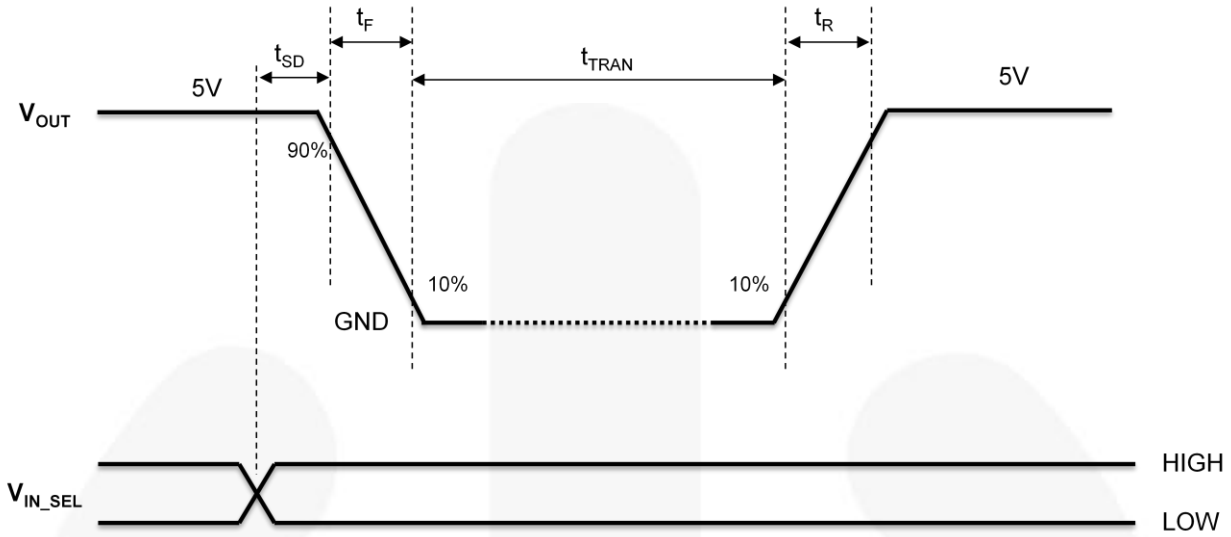


Figure 6. Transition Delay (V_{IN}=V_{BUS}=5 V)

Typical Characteristics

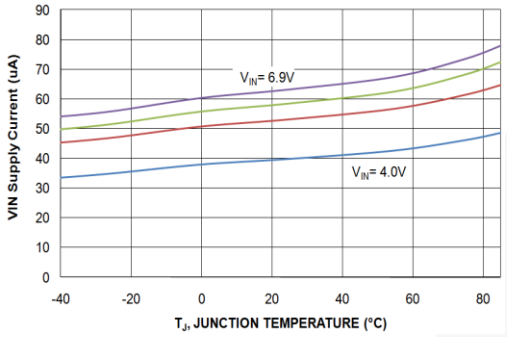


Figure 7. V_{IN} Quiescent Current (I_q) vs. Temperature

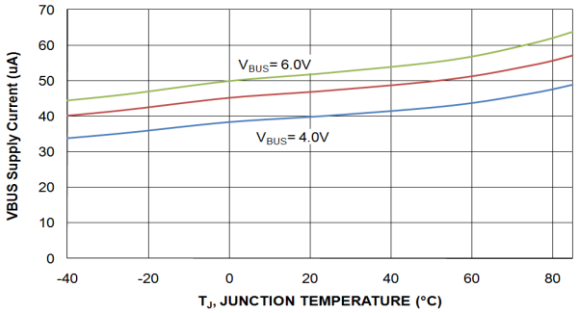


Figure 8. V_{BUS} Quiescent Current (I_q) vs. Temperature

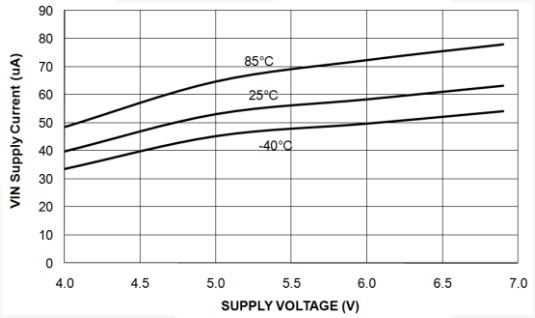


Figure 9. V_{IN} Quiescent Current vs. Supply Voltage

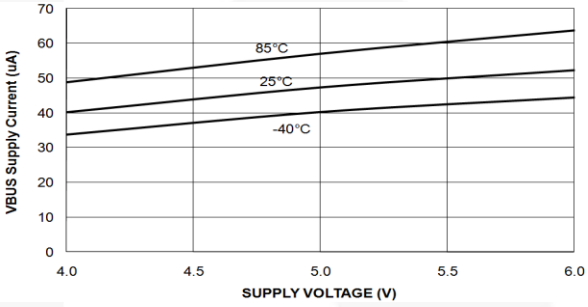


Figure 10. V_{BUS} Quiescent Current vs. Supply Voltage

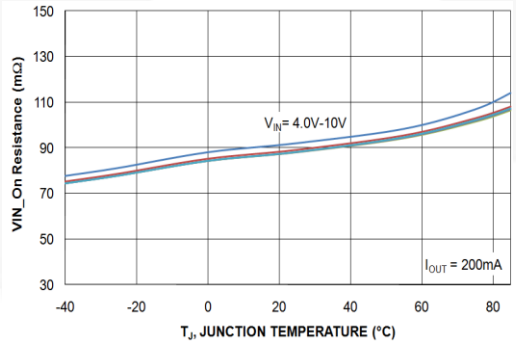


Figure 11. V_{IN} On Resistance (mΩ) vs. Temperature

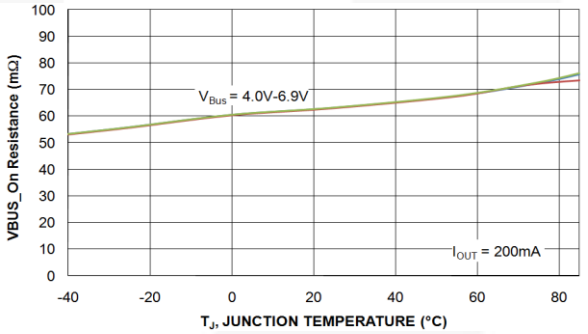


Figure 12. V_{BUS} On Resistance (mΩ) vs. Temperature

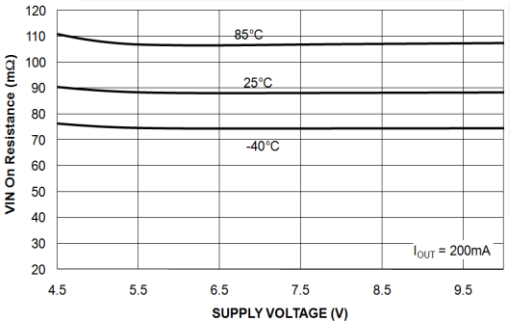


Figure 13. V_{IN} On Resistance (mΩ) vs. Supply Voltage

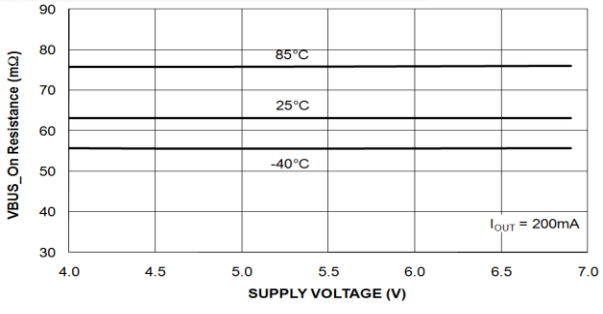


Figure 14. V_{BUS} On Resistance (mΩ) vs. Supply Voltage

Typical Characteristics (Continued)

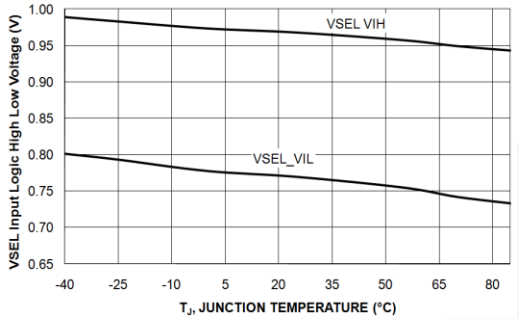


Figure 15. V_{IN}_SEL Input Logic High & Low Voltage vs. Temperature

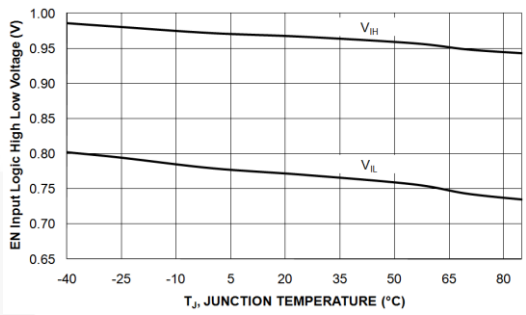


Figure 16. EN Input Logic High & Low Voltage vs. Temperature

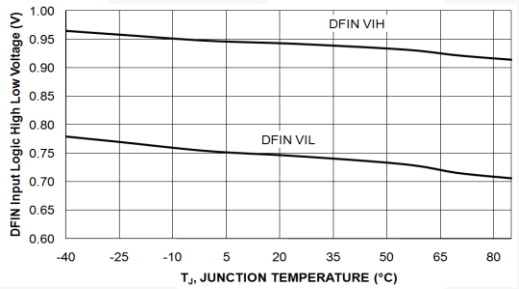


Figure 17. DF_IN Logic High & Low Voltage vs. Temperature

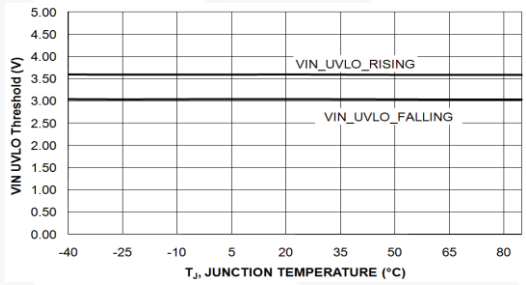


Figure 18. V_{IN_VULVO} vs. Temperature

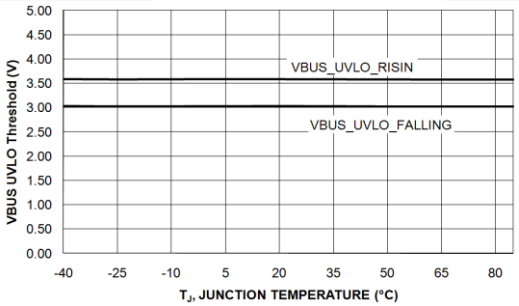


Figure 19. V_{BUS_VULVO} vs. Temperature

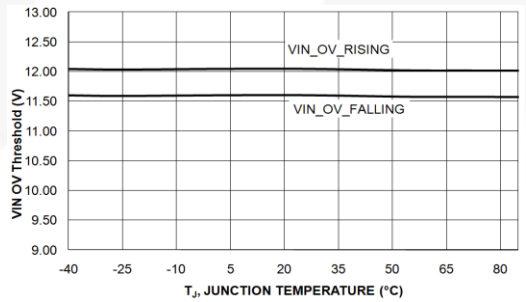


Figure 20. V_{IN_VOVLO} vs. Temperature

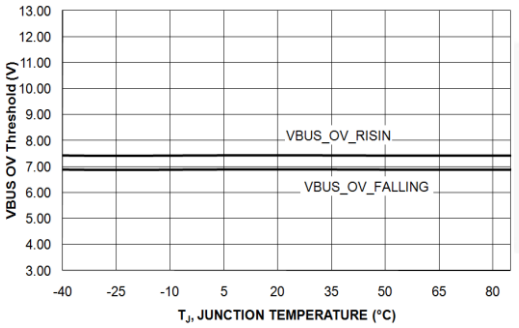


Figure 21. V_{BUS_VOVLO} vs. Temperature

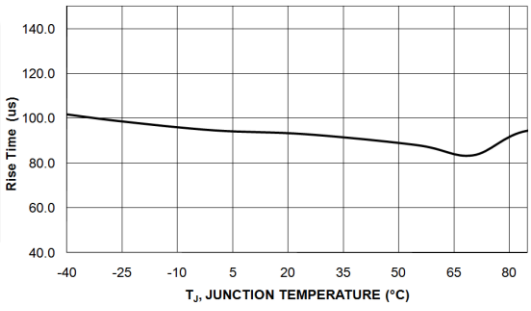


Figure 22. V_{OUT} t_R vs. Temperature

Typical Characteristics (Continued)

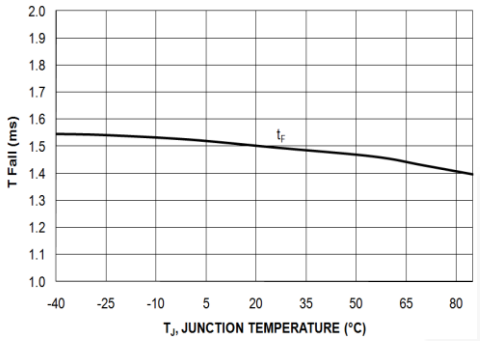


Figure 23. V_{OUT} t_F vs. Temperature

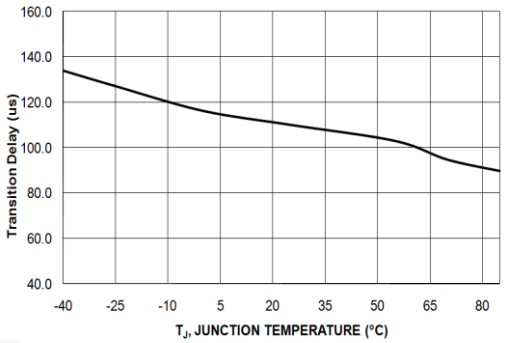


Figure 24. t_{TRAN} vs. Temperature

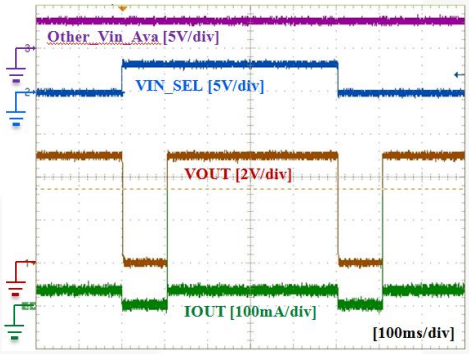


Figure 25. Power Source Transition (V_{IN}=V_{BUS}=5 V, EN=HIGH, V_{IN}_SEL=LOW→HIGH→LOW, C_{OUT}=4.7 µF, R_L=150 Ω)

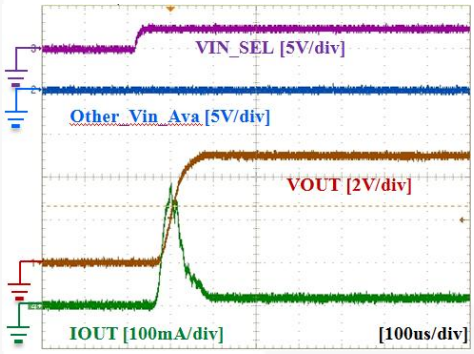


Figure 26. V_{IN} On Response (V_{IN}=GND→5 V, V_{BUS}=EN=GND, C_{OUT}=4.7 µF, R_L=150 Ω)

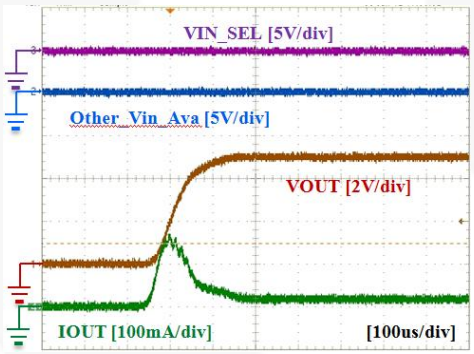


Figure 27. V_{BUS} On Response (V_{BUS}=GND→5 V, V_{IN}=EN=GND, C_{OUT}=4.7 µF, R_L=150 Ω)

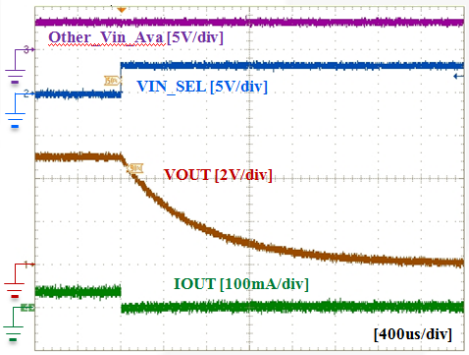


Figure 28. Off Response (V_{IN}=V_{BUS}=5 V, EN=HIGH, V_{IN}_SEL=LO→HIGH or HIGH→LOW, C_{OUT}=4.7 µF, R_L=150 Ω)

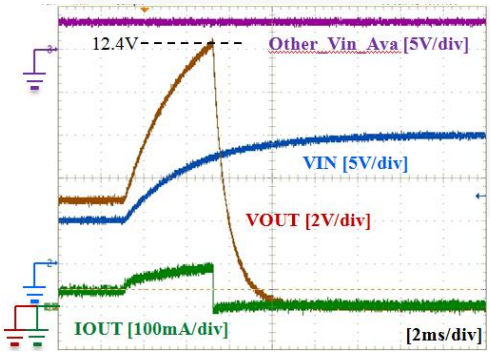


Figure 29. V_{IN} Over-Voltage Protection Response (V_{IN}=5 V→15 V, V_{BUS}=5 V, EN=V_{IN}_SEL=HIGH, C_{OUT}=4.7 µF, R_L=150 Ω)

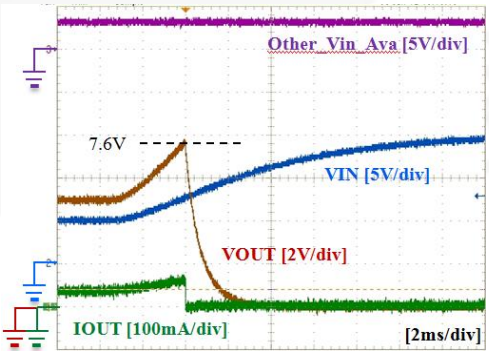


Figure 30. V_{BUS} Over-Voltage Protection Response (V_{BUS}=5 V→15 V, V_{IN}=5 V, EN=HIGH, V_{IN}_SEL=LOW, C_{OUT}=4.7 µF, R_L=150 Ω)

Operation and Application Information

The FPF3040 is a 18 V, 2 A-rated, Dual-Input Single-Output (DISO) load switch with slew-rate-controlled, low-on-resistance, based-on-N-channel MOSFET. The input operating range is from 4 V to 6.5 V at V_{BUS} and from 4 V to 10.5 V at V_{IN}. The internal circuitry is powered from the highest voltage source among V_{IN}, V_{BUS}, and V_{EN}.

Input Power Source Selection

Input power source can be selected by V_{IN_SEL} and DF_IN, respectively, depending on EN state. When EN is HIGH, the input source is selected by V_{IN_SEL} regardless of DF_IN. If V_{IN_SEL} is LOW, V_{BUS} is selected. If V_{IN_SEL} is HIGH, V_{IN} is selected.

Table 2. Input Power Selection by VIN_SEL

EN	V_{IN}>UVLO	V_{BUS}>UVLO	V_{IN_SEL}	DF_IN	V_{OUT}
HIGH	X	X	LOW	X	V_{BUS}
HIGH	X	X	HIGH	X	V_{IN}

When EN is LOW, the input source is selected by DF_IN and the number of valid input sources. If only one input source is valid, or more than UVLO, the source is selected automatically, regardless of DF_IN, to make a charging path in case the battery is depleted. If both V_{BUS} and V_{IN} have valid input sources, the input source is selected by DF_IN. If DF_IN is LOW, V_{IN} is selected. If DF_IN is HIGH or floating, V_{BUS} is selected. DF_IN is biased HIGH with an internal 1 µA pull-up current source.

Table 3. Input Power Selection by DF_IN

EN	V_{IN}>UVLO	V_{BUS}>UVLO	V_{IN_SEL}	DF_IN	V_{OUT}
LOW	YES	NO	HIGH	X	V_{IN}
LOW	NO	YES	LOW	X	V_{BUS}
LOW	YES	YES	LOW	Floating	V_{BUS}
LOW	YES	YES	HIGH	LOW	V_{IN}
LOW	NO	NO	X	X	Floating

V_{IN_SEL} can be the status output to indicate which input power source is used during EN is LOW. If V_{IN} is used, V_{IN_SEL} shows high. If V_{BUS} is used, V_{IN_SEL} shows LOW. The voltage level of HIGH signal is 5.3 V if any one of V_{IN}, V_{BUS} or EN is higher than 5.3 V. The signal is highest voltage among V_{IN}, V_{BUS}, and V_{EN} if none of them is higher than 5.3 V.

EN Voltage for Control Logic Power Supply

Internal control logic is powered from the highest voltage among V_{IN}, V_{BUS}, and V_{EN}. If valid V_{IN} or V_{BUS} higher than UVLO is applied, ON/OFF control by EN should be accomplished with V_{IH}/V_{IL}. If EN powers the internal control block without valid V_{IN} and V_{BUS}, more than 2.5 V is required on the EN pin to operate properly.

Over-Voltage Protection (OVP)

FPF3040 has over-voltage protection at both V_{IN} and V_{BUS}. If V_{IN} or V_{BUS} is higher than 12 V or 7.5 V, respectively, the power switch is off until input voltage is lower than the over-voltage trip level by hysteresis voltage of 0.5 V.

Reverse Power Supply for OTG

FPF3040 has a bi-directional switch so reverse power is allowed for On-The-Go (OTG) operation. Even if both V_{IN} and V_{BUS} are not available, reverse power can be also supported if internal control circuitry is powered by EN.

Reverse-Current Blocking

FPF3040 supports reverse-current blocking during EN LOW and an unselected channel.

Thermal Shutdown

During FPF3040 thermal shutdown, the power switch is turned off if junction temperature reaches over 150°C to avoid damage.

Wireless Charging System

FPF3040 can be used for an input power selector supporting Travel Adaptor (TA) and Wireless Charging (WC) with a single-input-based battery charger or Power Management IC (PMIC), including a charging block as shown in Figure 31. The system can recognize an input power source change between 5 V TA and 5 V WC without detection circuitry because FPF3040 has a 100 ms transition delay. OTG Mode can be supported without an additional power path, such as a MOSFET.

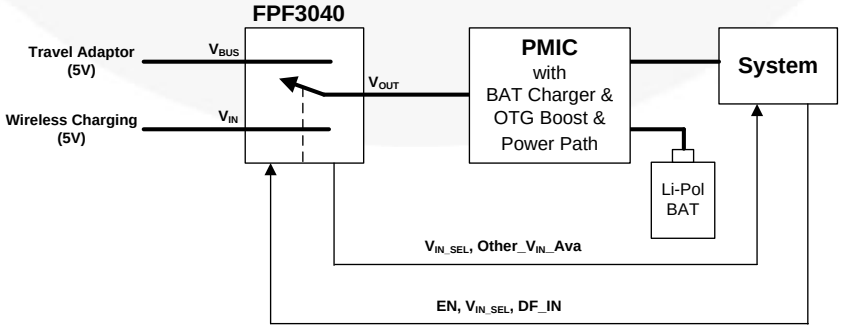
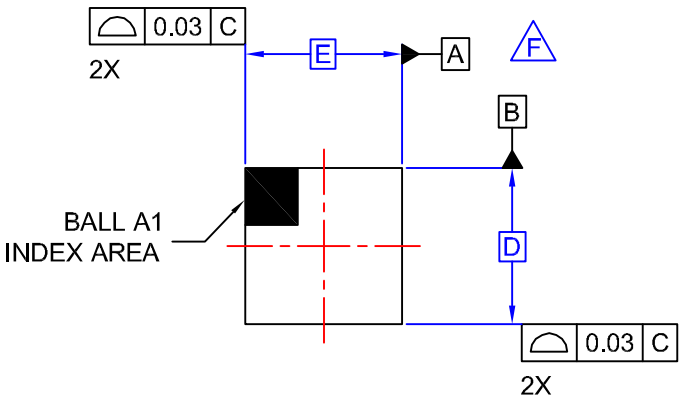


Figure 31. Block Diagram of Input Power Selector for Wireless Charging System

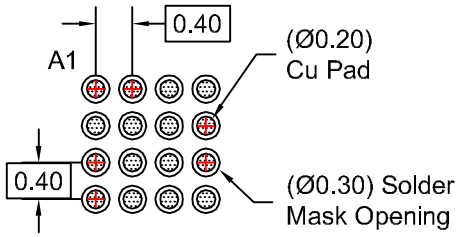
Product Specific Package Information

D	E	X	Y
1.96 mm ±0.03 mm	1.76 mm ±0.03 mm	0.28 mm	0.38 mm

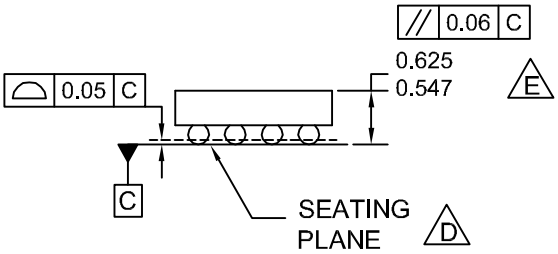
REVISIONS			
REV	DESCRIPTION	DATE	APP'D / SITE
1	Initial drawing release.	3-31-08	L. England
2	Changed land pad solder mask to individual pad openings. Other general updates for drawing consistency.	3-31-08	L. England / FSME

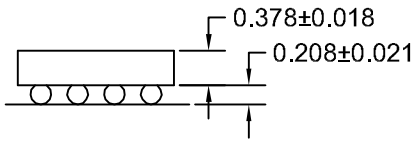


TOP VIEW

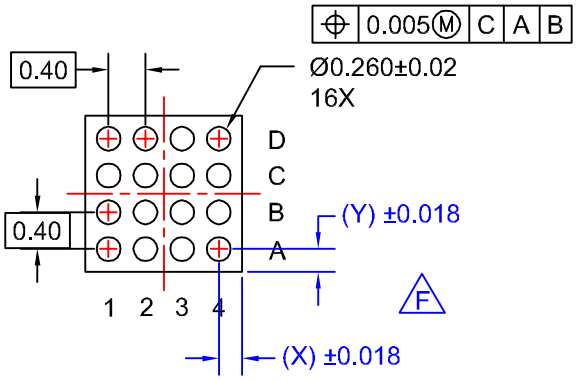


RECOMMENDED LAND PATTERN
(NSMD PAD TYPE)





SIDE VIEWS



BOTTOM VIEW

NOTES:

A. NO JEDEC REGISTRATION APPLIES.

B. DIMENSIONS ARE IN MILLIMETERS.

C. DIMENSIONS AND TOLERANCE PER ASME Y14.5M, 1994.

D. DATUM C IS DEFINED BY THE SPHERICAL CROWNS OF THE BALLS.

E. PACKAGE NOMINAL HEIGHT IS 586 MICRONS ±39 MICRONS (547-625 MICRONS).

F. FOR DIMENSIONS D, E, X, AND Y SEE PRODUCT DATASHEET.

G. DRAWING FILNAME: MKT-UC016AArev2.

APPROVALS	DATE
DRAWN L. England	10-26-09
DFTG. CHK. E. Shacham	10-26-09
ENGR. CHK.	

FAIRCHILD SEMICONDUCTOR™

16BALL WLCSP, 4X4 ARRAY
0.4MM PITCH, 250UM BALL

PROJECTION
INCH
[MM]

SCALE	SIZE	DRAWING NUMBER	REV
N/A	N/A	MKT-UC016AA	2

DO NOT SCALE DRAWING | SHEET 1 of 1

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