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November 2013

### FQB9N50C

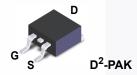
# N-Channel QFET<sup>®</sup> MOSFET 500 V, 9 A, 800 m $\Omega$

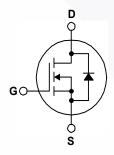
#### **Features**

- 9 A, 500 V,  $R_{DS(on)}$  = 800 m $\Omega$  (Max.) @  $V_{GS}$  = 10 V,  $I_D$  = 4.5 A
- Low Gate Charge (Typ. 28 nC)
- Low Crss (Typ. 24 pF)
- · 100% Avalanche Tested

### Description

This N-Channel enhancement mode power MOSFET is produced using Fairchild Semiconductor's proprietary planar stripe and DMOS technology. This advanced MOSFET technology has been especially tailored to reduce on-state resistance, and to provide superior switching performance and high avalanche energy strength. These devices are suitable for switched mode power supplies, active power factor correction (PFC), and electronic lamp hallasts





### **Absolute Maximum Ratings** T<sub>C</sub> = 25°C unless otherwise noted.

Symbol	Parameter		FQB9N50CTM	Unit
$V_{DSS}$	Drain-Source Voltage		500	V
I <sub>D</sub>	Drain Current - Continuous (T <sub>C</sub> = 25°C)		9	Α
	- Continuous (T <sub>C</sub> = 100°C)		5.4	А
I <sub>DM</sub>	Drain Current - Pulsed	(Note 1)	36	Α
V <sub>GSS</sub>	Gate-Source Voltage		± 30	V
E <sub>AS</sub>	Single Pulsed Avalanche Energy	(Note 2)	360	mJ
I <sub>AR</sub>	Avalanche Current	(Note 1)	9	Α
E <sub>AR</sub>	Repetitive Avalanche Energy	(Note 1)	13.5	mJ
dv/dt	Peak Diode Recovery dv/dt (Note 3		4.5	V/ns
Ъ	Power Dissipation (T <sub>C</sub> = 25°C)		135	W
$P_D$	- Derate above 25°C		1.07	W/°C
T <sub>J</sub> , T <sub>STG</sub>	Operating and Storage Temperature Range		-55 to +150	°C
T <sub>L</sub>	Maximum lead temperature for soldering purposes, 1/8" from case for 5 seconds		300	°C
			300	C

### **Thermal Characteristics**

	Symbol	Parameter	FQB9N50CTM	Unit
F	$R_{ heta JC}$	Thermal Resistance, Junction-to-Case, Max.	0.93	°C/W
F	$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient, Max.	62.5	C/VV

### **Package Marking and Ordering Information**

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
FQB9N50C	FQB9N50CTM	D <sup>2</sup> -PAK	330 mm	24 mm	800 units

### **Electrical Characteristics** $T_C = 25^{\circ}C$ unless otherwise noted.

Symbol	Parameter	Test Conditions	Min	Тур	Max	Unit
Off Cha	racteristics					
BV <sub>DSS</sub>	Drain-Source Breakdown Voltage	$V_{GS} = 0 \text{ V}, I_D = 250 \mu\text{A}$	500			V
ΔBV <sub>DSS</sub> / ΔT <sub>J</sub>	Breakdown Voltage Temperature Coefficient	I <sub>D</sub> = 250 μA, Referenced to 25°C		0.57		V/°C
1	Zero Gate Voltage Drain Current	V <sub>DS</sub> = 500 V, V <sub>GS</sub> = 0 V			1	μΑ
I <sub>DSS</sub>		V <sub>DS</sub> = 400 V, T <sub>C</sub> = 125°C			10	μΑ
I <sub>GSSF</sub>	Gate-Body Leakage Current, Forward	V <sub>GS</sub> = 30 V, V <sub>DS</sub> = 0 V			100	nA
I <sub>GSSR</sub>	Gate-Body Leakage Current, Reverse	V <sub>GS</sub> = -30 V, V <sub>DS</sub> = 0 V			-100	nA
On Cha	racteristics					
V <sub>GS(th)</sub>	Gate Threshold Voltage	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 250 μA	2.0		4.0	V
R <sub>DS(on)</sub>	Static Drain-Source On-Resistance	V <sub>GS</sub> = 10 V, I <sub>D</sub> = 4.5 A		0.65	0.8	Ω
g <sub>FS</sub>	Forward Transconductance	V <sub>DS</sub> = 40 V, I <sub>D</sub> = 4.5 A		6.5		S
C <sub>iss</sub>	c Characteristics Input Capacitance	V <sub>DS</sub> = 25 V, V <sub>GS</sub> = 0 V,		790	1030	pF
C <sub>oss</sub>	Output Capacitance	f = 1.0 MHz		130	170	pF
C <sub>rss</sub>	Reverse Transfer Capacitance	1 – 1.0 WH 12		24	30	pF
Switchi	ng Characteristics					
$t_{d(on)}$	Turn-On Delay Time	V <sub>DD</sub> = 250 V, I <sub>D</sub> = 9 A,		18	45	ns
t <sub>r</sub>	Turn-On Rise Time	$R_G = 25 \Omega$		65	140	ns
$t_{d(off)}$	Turn-Off Delay Time			93	195	ns
t <sub>f</sub>	Turn-Off Fall Time	(Note 4)		64	125	ns
$Q_g$	Total Gate Charge	V <sub>DS</sub> = 400 V, I <sub>D</sub> = 9 A,	/	28	35	nC
$Q_{gs}$	Gate-Source Charge	V <sub>GS</sub> = 10 V		4		nC
$Q_{gd}$	Gate-Drain Charge	(Note 4)		15		nC
Drain-S	ource Diode Characteristics ar	nd Maximum Ratings				
I <sub>S</sub>	Maximum Continuous Drain-Source Diode Forward Current				9	Α
I <sub>SM</sub>	Maximum Pulsed Drain-Source Diode F	Forward Current			36	Α
V <sub>SD</sub>	Drain-Source Diode Forward Voltage	V <sub>GS</sub> = 0 V, I <sub>S</sub> = 9 A			1.4	V
t <sub>rr</sub>	Reverse Recovery Time	V <sub>GS</sub> = 0 V, I <sub>S</sub> = 9 A,		335		ns
Q <sub>rr</sub>	Reverse Recovery Charge	dI <sub>F</sub> / dt = 100 A/μs		2.95		μС

#### NOTES:

<sup>1.</sup> Repetitive Rating : Pulse width limited by maximum junction temperature.

<sup>2.</sup> L = 8 mH, I $_{AS}$  = 9 A, V $_{DD}$  = 50 V, R $_{G}$  = 25  $\Omega$ , starting T $_{J}$  = 25°C.

 $<sup>3.~</sup>I_{SD} \leq~9~A,~di/dt~\leq 200~A/\mu s,~V_{DD} \leq BV_{DSS,}~starting~~T_J = 25^{\circ}C.$ 

<sup>4.</sup> Essentially independent of operating temperature.

### **Typical Characteristics**

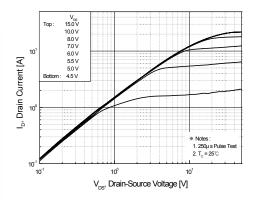


Figure 1. On-Region Characteristics

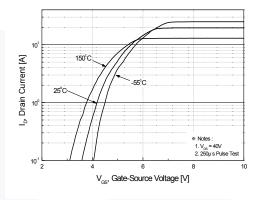


Figure 2. Transfer Characteristics

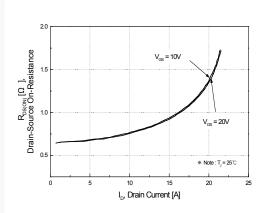


Figure 3. On-Resistance Variation vs Drain Current and Gate Voltage

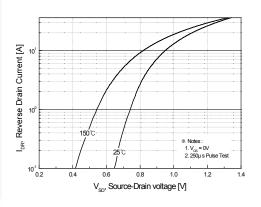


Figure 4. Body Diode Forward Voltage Variation with Source Current and Temperature

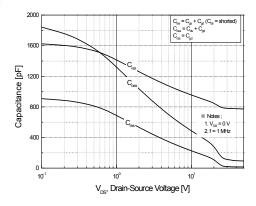


Figure 5. Capacitance Characteristics

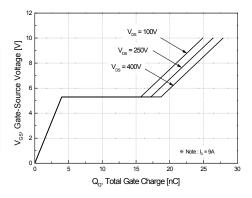


Figure 6. Gate Charge Characteristics

### Typical Characteristics (Continued)

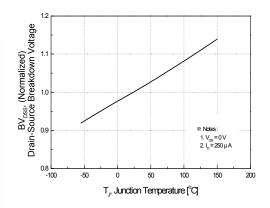


Figure 7. Breakdown Voltage Variation vs Temperature

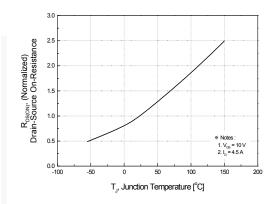


Figure 8. On-Resistance Variation vs Temperature

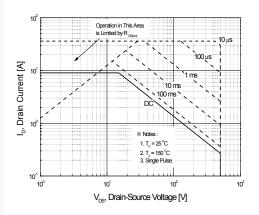


Figure 9. Maximum Safe Operating Area

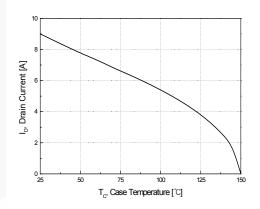


Figure 10. Maximum Drain Current vs Case Temperature

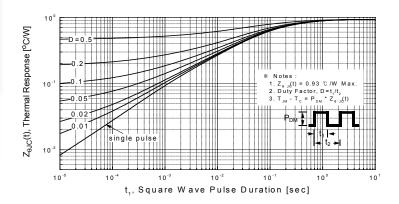


Figure 11. Transient Thermal Response Curve

Figure 12. Gate Charge Test Circuit & Waveform

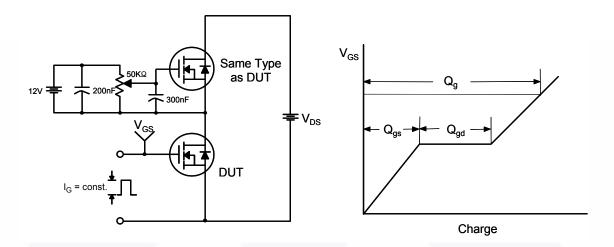


Figure 13. Resistive Switching Test Circuit & Waveforms

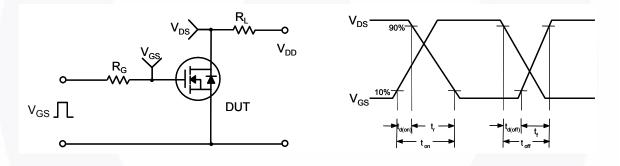
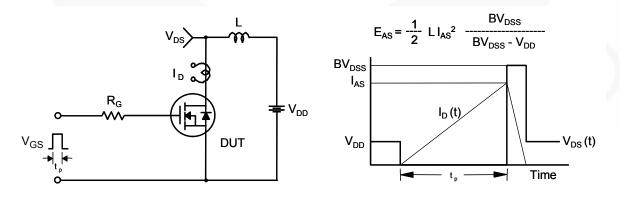


Figure 14. Unclamped Inductive Switching Test Circuit & Waveforms



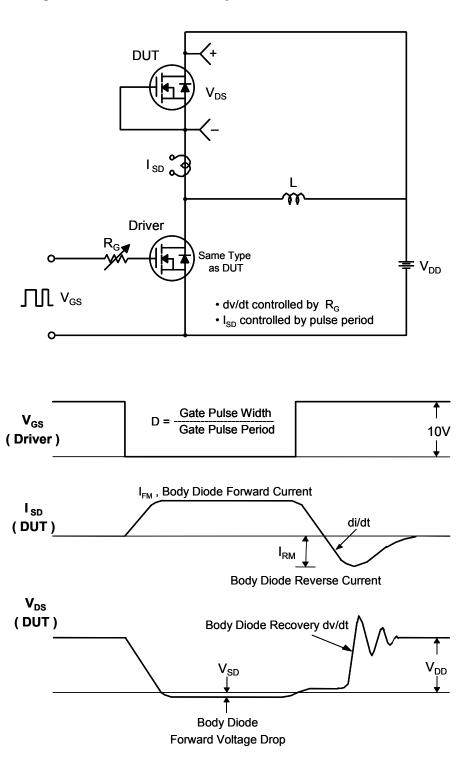


Figure 15. Peak Diode Recovery dv/dt Test Circuit & Waveforms

### **Mechanical Dimensions**

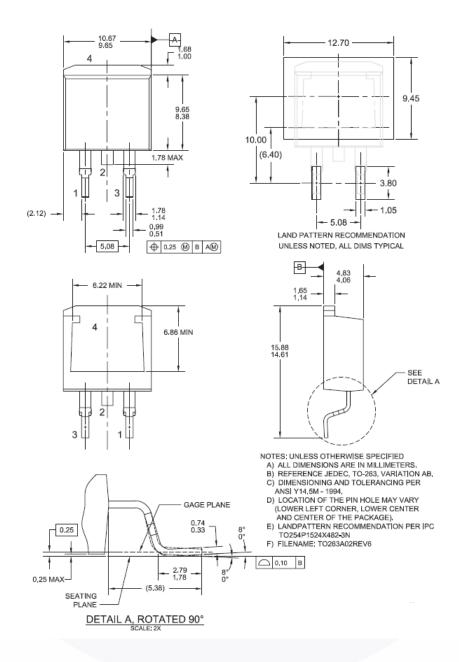


Figure 16. TO263 (D<sup>2</sup>PAK), Molded, 2-Lead, Surface Mount

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