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November 2013

FQI13N50C

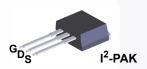
N-Channel QFET[®] MOSFET 500 V, 13 A, 480 m Ω

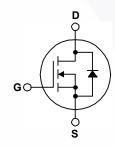
Features

- 13 A, 500 V, $R_{DS(on)}$ = 480 m Ω (Max.) $@V_{GS}$ = 10 V, I_D = 6.5 A
- Low Gate Charge (Typ. 43 nC)
- Low Crss (Typ. 20 pF)
- · 100% Avalanche Tested
- · RoHS Compliant

Description

This N-Channel enhancement mode power MOSFET is produced using Fairchild Semiconductor's proprietary planar stripe and DMOS technology. This advanced MOSFET technology has been especially tailored to reduce on-state resistance, and to provide superior switching performance and high avalanche energy strength. These devices are suitable for switched mode power supplies, active power factor correction (PFC), and electronic lamp ballasts.





Absolute Maximum Ratings T_C = 25°C unless otherwise noted.

Symbol	Parameter		FQI13N50CTU	Unit
V_{DSS}	Drain-Source Voltage		500	V
I _D	Drain Current - Continuous (T _C = 25°C)		13	Α
	- Continuous (T _C = 100°C)		8	Α
I _{DM}	Drain Current - Pulsed	(Note 1)	52	Α
V _{GSS}	Gate-Source Voltage		± 30	V
E _{AS}	Single Pulsed Avalanche Energy		860	mJ
I _{AR}	Avalanche Current	(Note 1)	13	Α
E _{AR}	Repetitive Avalanche Energy	(Note 1)	19.5	mJ
dv/dt	Peak Diode Recovery dv/dt (Note 3)		4.5	V/ns
P _D	Power Dissipation (T _C = 25°C)		195	W
	- Derate above 25°C		1.56	W/°C
T _J , T _{STG}	Operating and Storage Temperature Range		-55 to +150	°C
T _L	Maximum lead temperature for soldering purposes, 1/8" from case for 5 seconds		300	°C
· L			330	

Thermal Characteristics

Symbol	Parameter	FQI13N50CTU	Unit	
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case, Max.	0.64	°C/W	
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient, Max.	62.5	°C/W	

Package Marking and Ordering Information

Device Marking Device		Package Reel Size		Tape Width	Quantity	
FQI13N50C	FQI13N50CTU	I ² -PAK	Tube	N/A	50 units	

Electrical Characteristics $T_C = 25^{\circ}C$ unless otherwise noted.

Symbol	Parameter	Test Conditions	Min	Тур	Max	Unit
Off Cha	racteristics					
BV _{DSS}	Drain-Source Breakdown Voltage	$V_{GS} = 0 \text{ V}, I_D = 250 \mu\text{A}$	500			V
ΔBV _{DSS} / ΔT _J	Breakdown Voltage Temperature Coefficient	I _D = 250 μA, Referenced to 25°C		0.5		V/°C
1	Zero Gate Voltage Drain Current	V _{DS} = 500 V, V _{GS} = 0 V			1	μΑ
I _{DSS}		V _{DS} = 400 V, T _C = 125°C			10	μΑ
I _{GSSF}	Gate-Body Leakage Current, Forward	V _{GS} = 30 V, V _{DS} = 0 V			100	nA
I_{GSSR}	Gate-Body Leakage Current, Reverse	V _{GS} = -30 V, V _{DS} = 0 V			-100	nA
On Cha	racteristics					
V _{GS(th)}	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_{D} = 250 \mu\text{A}$	2.0		4.0	V
R _{DS(on)}	Static Drain-Source On-Resistance	V _{GS} = 10 V, I _D = 6.5 A		0.39	0.48	Ω
g _{FS}	Forward Transconductance	V _{DS} = 40 V, I _D = 6.5 A	\	15		S
C _{iss}	Input Capacitance	V _{DS} = 25 V, V _{GS} = 0 V,		1580	2055	pF
C _{oss}	Output Capacitance Reverse Transfer Capacitance	f = 1.0 MHz		180	235 25	pF pF
orss	Treverse Transfer Capacitance			20	23	рі
Switchi	ng Characteristics					
t _{d(on)}	Turn-On Delay Time	V _{DD} = 250 V, I _D = 13 A,		25	60	ns
t _r	Turn-On Rise Time	$R_G = 25 \Omega$		100	210	ns
t _{d(off)}	Turn-Off Delay Time			130	270	ns
t _f	Turn-Off Fall Time	(Note 4)		100	210	ns
Qg	Total Gate Charge	V _{DS} = 400 V, I _D = 13 A,	/	43	56	nC
Q _{gs}	Gate-Source Charge	V _{GS} = 10 V		7.5		nC
Q _{gd}	Gate-Drain Charge	(Note 4)		18.5		nC
Drain-S	ource Diode Characteristics a	nd Maximum Ratings				
I _S	Maximum Continuous Drain-Source Diode Forward Current				13	Α
I _{SM}	Maximum Pulsed Drain-Source Diode F	Forward Current			52	Α
V _{SD}	Drain-Source Diode Forward Voltage	V _{GS} = 0 V, I _S = 13 A			1.4	V
t _{rr}	Reverse Recovery Time	V _{GS} = 0 V, I _S = 13 A,		410		ns
Q _{rr}	Reverse Recovery Charge	dI _F / dt = 100 A/μs		4.5		μC

NOTES:

 $^{{\}it 1. Repetitive Rating: Pulse width limited by maximum junction temperature.}\\$

^{2.} L =6.0 mH, I_{AS} = 13A, V_{DD} = 50V, R_{G} = 25 Ω , starting T_{J} = 25°C.

 $^{3.~}I_{SD} \leq 13A,~di/dt \leq 200A/\mu s,~V_{DD} \leq BV_{DSS,}~starting~~T_J = 25^{\circ}C.$

^{4.} Essentially independent of operating temperature.

Typical Characteristics

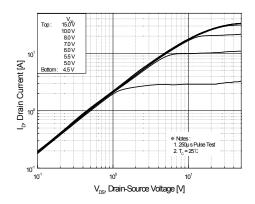


Figure 1. On-Region Characteristics

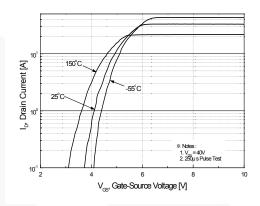


Figure 2. Transfer Characteristics

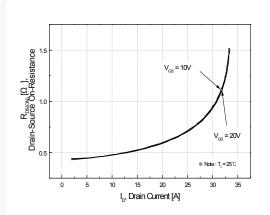


Figure 3. On-Resistance Variation vs Drain Current and Gate Voltage

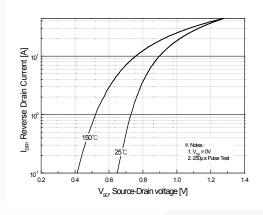


Figure 4. Body Diode Forward Voltage Variation with Source Current and Temperature

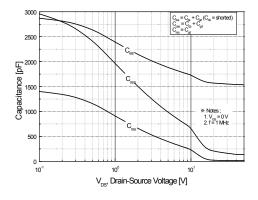


Figure 5. Capacitance Characteristics

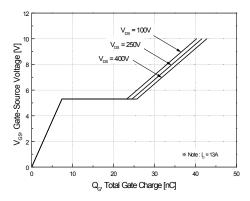


Figure 6. Gate Charge Characteristics

Package Dimensions (Continued)

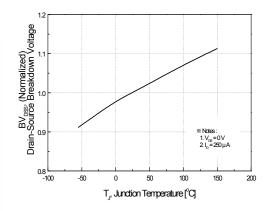


Figure 7. Breakdown Voltage Variation vs Temperature

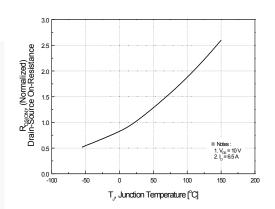


Figure 8. On-Resistance Variation vs Temperature

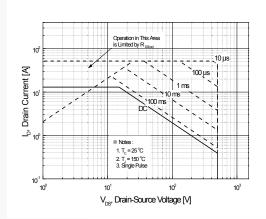


Figure 9. Maximum Safe Operating Area

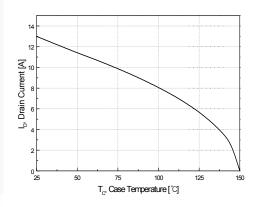


Figure 10. Maximum Drain Current vs Case Temperature

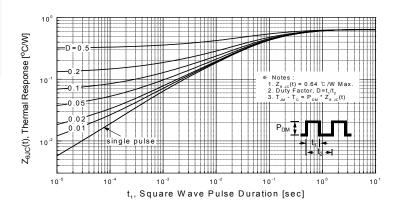


Figure 11. Transient Thermal Response Curve

Figure 12. Gate Charge Test Circuit & Waveform

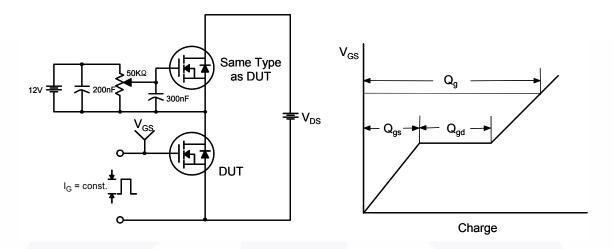


Figure 13. Resistive Switching Test Circuit & Waveforms

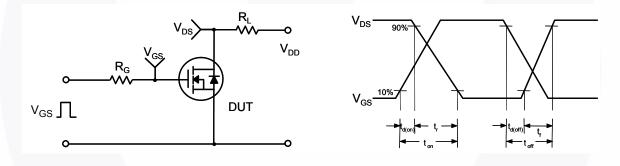
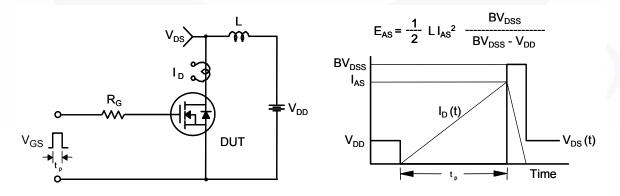


Figure 14. Unclamped Inductive Switching Test Circuit & Waveforms



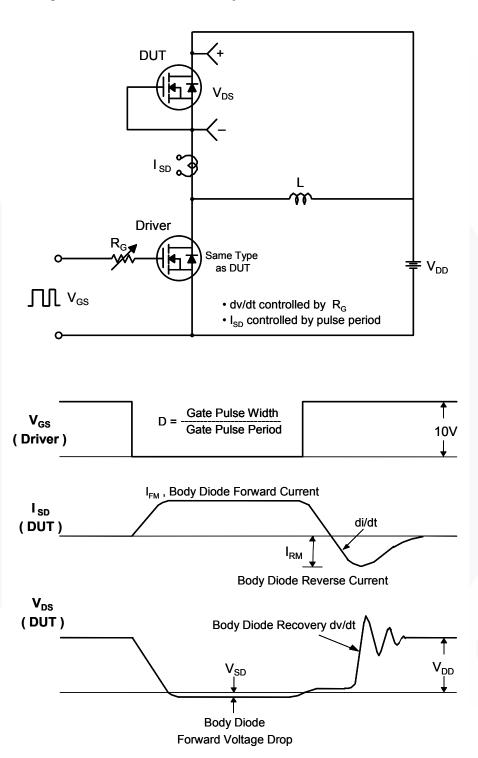


Figure 15. Peak Diode Recovery dv/dt Test Circuit & Waveforms

Mechanical Dimensions

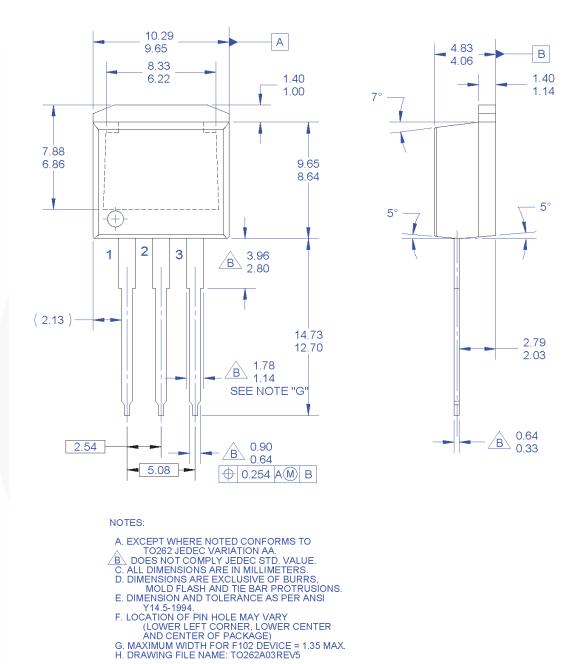


Figure 16. TO262 (I²PAK), Molded, 3-Lead, Jedec Variation AA

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