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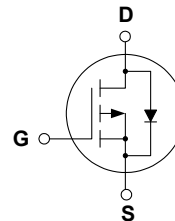
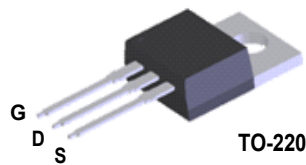
FQP17P10 **P-Channel QFET® MOSFET** **- 100 V, - 16.5 A, 190 mΩ**

Description

This P-Channel enhancement mode power MOSFET is produced using Fairchild Semiconductor®'s proprietary planar stripe and DMOS technology. This advanced MOSFET technology has been especially tailored to reduce on-state resistance, and to provide superior switching performance and high avalanche energy strength. These devices are suitable for switched mode power supplies, audio amplifier, DC motor control, and variable switching power applications.

Features

- -16.5 A, -100 V, $R_{DS(on)} = 190 \text{ m}\Omega$ (Max.) @ $V_{GS} = -10 \text{ V}$, $I_D = -8.25 \text{ A}$
- Low Gate Charge (Typ. 30 nC)
- Low C_{rss} (Typ. 100 pF)
- 100% Avalanche Tested
- 175°C Maximum Junction Temperature Rating



Absolute Maximum Ratings $T_C = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter		FQP17P10	Unit
V _{DSS}	Drain-Source Voltage		-100	V
I _D	Drain Current	- Continuous (T _C = 25°C)	-16.5	A
		- Continuous (T _C = 100°C)	-11.7	A
I _{DM}	Drain Current	- Pulsed (Note 1)	-66	A
V _{GSS}	Gate-Source Voltage		± 30	V
E _{AS}	Single Pulsed Avalanche Energy (Note 2)		580	mJ
I _{AR}	Avalanche Current (Note 1)		-16.5	A
E _{AR}	Repetitive Avalanche Energy (Note 1)		10	mJ
dv/dt	Peak Diode Recovery dv/dt (Note 3)		-6.0	V/ns
P _D	Power Dissipation (T _C = 25°C)		100	W
	- Derate above 25°C		0.67	W/°C
T _J , T _{STG}	Operating and Storage Temperature Range		-55 to +175	°C
T _L	Maximum lead temperature for soldering purposes, 1/8" from case for 5 seconds		300	°C

Thermal Characteristics

Symbol	Parameter	FQP17P10	Unit
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case, Max.	1.5	$^\circ\text{C/W}$
$R_{\theta CS}$	Thermal Resistance, Case-to-Sink, Typ.	0.5	$^\circ\text{C/W}$
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient, Max.	62.5	$^\circ\text{C/W}$

Electrical Characteristics $T_C = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
Off Characteristics						
BV _{DSS}	Drain-Source Breakdown Voltage	V _{GS} = 0 V, I _D = -250 μA	-100	--	--	V
ΔBV _{DSS} / ΔT _J	Breakdown Voltage Temperature Coefficient	I _D = -250 μA, Referenced to 25°C	--	-0.1	--	V/°C
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} = -100 V, V _{GS} = 0 V	--	--	-1	μA
		V _{DS} = -80 V, T _C = 150°C	--	--	-10	μA
I _{GSSF}	Gate-Body Leakage Current, Forward	V _{GS} = -30 V, V _{DS} = 0 V	--	--	-100	nA
I _{GSSR}	Gate-Body Leakage Current, Reverse	V _{GS} = 30 V, V _{DS} = 0 V	--	--	100	nA
On Characteristics						
V _{GS(th)}	Gate Threshold Voltage	V _{DS} = V _{GS} , I _D = -250 μA	-2.0	--	-4.0	V
R _{DS(on)}	Static Drain-Source On-Resistance	V _{GS} = -10 V, I _D = -8.25 A	--	0.14	0.19	Ω
g _{FS}	Forward Transconductance	V _{DS} = -40 V, I _D = -8.25 A	--	9.9	--	S
Dynamic Characteristics						
C _{iss}	Input Capacitance	V _{DS} = -25 V, V _{GS} = 0 V, f = 1.0 MHz	--	850	1100	pF
C _{oss}	Output Capacitance		--	310	400	pF
C _{rss}	Reverse Transfer Capacitance		--	100	130	pF
Switching Characteristics						
t _{d(on)}	Turn-On Delay Time	V _{DD} = -50 V, I _D = -16.5 A, R _G = 25 Ω (Note 4)	--	17	45	ns
t _r	Turn-On Rise Time		--	200	410	ns
t _{d(off)}	Turn-Off Delay Time		--	45	100	ns
t _f	Turn-Off Fall Time		--	100	210	ns
Q _g	Total Gate Charge	V _{DS} = -80 V, I _D = -16.5 A, V _{GS} = -10 V (Note 4)	--	30	39	nC
Q _{gs}	Gate-Source Charge		--	4.8	--	nC
Q _{gd}	Gate-Drain Charge		--	17	--	nC
Drain-Source Diode Characteristics and Maximum Ratings						
I _S	Maximum Continuous Drain-Source Diode Forward Current		--	--	-16.5	A
I _{SM}	Maximum Pulsed Drain-Source Diode Forward Current		--	--	-66	A
V _{SD}	Drain-Source Diode Forward Voltage	V _{GS} = 0 V, I _S = -16.5 A	--	--	-4.0	V
t _{rr}	Reverse Recovery Time	V _{GS} = 0 V, I _S = -16.5 A,	--	120	--	ns
Q _{rr}	Reverse Recovery Charge	dI _F / dt = 100 A/μs	--	0.52	--	μC

Notes:

1. Repetitive Rating ; Pulse width limited by maximum junction temperature
2. $L = 3.2\text{ mH}$, $I_{AS} = -16.5\text{ A}$, $V_{DD} = -25\text{ V}$, $R_G = 25\text{ }\Omega$, Starting $T_J = 25^\circ\text{C}$
3. $I_{SD} \leq -16.5\text{ A}$, $dI/dt \leq 300\text{ A}/\mu\text{s}$, $V_{DD} \leq BV_{DSS}$, Starting $T_J = 25^\circ\text{C}$
4. Essentially independent of operating temperature

Typical Characteristics

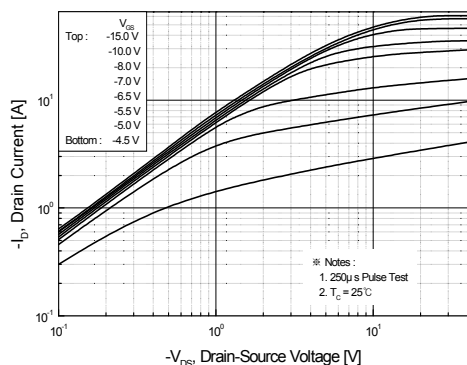


Figure 1. On-Region Characteristics

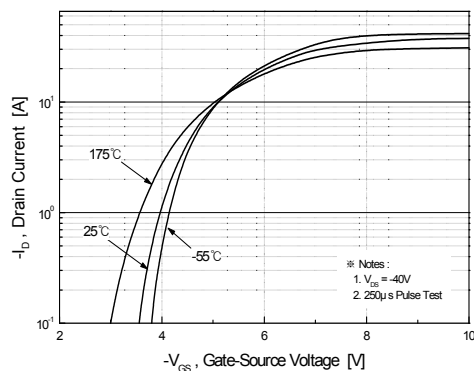


Figure 2. Transfer Characteristics

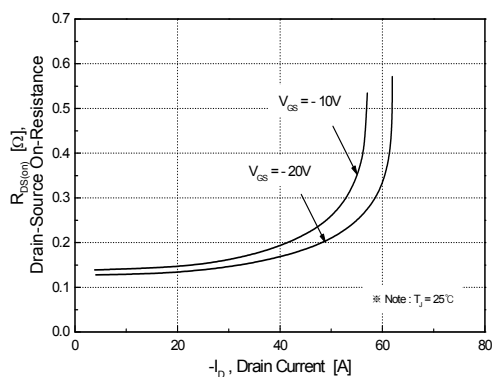


Figure 3. On-Resistance Variation vs. Drain Current and Gate Voltage

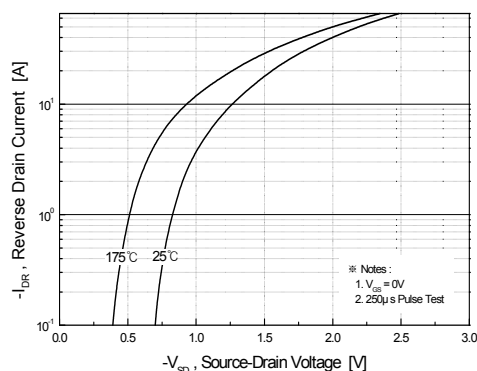


Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature

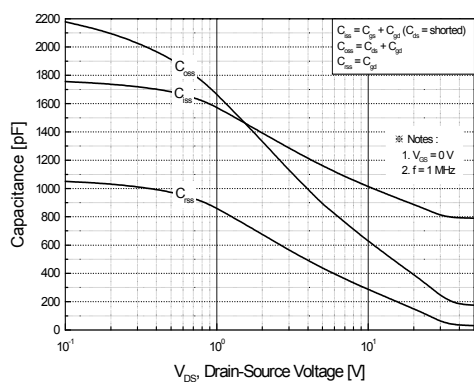


Figure 5. Capacitance Characteristics

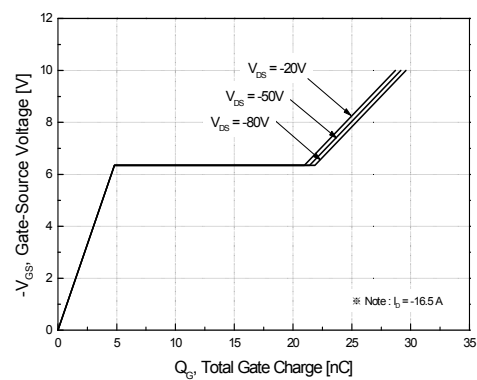


Figure 6. Gate Charge Characteristics

Dimensions in Millimeters

Typical Characteristics (Continued)

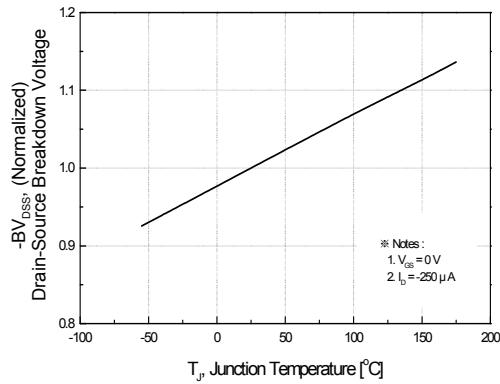


Figure 7. Breakdown Voltage Variation vs. Temperature

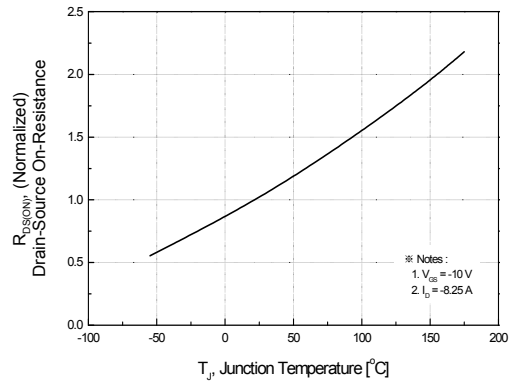


Figure 8. On-Resistance Variation vs. Temperature

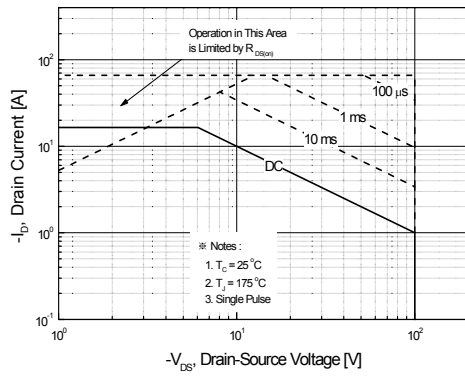


Figure 9. Maximum Safe Operating Area

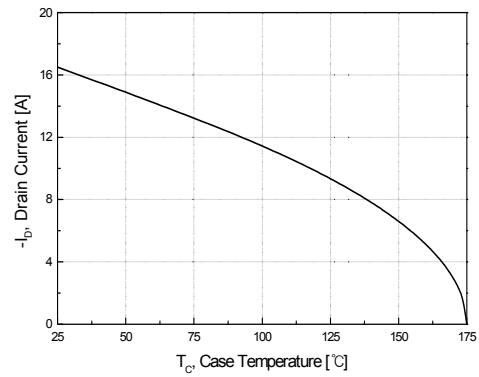


Figure 10. Maximum Drain Current vs. Case Temperature

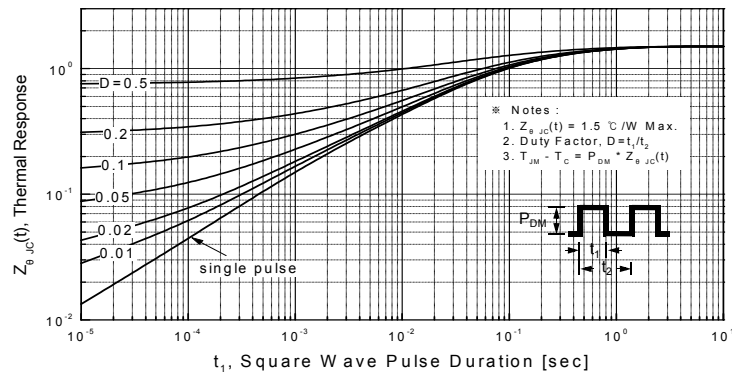
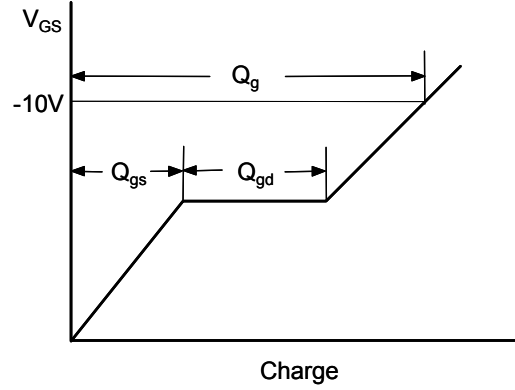
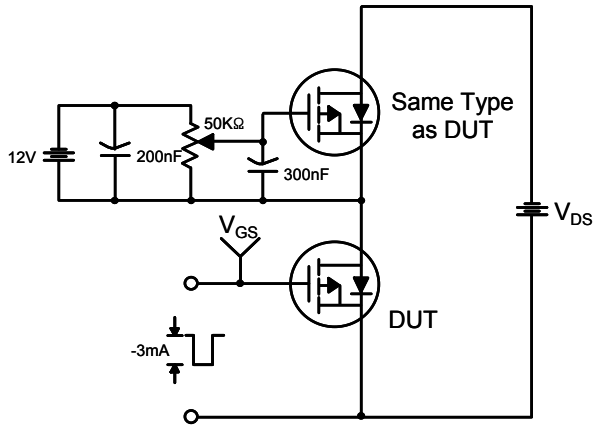
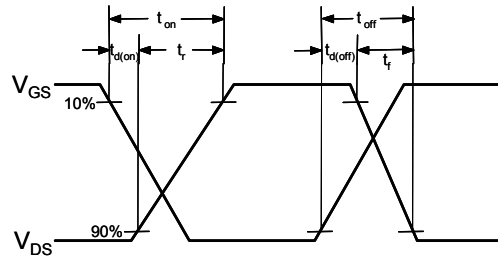
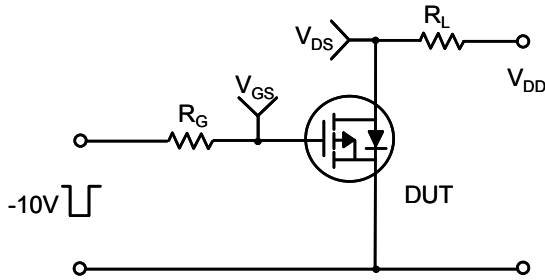


Figure 11. Transient Thermal Response Curve

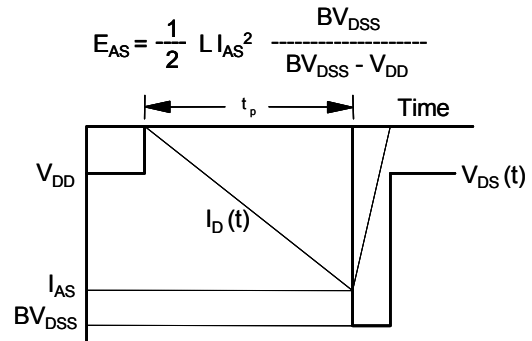
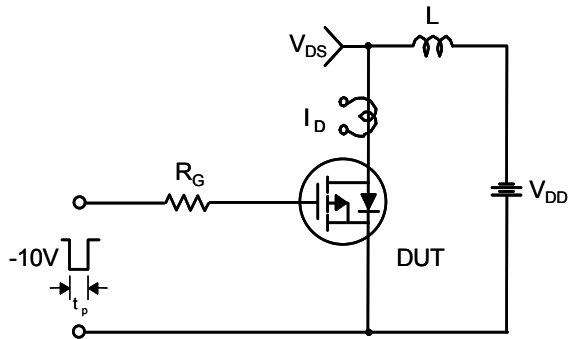
Gate Charge Test Circuit & Waveform



Resistive Switching Test Circuit & Waveforms

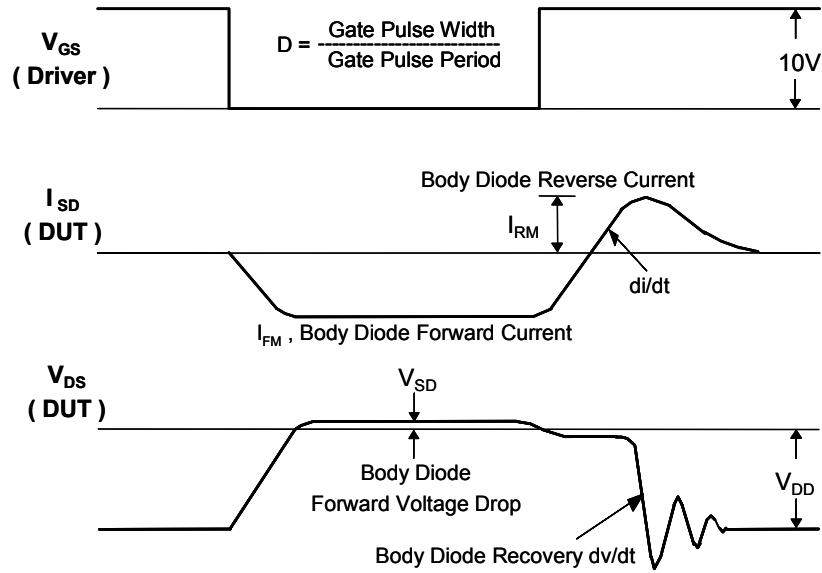
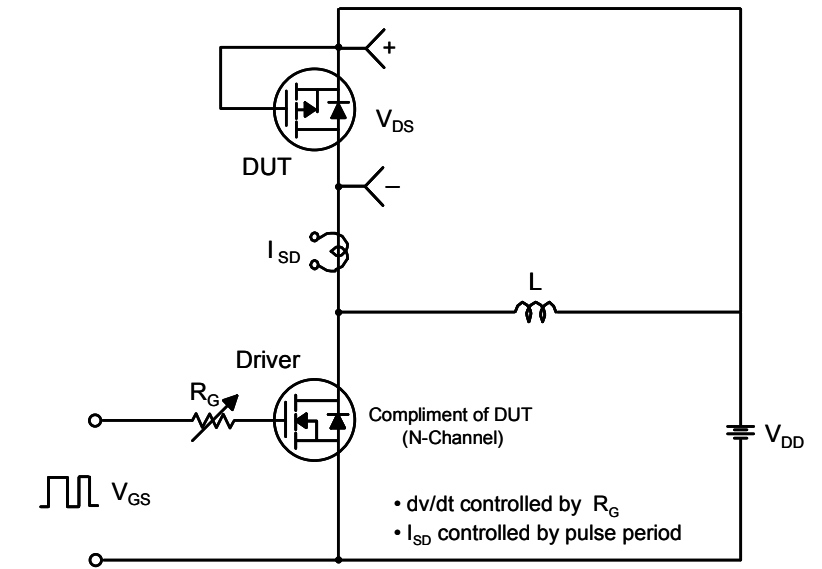


Unclamped Inductive Switching Test Circuit & Waveforms



Dimensions in Millimeters

Peak Diode Recovery dv/dt Test Circuit & Waveforms



Technical drawing of a TO-220B package showing three views: front, side, and top. The front view includes dimensions for pin spacing (1.91, 2.54, 5.08), pin diameter (1.78, 1.14, 1.02, 0.38), and body dimensions (10.67, 9.65, 3.43, 2.54, 16.51, 14.22). It also shows a circular pin hole with a diameter of 4.09 and a tolerance of 3.50. The side view shows the package height (4.83, 3.56) and pin angle (7°, 3°). The top view shows the package width (8.89, 6.86) and pin spacing (3, 2, 1). A table of dimensions and tolerances is provided at the bottom right.

Feature	Dimension	Tolerance	Material	Notes
Pin Hole Diameter	4.09	3.50	B	Reference JEDEC, TO-220, Issue K, Variation AB, Dated April, 2002.
Pin Spacing	1.91, 2.54, 5.08	0.36	B	All dimensions are in millimeters.
Pin Diameter	1.78, 1.14, 1.02, 0.38	0.36	B	Dimensioning and tolerancing per ANSI Y14.5 - 1973.
Pin Angle	7°, 3°	0.61	B	Location of the pin hole may vary (lower left corner, lower center and center of the package).
Package Height	4.83, 3.56	0.33	B	Does not comply JEDEC standard value.
Package Width	8.89, 6.86	0.33	B	"A1" dimensions represent like below:
Pin Spacing (Top View)	3, 2, 1	0.33	B	Single Gauge = 0.51 - 0.61
Pin Spacing (Side View)	1.78, 1.14, 1.02, 0.38	0.33	B	Dual Gauge = 1.14 - 1.40
Pin Angle (Side View)	5°, 3°	0.33	B	Drawing file name: TO220B03REV6

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