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November 2013

FQP55N10

N-Channel QFET[®] MOSFET 100 V, 55 A, 26 m Ω

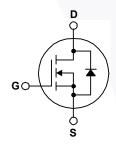
Description

This N-Channel enhancement mode power MOSFET is produced using Fairchild Semiconductor's proprietary planar stripe and DMOS technology. This advanced MOSFET technology has been especially tailored to reduce on-state resistance, and to provide superior switching performance and high avalanche energy strength. These devices are suitable for switched mode power supplies, audio amplifier, DC motor control, and variable switching power applications.

Features

- 55 A, 100 V, $R_{DS(on)}$ = 26 m Ω (Max.) @ V_{GS} = 10 V, I_D = 27.5 A
- Low Gate Charge (Typ. 75 nC)
- · Low Crss (Typ. 130 pF)
- · 100% Avalanche Tested
- 175°C Maximum Junction Temperature Rating





Absolute Maximum Ratings $T_C = 25^{\circ}C$ unless otherwise noted.

Symbol	Parameter		FQP55N10	Unit
V_{DSS}	Drain-Source Voltage		100	V
I _D	Drain Current - Continuous (T _C = 25°C)		55	Α
	- Continuous (T _C = 100°C)		38.9	Α
I _{DM}	Drain Current - Pulsed	(Note 1)	220	Α
V_{GSS}	Gate-Source Voltage		± 25	V
E _{AS}	Single Pulsed Avalanche Energy	(Note 2)	1100	mJ
I _{AR}	Avalanche Current	(Note 1)	55	Α
E _{AR}	Repetitive Avalanche Energy	(Note 1)	15.5	mJ
dv/dt	Peak Diode Recovery dv/dt	(Note 3)	6.0	V/ns
P_{D}	Power Dissipation (T _C = 25°C)		155	W
	- Derate above 25°C		1.03	W/°C
T _J , T _{STG}	Operating and Storage Temperature Range		-55 to +175	°C
T _L	Maximum Lead Temperature for Soldering, 1/8" from Case for 5 seconds		300	°C
			300	C

Thermal Characteristics

Symbol	Parameter	FQP55N10	Unit	
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case, Max.	0.97	°C/W	
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient, Max.	62.5	°C/W	

Marking and Ordering Information

Part Number	Top Mark	Package	Packing Method	Reel Size	Tape Width	Quantity
FQP55N10	FQP55N10	TO-220	Tube	N/A	N/A	50 units

Electrical Characteristics T_C = 25°C unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Тур	Max	Unit
Off Cha	aracteristics					
BV _{DSS}	Drain-Source Breakdown Voltage	V _{GS} = 0 V, I _D = 250 μA	100			V
ΔBV _{DSS} / ΔΤ _J	Breakdown Voltage Temperature Coefficient	I _D = 250 μA, Referenced to 25°C		0.1		V/°C
Inss		V _{DS} = 100 V, V _{GS} = 0 V			1	μΑ
	Zero Gate Voltage Drain Current	V _{DS} = 80 V, T _C = 150°C			10	μΑ
I _{GSSF}	Gate-Body Leakage Current, Forward	V _{GS} = 25 V, V _{DS} = 0 V			100	nA
I _{GSSR}	Gate-Body Leakage Current, Reverse	V _{GS} = -25 V, V _{DS} = 0 V			-100	nA
On Cha	aracteristics					
V _{GS(th)}	Gate Threshold Voltage	V _{DS} = V _{GS} , I _D = 250 μA	2.0		4.0	V
R _{DS(on)}	Static Drain-Source On-Resistance	V _{GS} = 10 V, I _D = 27.5 A		0.021	0.026	Ω
9 _{FS}	Forward Transconductance	V _{DS} = 40 V, I _D = 27.5 A		38		S
Dynam	ic Characteristics					
C _{iss}	Input Capacitance	V _{DS} = 25 V, V _{GS} = 0 V,		2100	2730	pF
Coss	Output Capacitance	f = 1.0 MHz		640	830	pF
C _{rss}	Reverse Transfer Capacitance			130	170	pF
Switchi	ing Characteristics					
t _{d(on)}	Turn-On Delay Time	V_{DD} = 50 V, I_{D} = 55 A, R_{G} = 25 Ω (Note 4)		25	60	ns
t _r	Turn-On Rise Time			250	510	ns
t _{d(off)}	Turn-Off Delay Time			110	230	ns
t _f	Turn-Off Fall Time			140	290	ns
Qg	Total Gate Charge	V_{DS} = 80 V, I_{D} = 55 A, V_{GS} = 10 V (Note 4)		75	98	nC
Q _{gs}	Gate-Source Charge			13		nC
Q _{gd}	Gate-Drain Charge			36	/-	nC
1	Source Diode Characteristics a	nd Maximum Ratings				
I _S	Maximum Continuous Drain-Source Diode Forward Current				55	Α
I _{SM}	Maximum Pulsed Drain-Source Diode F	Source Diode Forward Current			220	Α
V _{SD}	Drain-Source Diode Forward Voltage	V _{GS} = 0 V, I _S = 55 A		//	1.5	V
t _{rr}	Reverse Recovery Time	V _{GS} = 0 V, I _S = 55 A,		100		ns
Q _{rr}	Reverse Recovery Charge	$dI_{F} / dt = 100 A/\mu s$		380		nC

- **Notes:** 1. Repetitive Rating : Pulse width limited by maximum junction temperature. 2. L = 0.55 mH, I_{AS} = 55 A, V_{DD} = 25 V, R_G = 25 Ω , starting T_J = 25°C. 3. $I_{SD} \le$ 55 A, di/dt \le 300 A/ μ s, $V_{DD} \le$ BV $_{DSS}$, starting T_J = 25°C. 4. Essentially independent of operating temperature.

Typical Characteristics

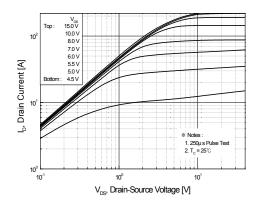


Figure 1. On-Region Characteristics

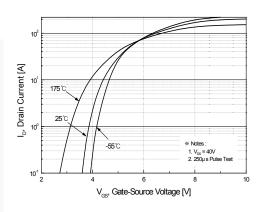


Figure 2. Transfer Characteristics

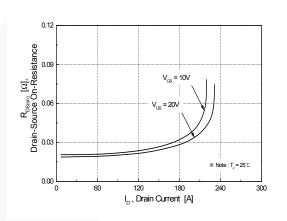


Figure 3. On-Resistance Variation vs. Drain Current and Gate Voltage

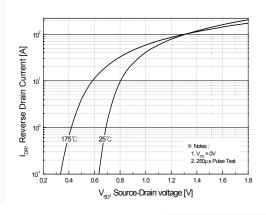


Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature

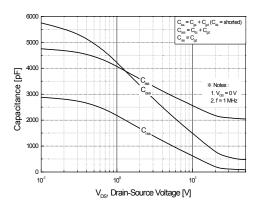


Figure 5. Capacitance Characteristics

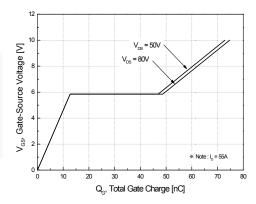


Figure 6. Gate Charge Characteristics

Typical Characteristics (Continued)

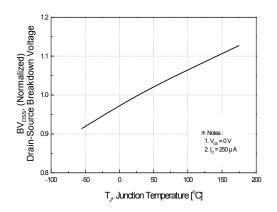


Figure 7. Breakdown Voltage Variation vs. Temperature

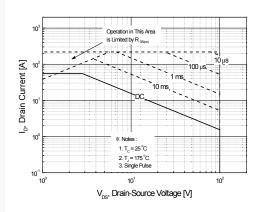


Figure 9. Maximum Safe Operating Area

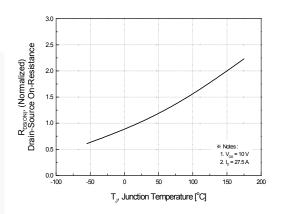


Figure 8. On-Resistance Variation vs. Temperature

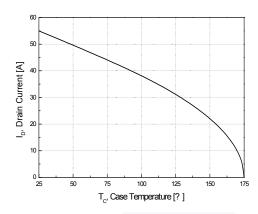


Figure 10. Maximum Drain Current vs. Case Temperature

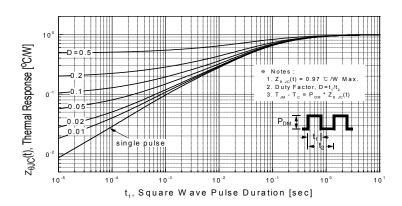


Figure 11. Transient Thermal Response Curve

Figure 12. Gate Charge Test Circuit & Waveform

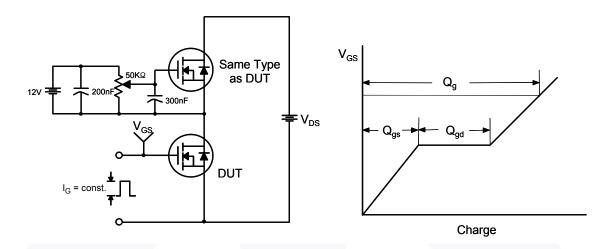


Figure 13. Resistive Switching Test Circuit & Waveforms

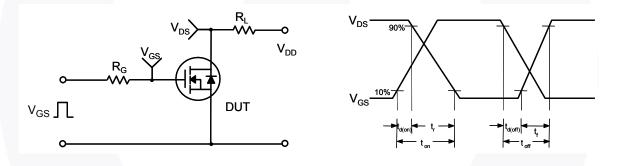
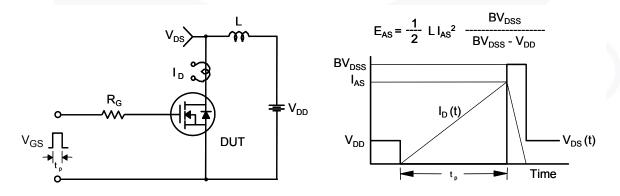


Figure 14. Unclamped Inductive Switching Test Circuit & Waveforms



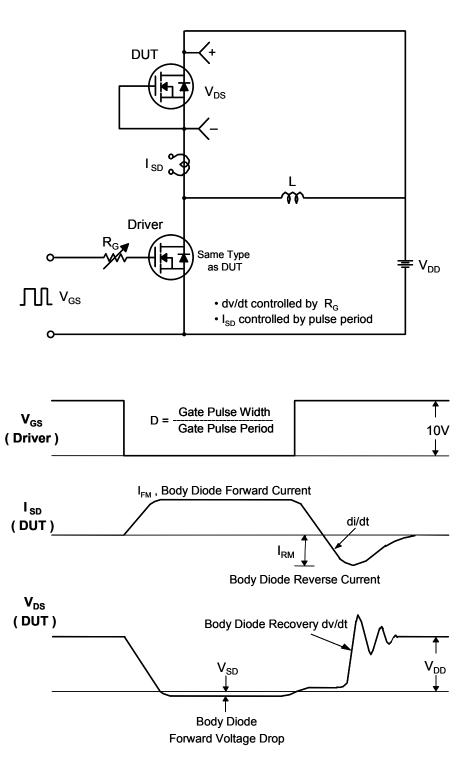
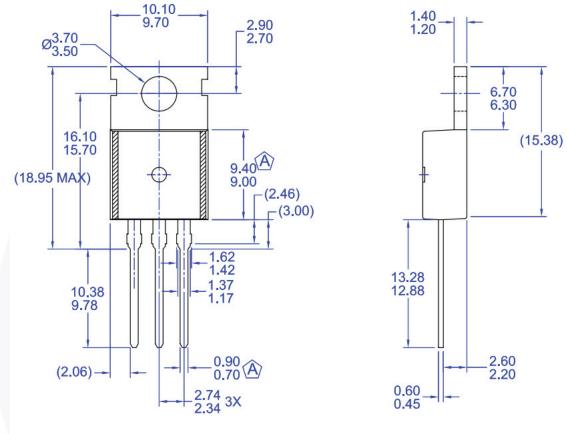


Figure 15. Peak Diode Recovery dv/dt Test Circuit & Waveforms

Mechanical Dimensions



4.70 4.30 10.20 9.80

NOTES:

- (A) CONFORMS TO JEDEC TO-220 VARIATION AB EXCEPT WHERE NOTED
- B) ALL DIMENSIONS ARE IN MILLIMETERS.
- C) DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.
- D) DRAWING FILE/REVISION: MKT-TO220Y03REV1

Figure 16. TO220, Molded, 3-Lead, Jedec Variation AB

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