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FSA1208
Low-Power, Eight-Port, High-Speed Isolation Switch

Features

- Low On Capacitance: 6 pF Typical
- Low On Resistance: 15 Ω Typical
- Low Power Consumption: 1 A Maximum
- 10 µA Maximum I_{CCT} over an Expanded Voltage Range (V_{IN}=2.3 V, V_{CC}=4.3 V)
- Wide -3 dB Bandwidth: > 400 MHz
- Packaged in Space-Saving 20-Lead MLP (2.5 x 4.5 mm)
- 7.5 kV ESD Rating; >16 kV Power/GND ESD Rating
- Low C_{OFF} Capacitance: 2.5 pF Typical

Applications

- DIMM DDR Memory

Description

The FSA1208 is a low-power, eight-port, high-speed switch. This part is configured as a single-pole, single-throw switch and is optimized for isolating a high-speed source, such as a DDR memory bus. The FSA1208 features an extremely low on capacitance (C_{ON}) of 6 pF Superior channel-to-channel crosstalk minimizes interference.

The FSA1208 contains special circuitry on the A & B pins that allows the device to withstand an over-voltage condition. This device is also designed to minimize current consumption even when the control voltage applied to the /OE pin is lower than the supply voltage (V_{CC}). Applications include port isolation and switching in DDR memory modules, portable cell phones, PDAs, digital cameras, printers, and notebook computers.

Ordering Information

Part Number	Top Mark	Operating Temperature Range	Package
FSA1208BQX	F1208	-40 to +85°C	20-Lead, Quad, Molded Leadless Package (MLP), 2.5 x 4.5 mm

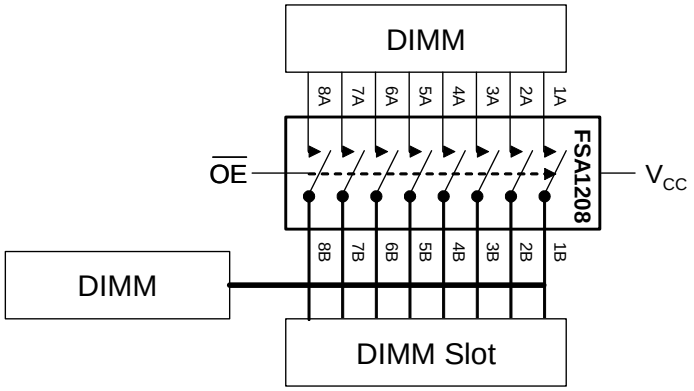


Figure 1. Analog Symbol

October-2017, Rev. 2

Publication Order Number:
FSA1208/D

Pin Configurations

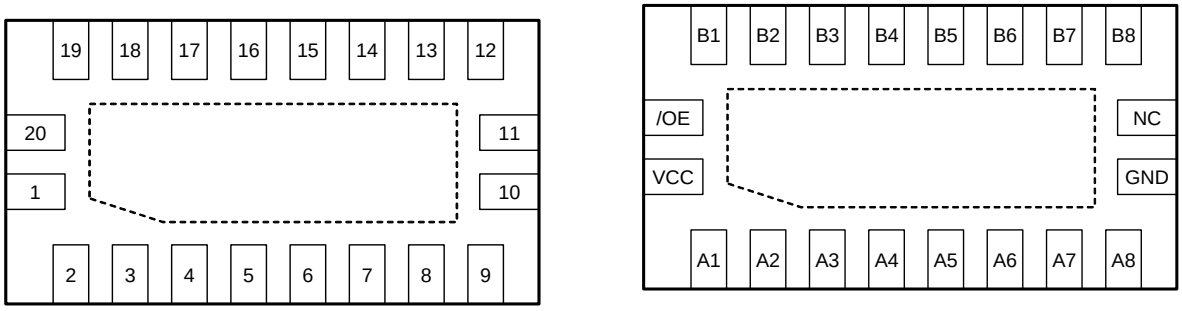


Figure 2. Pin Assignments for MLP (Top Through View)

Pin Definitions

Pin #	Name	Description
20	/OE	Switch Enable
2-9	A1-A8	A Side of Bus
12-19	B8-B1	B Side of Bus
11	NC	No Connection
1	VCC	Power
10	GND	Ground

Truth Table

/OE	Function
HIGH	Disconnect
LOW	A1-A8=B1-B8

Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Parameter		Min.	Max.	Unit
V_{CC}	Supply Voltage		-0.50	+5.25	V
V_{CNTRL}	DC Input Voltage (/OE)[1]		-0.50	V_{CC}	V
V_{SW}	DC Switch I/O Voltage[1]		-0.50	5.25	V
I_{IK}	DC Input Diode Current		-50		mA
I_{OUT}	DC Output Current			50	mA
T_{STG}	Storage Temperature		-65	+150	°C
ESD	Human Body Model, JEDEC: JESD22-A114	All Pins		7.5	kV
		I/O to GND		8	
		Power to GND		16	
	Charged Device Model, JEDEC: JESD22-C101			2	

Note:

1. The input and output negative ratings may be exceeded if the input and output diode current ratings are observed.

Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. ON Semiconductor does not recommend exceeding them or designing to Absolute Maximum Ratings.

Symbol	Parameter	Min.	Max.	Unit
V_{CC}	Supply Voltage	2.3	4.3	V
V_{CNTRL}[2]	Control Input Voltage (S, /OE)	0	V_{CC}	V
V_{SW}	Switch I/O Voltage	-0.5	V_{CC}	V
T_A	Operating Temperature	-40	+85	°C

Note:

2. The control input must be held HIGH or LOW; it must not float.

DC Electrical Characteristics

All typical values are at 25°C unless otherwise specified.

Symbol	Parameter	Conditions	V_{CC} (V)	T_A=- 40°C to +85°C			Units
				Min.	Typ.	Max.	
V_{IK}	Clamp Diode Voltage	I_{IN}=-18 mA	2.5			-1.2	V
V_{IH}	Input Voltage High		2.3 to 3.6	1.3			V
			4.3	1.7			V
V_{IL}	Input Voltage Low		2.3 to 3.6			0.5	V
			4.3			0.7	V
I_{IN}	Control Input Leakage	V_{SW}=0 to V_{CC}	4.3	-1		1	µA
I_{OZ}	Off State Leakage	0 ≤ A, B ≤ 3.6 V	4.3	-2		2	µA
R_{ON}	Switch On Resistance[3]	V_{SW}=0 V, I_{ON}=-10 mA Figure 3	2.5		7		Ω
		V_{SW}=1.8 V, I_{ON}=-10 mA Figure 3	2.5		15		Ω
I_{CC}	Quiescent Supply Current	V_{IN}=0 or V_{CC}, I_{OUT}=0	4.3			1	µA
I_{CCT}	Increase in I_{CC} Current Per Control Voltage and V_{CC}	V_{IN}=1.8 V	2.7			10	µA

Note:
3. Measured by the voltage drop between A and B pins at the indicated current through the switch. On resistance is determined by the lower of the voltage on the two (A or B ports).

AC Electrical Characteristics

All typical values are for V_{CC}=2.5 V at 25°C unless otherwise specified.

Symbol	Parameter	Conditions	V_{CC} (V)	T_A=- 40°C to +85°C			Units
				Min.	Typ.	Max.	
t_{on}	Turn-On Time, /OE to Output	R_L=50 Ω, C_L=5 pF V_{SW}=1.8 V Figure 4, Figure 5	2.3 to 3.6		15	34	ns
t_{uff}	Turn-Off Time, /OE to Output	R_L=50 Ω, C_L=5 pF V_{SW}=1.8 V Figure 4, Figure 5	2.3 to 3.6		12	25	ns
t_{ad}	Propagation Delay[4]	R_L=50 Ω, C_L=5 pF Figure 4, Figure 6	3.3		0.35		ns
O_{IRR}	Off Isolation	R_L=50 Ω, f=400 MHz Figure 11	2.3 to 3.6		-40		dB
Xtalk	Non-Adjacent Channel Crosstalk	R_L=50 Ω, f=100 MHz Figure 12	2.3 to 3.6		-40		dB
BW	-3dB Bandwidth	R_L=50 Ω, C_L=0 pF Figure 10	2.3 to 3.6		1000		MHz
		R_L=50 Ω, C_L=5 pF Figure 10			750		MHz

Note:
4. Guaranteed by characterization.

High-Speed-Related AC Electrical Characteristics

Symbol	Parameter	Conditions	V_{CC} (V)	T_A=- 40ºC to +85ºC			Units
				Min.	Typ.	Max.	
$t_{SK(O)}$	Channel-to-Channel Skew (5)	C_L=5 pF	3.3		40	80	ps
$t_{SK(P)}$	Skew of Opposite Transitions of the Same Output (5)	C_L=5 pF	3.3		15	40	ps
$t_{SK(PKG)}$	Package-to-Package Skew (5)	C_L=5 pF	3.3		60	100	ps

Note:

5. Guaranteed by characterization.

Capacitance

Symbol	Parameter	Conditions	T_A=- 40ºC to +85ºC			Units
			Min.	Typ.	Max.	
C_{IN}	Control Pin Input Capacitance	V_{CC}=0.2 V, f=1 MHz		2.0		pF
C_{ON}	D+/D- On Capacitance	V_{CC}=2.5 V, /OE=0 V, f=1 MHz Figure 9		6.0		
C_{OFF}	D1n, D2n Off Capacitance	V_{CC} and /OE=2.5 V, f=1 MHz Figure 8		2.5		

Test Diagrams

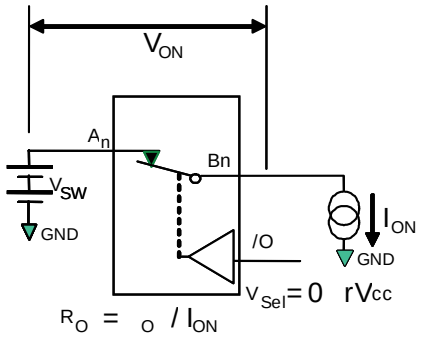
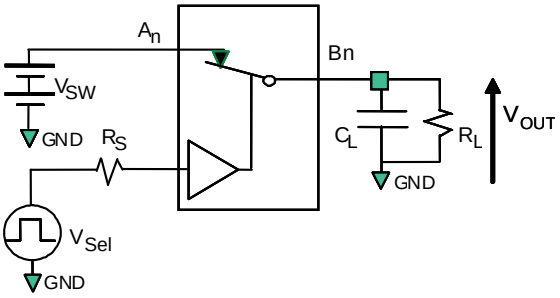


Figure 3. On Resistance



R_L, R_S, and C_L are functions of the application environment (see AC tables for specific values). C_L includes test fixture and stray capacitance.

Figure 4. AC Test Circuit Load

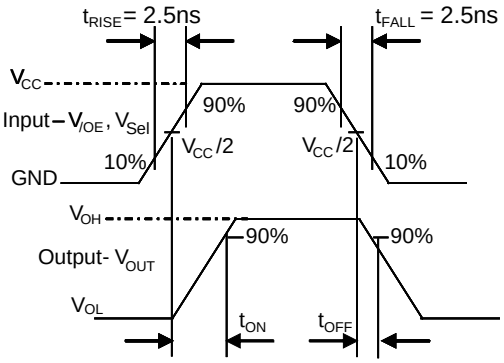


Figure 5. Turn-On / Turn-Off Waveforms

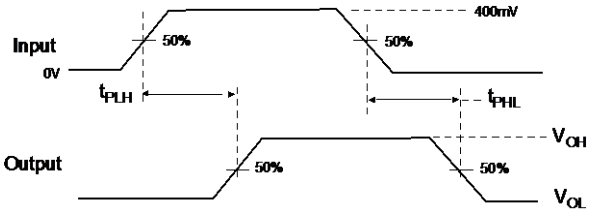


Figure 6. Propagation Delay (t_{ry} t_o – 500ps)

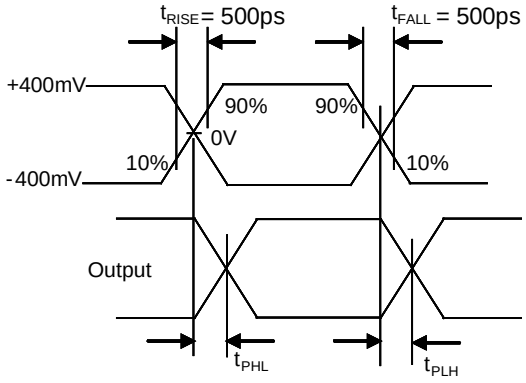


Figure 7. Intra-Pair Skew Test tSK(P)

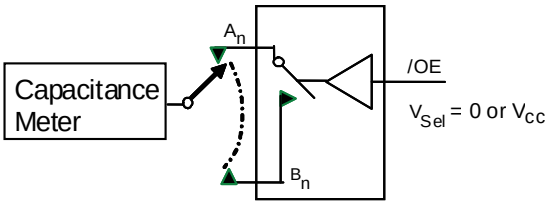


Figure 8. Channel Off Capacitance

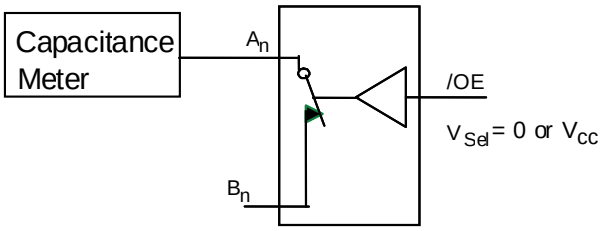
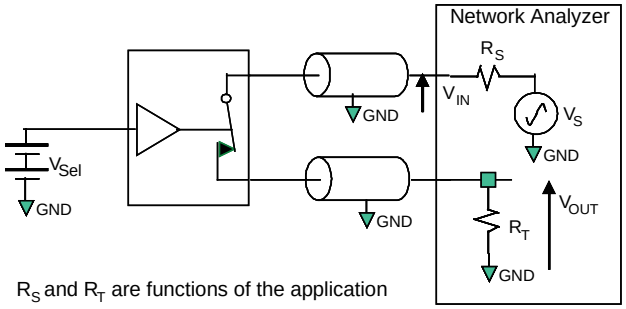


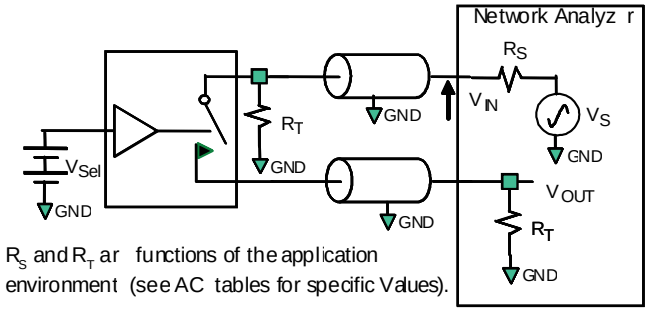
Figure 9. Channel On Capacitance

Test Diagrams (Continued)



R_S and R_T are functions of the application environment (see AC Tables for specific values).

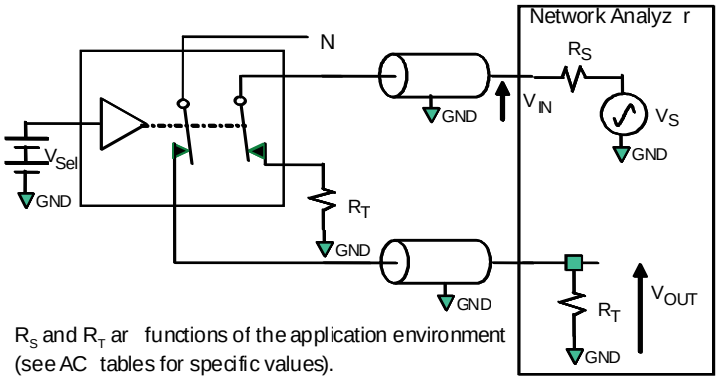
Figure 10. Bandwidth



R_S and R_T ar functions of the application environment (see AC tables for specific Values).

Off isolation = 20 Log (V_{OUT}/ V_{IN})

Figure 11. Channel Off Isolation

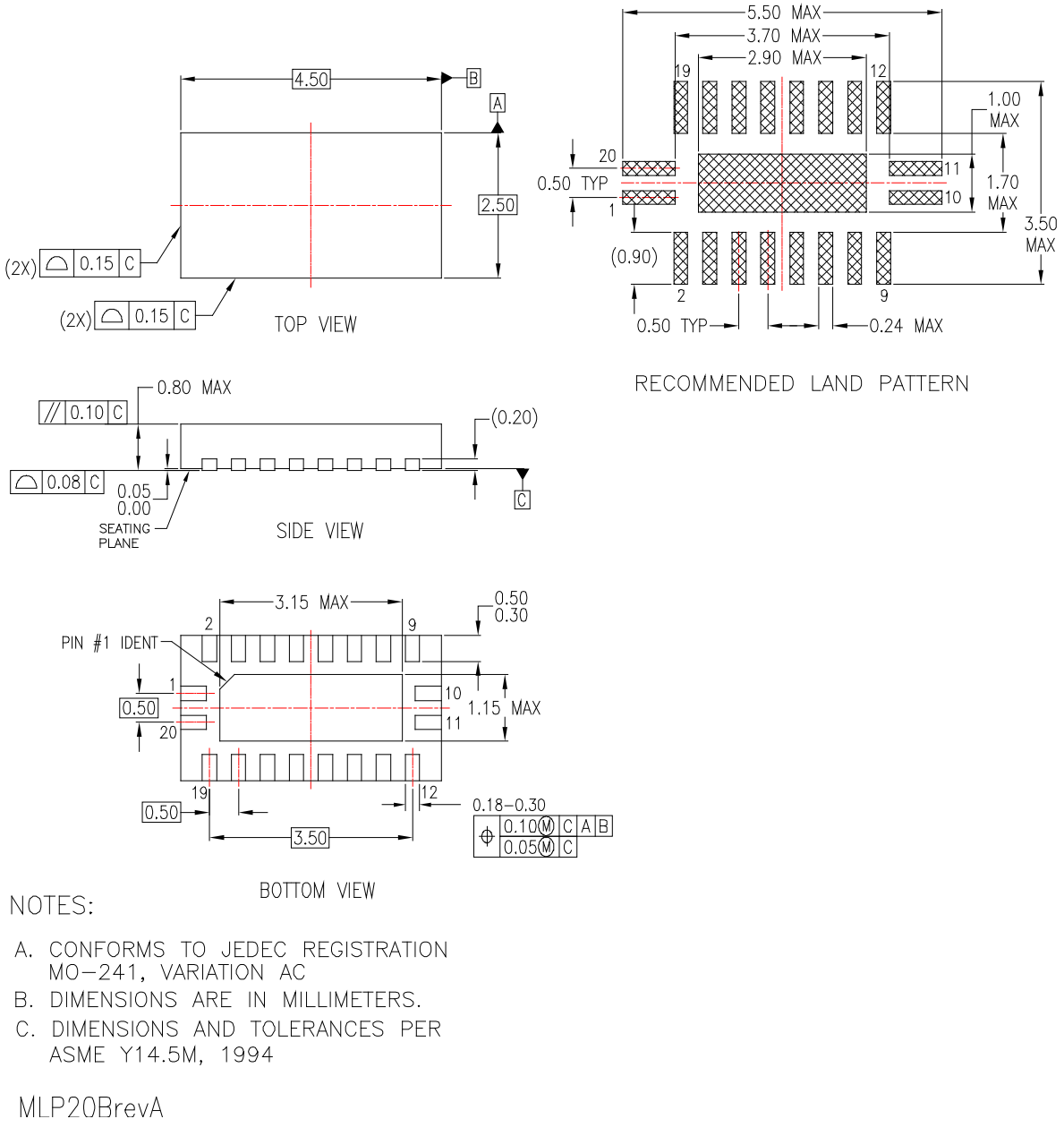


R_S and R_T ar functions of the application environment (see AC tables for specific values).

Crosstalk = 20 Log (V_{OUT} / V_{IN})

Figure 12. Non-Adjacent Channel-to-Channel Crosstalk

Physical Dimensions



NOTES:

A. CONFORMS TO JEDEC REGISTRATION MO–241, VARIATION AC
B. DIMENSIONS ARE IN MILLIMETERS.
C. DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994

MLP20BrevA

Figure 13. 20-Lead, Molded Leadless Package (MLP)

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