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August 2009

# FSA2367 — Low $R_{ON}$ (0.75 $\Omega$ ) Triple-SPDT, Negative-Swing Audio Source Switch

#### **Features**

- 10μA Maximum I<sub>CCT</sub> Current Over Expanded Control Voltage Range (V<sub>IN</sub>=2.6V, V<sub>CC</sub>=4.3V)
- On Capacitance 55pF Typical (C<sub>ON</sub>)
- 0.75Ω Typical On Resistance (R<sub>ON</sub>)
- Common Ports 1A, 2A, 3A with Negative Swing Audio to -2V
- -3db Bandwidth: >150 MHz
- Low Power Consumption (1µA Maximum)
- Power-Off Feature for 1A/2A/3A Pin (I<sub>IN</sub> < 2µA)</p>
- Packaged in Pb-Free 14-Pin TSSOP and DQFN

## **Applications**

- Cell Phone, PDA, Digital Camera, and Notebook
- LCD Monitor, TV, and Set-Top Box

#### Description

The FSA2367 is a triple Single-Pole Double-Throw (SPDT) switch that multiplexes three sources of data or audio under independent control pins. The FSA2367 has special circuitry on the 1A, 2A, 3A pins that allows a power-off feature. With the  $V_{\rm CC}$  supply removed and a voltage on the 1A/2A/3A pins, there is minimal leakage current into the 1A/2A/3A data pins. In addition, the FSA2367 also features very low quiescent current to extend battery life. The low quiescent current allows mobile handset applications direct interface with the baseband processor general-purpose I/Os. Typical applications involve switching in portables and consumer applications such as cell phones, digital cameras, and notebooks with hubs or controllers.

#### **IMPORTANT NOTE:**

For additional information, please contact <a href="mailto:analogswitch@fairchildsemi.com">analogswitch@fairchildsemi.com</a>.

## **Ordering Information**

Part Number	Top Mark	Top Mark  Eco Status Package			
FSA2367BQX	2367	Green	14-Terminal Depopulated very thin Quad Flat-pack No leads (DQFN) 2.5 x 3.0mm, JEDEC MO-241		
FSA2367MTCX	FSA2367	RoHS	14-Lead Thin Shrink Small Outline Package (TSSOP), 4.4mm Wide, JEDEC MO-153		

For Fairchild's definition of Eco Status, please visit: http://www.fairchildsemi.com/company/green/rohs\_green.html.

## **Analog Symbol**

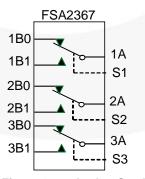


Figure 1. Analog Symbol

## **Pin Assignments**

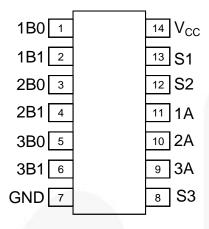


Figure 2. Pin Assignment TSSOP-14 (Top View)

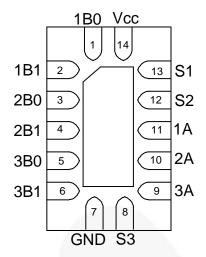


Figure 3. Pad Assignment DQFN-14 (Top View)

## **Pin Descriptions**

Pin Name	Description
S1, S2, S3	Switch Control Selects
1A, 2A, 3A	A Data Bus (Common)
1Bn, 2Bn, 3Bn	Multiplexed Source inputs

#### **Truth Table**

S1, S2, S3	Function
LOW	1B0=1A; 2B0=2A; 3B0=3A
HIGH	1B1=1A; 2B1=2A; 3B1=3A

#### **Absolute Maximum Ratings**

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Parameter	Conditions	Min.	Max.	Unit
V <sub>CC</sub>	Supply Voltages		-0.5	6.0	V
	Switch I/O Voltage <sup>(1)</sup>	1Bn, 2Bn Pins	V <sub>CC</sub> -5.5V	V <sub>CC</sub> -0.3V	V
$V_{SW}$	Switch i/O voltage	1A, 2A Pins	V <sub>CC</sub> -5.5V	V <sub>CC</sub> -0.3V	V
V <sub>CNTRL</sub>	Control Input Voltage <sup>(1)</sup>	S0, S1	-0.5	6.0	V
	Input Clamp Diode Current		-50		mA
	Switch I/O Current	Continuous		350	mA
	Peak Switch Current	Pulsed at 1ms duration, <10% Duty Cycl	Э	500	mA
0	Dower Dissipation at 950C	DQFN14 package		2.5	μW
P <sub>D</sub>	Power Dissipation at 85°C	TSSOP14 package		2.5	μW
T <sub>STG</sub>	Storage Temperature Range		-65	+150	°C
TJ	Maximum Junction Temperature			+150	°C
$T_L$	Lead Temperature	Soldering, 10 seconds	\	+260	°C
	Human Body Model (JEDEC: JESD22-A114)	All Pins		5500	kV
		I/O to GND		8000	
ESD	(0LDL0. 0L0D22-ATT+)	VCC to GND		8000	
	Charged Device Model (JEDEC-J	ESD22-C101)		2000	kV

#### Note:

1. Input and output negative ratings may be exceeded if input and output diode current ratings are observed.

## **Recommended Operating Conditions**

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to absolute maximum ratings.

Symbol	Parameter	Min.	Max.	Unit
V <sub>CC</sub>	Supply Voltages	2.7	4.3	V
V <sub>S0:S1</sub>	Control Input Voltage	0	V <sub>CC</sub>	V
V <sub>SW</sub>	Switch I/O Voltage	V <sub>CC</sub> -5.5	V <sub>CC</sub> -0.3	V
T <sub>A</sub>	Operating Temperature	-40	+85	°C
$\theta_{JA}$	Thermal Resistance (free air)		145	°C/W

### **DC Electrical Characteristics**

All typical values are at 25°C unless otherwise specified.

Cymbal	Danamatan	Conditions	V (\( \)	T <sub>A</sub> =- 40°C to +85°C			Hnit
Symbol	Parameter	Conditions	Vcc (V)	Min.	Тур.	Max.	Unit
	Analog Signal Range			Vcc- 5.5		Vcc	V
V <sub>IK</sub>	Clamp Diode Voltage	I <sub>IN</sub> =-18mA	3.0			-1.2	V
V <sub>IH</sub>	Input Voltage High		2.7 to 3.6	1.2			V
VIH	Input voltage riigii		3.6 to 4.3	1.5			v
V <sub>IL</sub>	Input Voltage Low		2.7 to 3.6			0.5	V
V IL	mput voltago zow		3.6 to 4.3			0.7	, v
I <sub>IN</sub>	Control Input Leakage	$V_{IN}$ =0 to $V_{cc}$	4.3			±1	μΑ
I <sub>OFF</sub>	Power-Off Leakage Current (Common Port Only 1A, 2A)	Common Port (1A, 2A), $V_{SW=}0$ to 4.3V, $V_{CC}=0$ V	0V			±10	μA
I <sub>NO(0FF)</sub>	Off-Leakage Current of Port 1Bn, 2Bn	1Bn, 2Bn=0.5V, V <sub>CC</sub> - 0.5V or Floating 1A, 2A=0.5V, V <sub>CC</sub> - 0.5V	4.3	-250	10	250	nA
		Figure 8					
I <sub>NC(0N)</sub>	On-Leakage Current of Port 1Bn, 2Bn	1Bn, 2Bn=Floating 1A, 2A=0.5V, V <sub>CC</sub> – 0.5V Figure 10	4.3	-250	10	250	nA
R <sub>ON</sub>	Switch On Resistance <sup>(2)</sup>	1Bn or 2Bn=0V, 0.7V, 2.0V,2.7V, I <sub>ON=</sub> -100m Figure 9	2.7		0.75	2.00	Ω
$\Delta R_{ON}$	Delta R <sub>ON</sub> <sup>(3)</sup>	1Bn or 2Bn=0.7V , I <sub>ON=</sub> -100mA	2.7		0.5		Ω
R <sub>FLAT(ON)</sub>	On Resistance Flatness <sup>(4)</sup>	1Bn or 2Bn=0V, 0.7V, 2.0V,2.7V, I <sub>ON=</sub> -100mA	2.7 to 4.3		0.23	0.40	Ω
I <sub>cc</sub>	Quiescent Supply Current	V <sub>SW=</sub> 0 or V <sub>CC</sub> , I <sub>OUT</sub> =0	4.3			500	nA
	Increase in I <sub>CC</sub> Current per	V <sub>CNTRL=</sub> 2.6V	4.3		2.2	10.0	^
I <sub>CCT</sub>	Control Voltage and V <sub>CC</sub>	V <sub>CNTRL=</sub> 1.8V	4.3		6.5	15.0	μA

#### Notes:

- 2. Measured by the voltage drop between the 1Bn (2Bn, 3Bn) and 1A (2A, 3A) pins at the indicated current through the switch. On resistance is determined by the lower voltage on the two.
- 3. Guaranteed by characterization; not tested in production.
- 4. Flatness is defined as the difference between minimum and maximum on resistance over the specified range.

## **AC Electrical Characteristics**

All typical values are for  $V_{\text{CC}}$ =3.3V at 25°C unless otherwise specified.

Coursels al	Danamatan	Canditions	V 00	T <sub>A</sub> =- 40°C to +85°C			Unit
Symbol	Parameter	Conditions	Vcc (V)	Min.	Тур.	Max.	
t <sub>ON</sub>	Turn-On Time, S to Output	$V_{Bn}$ =1.5V, $R_L$ =50 $\Omega$ , $C_L$ =35pF	2.7 to 4.3		45	60	ns
		Figure 10, Figure 12					
t <sub>OFF</sub>	Turn-Off Time, S to Output	$V_{Bn}$ =1.5V, $R_L$ =50 $\Omega$ , $C_L$ =35pF	2.7 to 4.3		25	45	ns
		Figure 10, Figure 12					
	Propagation Delay <sup>(5)</sup>	$R_L=50\Omega$ , $C_L=5pF$	2.2		0.25		ns
t <sub>PD</sub>	Propagation Delay	Figure 10, Figure 13	3.3				
t <sub>BBM</sub>	Break-Before-Make <sup>(5)</sup>	$R_L$ =50 $\Omega$ , $C_L$ =35pF $V_{IN1}$ = $V_{IN2}$ = $V_{IN3}$ =1.5V	2.7 to 4.3	1	6		ns
		Figure 11					
Q	Charge Injection	$\begin{array}{l} R_{\text{GEN=}}0\Omega,C_{\text{L}}\text{=}100\text{pF},\\ R_{\text{L}}\text{=}\text{OPEN};V_{\text{GEN=}}0V \end{array}$	2.7 to 4.3		9		рС
		Figure 14					
O <sub>IRR</sub>	Off-Isolation	f=100 kHz, $R_L$ =50 $\Omega$	2.7 to 4.3		-70	A.	dB
OIRR	On-isolation	Figure 4, Figure 16	2.7 10 4.3				
Xtalk	Non-Adjacent Channel	f=100 kHz, $R_L$ =50 $\Omega$	2.7 to 4.3		-100		dB
Alain	Crosstalk	Figure 5, Figure 17	2.7 10 4.3		-100		ub
THD	Total Harmonic Distortion	$R_L$ =600 $\Omega$ , $V_{SW=}$ 0.5 $V_{pp}$ , f=20 Hz to 20kHz	2.7 to 4.3		0.01		%
		Figure 20					
DW	Odle le que dividable	$R_L=50\Omega$ , $C_L=0$ , $5pF$	0.71.40		450		N 41 1-
BW	-3db bandwidth	Figure 6, Figure 15	2.7 to 4.3		150		MHz

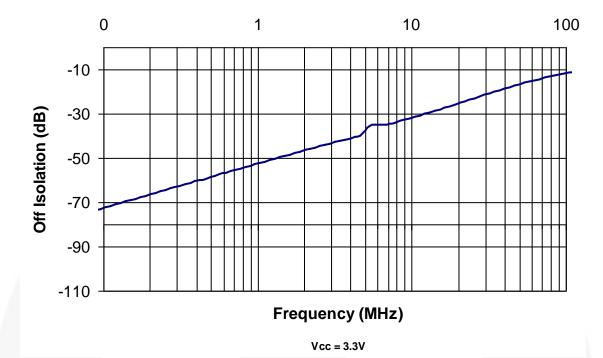
#### Note:

5. Guaranteed by characterization; not tested in production.

## Capacitance

Cumbal	Doromotor	Conditions	T <sub>A</sub> =- 40°C to +85°C			Unit
Symbol	Parameter	Conditions	Min.	Тур.	Max.	Onit
C <sub>IN</sub>	Control Pin Input Capacitance	V <sub>CC</sub> =0V		2.5		
C <sub>ON</sub>	A/B On Capacitance	V <sub>CC</sub> =3.3, f=1MHz Figure 19			55	pF
C <sub>OFFB</sub>	Port 1Bn, 2Bn,3Bn Off Capacitance	V <sub>CC</sub> =3.3, f=1MHz Figure 18			16	3/
C <sub>OFFA</sub>	Port 1A, 2A,3A Off Capacitance	V <sub>CC</sub> =3.3, f=1MHz Figure 18			20	

## **Typical Performance Characteristics**



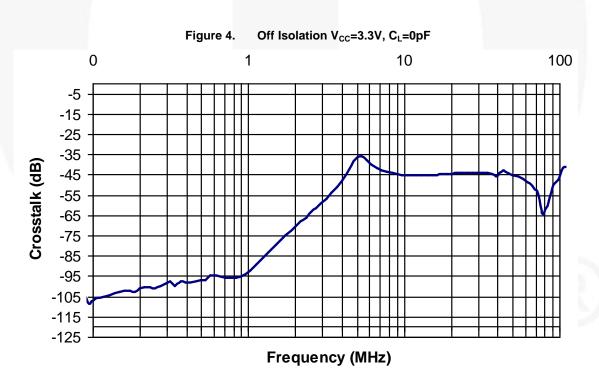


Figure 5. Non-Adjacent Crosstalk V<sub>CC</sub>=3.3, C<sub>L</sub>=0pF

## **Typical Performance Characteristics** (Continued)

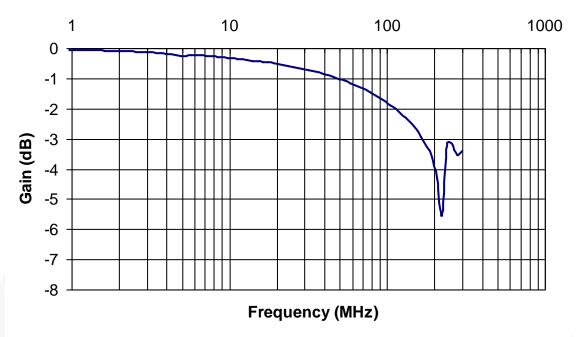


Figure 6. Bandwidth Characterization, Frequency Response at V<sub>CC</sub>=3.3V, C<sub>L</sub>=0pF

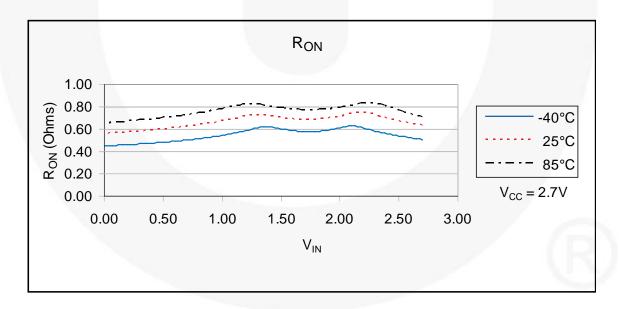


Figure 7. On Resistance

## **Test Diagrams**

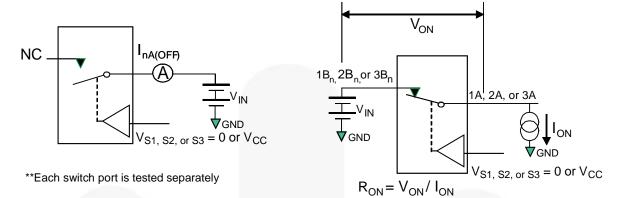
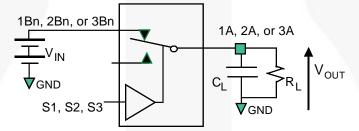


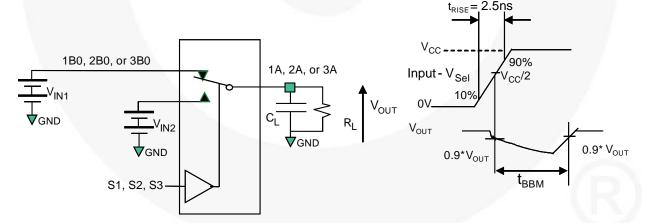
Figure 8. Off Leakage

Figure 9. On Resistance



 $R_L$  and  $C_L$  are functions of the application environment (see AC Tables for specific values)  $C_L$  includes test fixture and stray capacitance

Figure 10. AC Test Circuit Load



 $R_L$  and  $C_L$  are functions of the application environment (see AC Tables for specific values)  $C_L$  includes test fixture and stray capacitance

Figure 11. Break-Before-Make Interval Timing

## Test Diagrams (Continued)

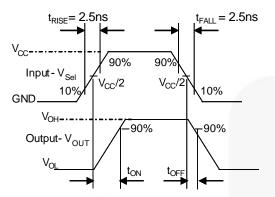


Figure 12. Turn-On / Turn-Off Waveforms

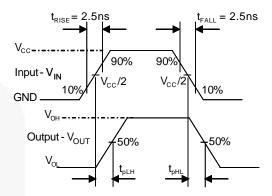


Figure 13. Switch Propagation Delay Waveforms

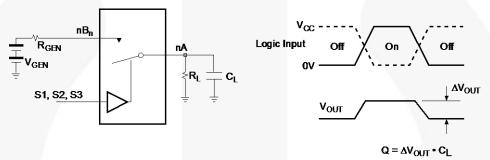


Figure 14. Charge Injection Test (Q=ΔV<sub>OUT</sub> \* C<sub>L</sub>)

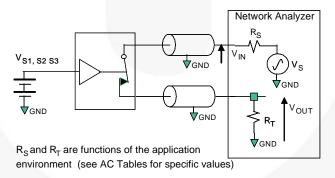


Figure 15. Bandwidth

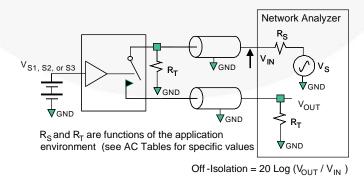


Figure 16. Channel Off Isolation

#### Test Diagrams (Continued)

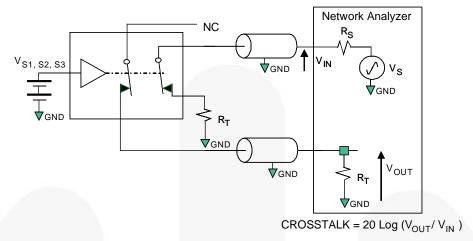


Figure 17. Non-Adjacent Channel-to-Channel Crosstalk

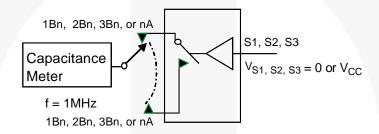


Figure 18. Channel Off Capacitance

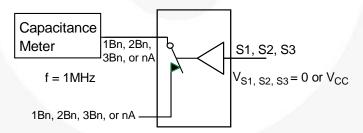


Figure 19. Channel On Capacitance

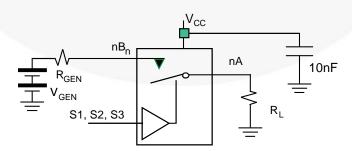
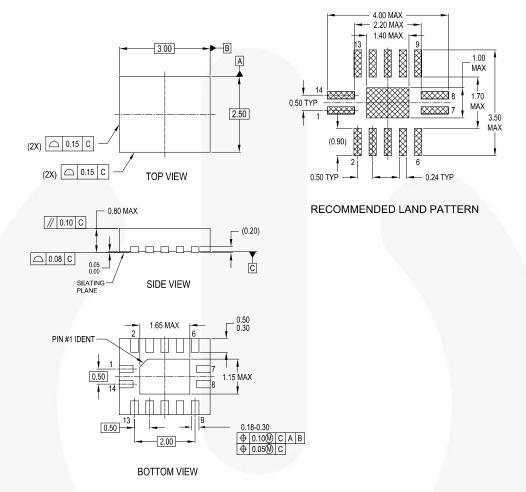


Figure 20. Total Harmonic Distortion

## **Physical Dimensions**



#### NOTES:

- A. CONFORMS TO JEDEC REGISTRATION MO-241, VARIATION AA
- B. DIMENSIONS ARE IN MILLIMETERS
- C. DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994

#### MLP14ArevA

#### Figure 21. 14-Terminal Depopulated very thin Quad Flat-pack No leads (DQFN)

Package drawings are provided as a service to customers considering Fairchild components. Drawings may change in any manner without notice. Please note the revision and/or date on the drawing and contact a Fairchild Semiconductor representative to verify or obtain the most recent revision. Package specifications do not expand the terms of Fairchild's worldwide terms and conditions, specifically the warranty therein, which covers Fairchild products.

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## Physical Dimensions (Continued)

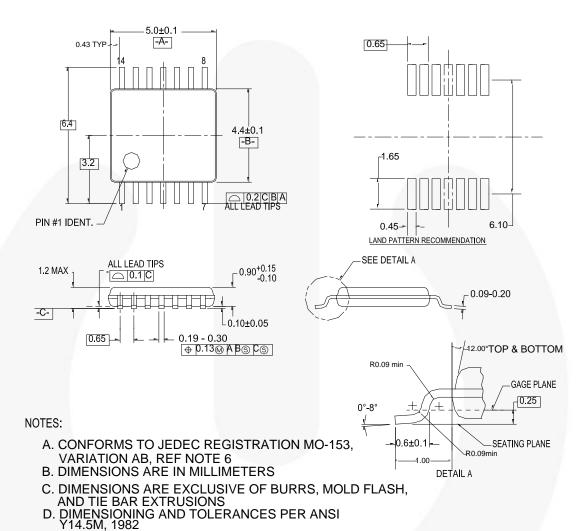


Figure 22. 4-Lead Thin Shrink Small Outline Package (TSSOP)

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E. LANDPATTERN STANDARD: SOP65P640X110-14M

F. DRAWING FILE NAME: MTC14REV6





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#### Definition of Terms

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Preliminary	First Production	Datasheet contains preliminary data; supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve design.		
		Datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve the design.		
Obsolete	Not In Production	Datasheet contains specifications on a product that is discontinued by Fairchild Semiconductor. The datasheet is for reference information only.		

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