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FAIRCHILD SEMICONDUCTOR®

July 2012

FSA806 — USB2.0 High-Speed (480Mbps), UART, and Audio Switch with Negative Signal Capability

Features

- 3:1 Switch Handles:
  - Audio Headsets
  - UART
  - Up to Two High- and Low-Speed USB Data
- Negative-Swing-Capable Audio Channel
- Built-in Termination Resistors for Audio Pop Reduction
- Simple Switch Control Using Two Select Pins

Applications

- Cell Phones, MP3 Players, PDAs

Description

The FSA806 is a 3:1 USB accessory switch that enables USB data, stereo and mono audio, and UART data to share a common connector port. Two ports are designed for high-speed USB 2.0 signaling, while also capable of full speed USB and UART communication. The architecture is designed to allow audio signals to swing below ground so a common USB and headphone jack can be used for personal media players and portable peripheral devices.

The FSA806 meets both USB Rev. 2.0 and micro-USB specifications.

Ordering Information

Part Number	Operating Temperature Range	Top Mark	Package
FSA806UMX	-40 to +85°C	KN	12-Lead Quad, 1.8 x 1.8mm Ultrathin Molded Leadless Package (UMLP)

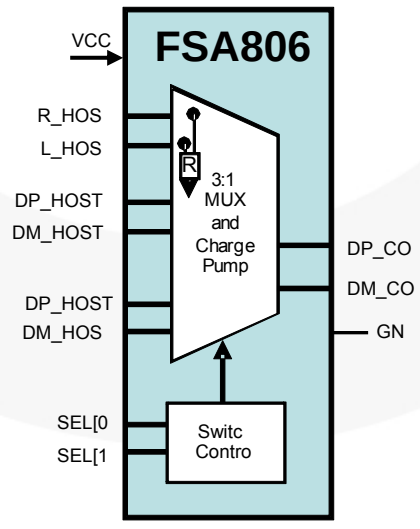


Figure 1. Functional Block Diagram

Application Diagram

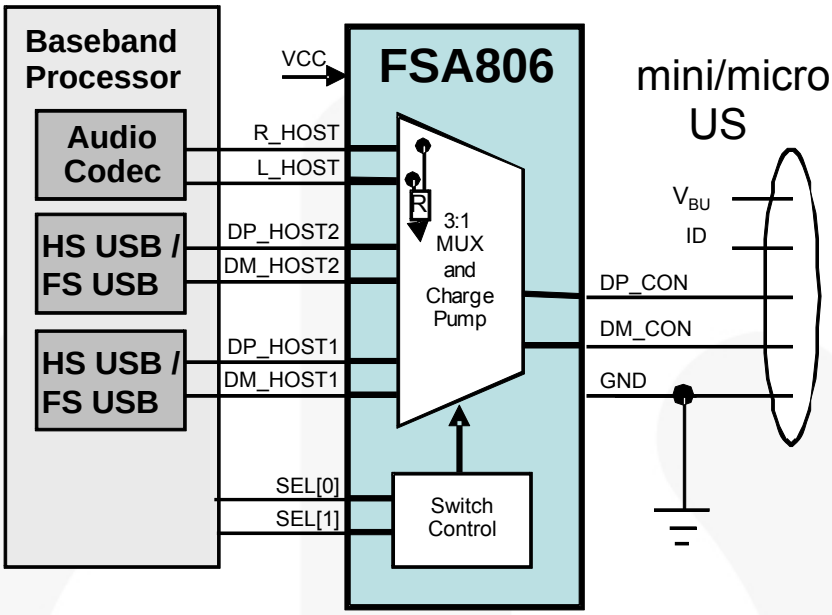


Figure 2. Typical Application

Functional Description

The FSA806 USB2.0 accessory switch is designed to consolidate wired accessories for portable devices, such as cellular telephones and portable audio players. The benefits of consolidation include reduced space requirements from a reduction of connectors and their size. The micro-USB connector, for example, reduces connector height and depth, allowing for slimmer overall designs. Using the USB industry standard and a common connector type, for accessories such as chargers and headsets, greatly reduces the waste associated with new phone purchases by allowing re-use of the accessories.

Using just five wires for all connection types considerably reduces the cost of wired accessories and simplifies their construction. The FSA806 facilitates adopting this methodology because it is designed to redirect the DP/DM pins from the USB connector to one of three ports at the baseband's discretion.

Applications with Multiple USB Controllers

When operating with two USB controllers, it is recommended to configure the switches to OPEN before switching to the other (second) USB interface. The OPEN setting duration should be long enough for the accessory to go to a SE0 state, when the switch is set to the other (second) USB port, the new controller re-enumerates.

Mode Descriptions

The FSA806 select pins control the switching operations, SEL[0] and SEL[1] described in Table 1

Table 1. Selection Truth Table

SEL[1]	SEL[0]	Switch Action	Description
0	0	OPEN	Open all switch paths (device in low-power mode)
0	1	USB1, UART	Closes USB1 path to D+/D-, default condition(1) - DP_CON connected to DP_HOST1 - DM_CON connected to DM_HOST1
1	0	USB2, UART	Closes USB2 path to D+/D- - DP_CON connected to DP_HOST2 - DM_CON connected to DM_HOST2
1	1	AUDIO	Closes audio path to D+/D- only - DP_CON connected to R_HOST - DM_CON connected to L_HOST

Notes:

1. The SELECT pins are CMOS inputs and should not be left in a floating condition. Some applications require a UART path be in the CLOSED position on power-up for initial programming of the device under test. If that condition is desired, the two SELECT pins should be pulled to the correct levels with external resistors that should exceed 100KΩ to reduce the static power consumption. In other applications, adding weak pull-down resistors to GND defaults the device to all paths open (low-power mode).
2. When the audio switch is in the OPEN position, the R and L are terminated to GND with internal termination resistors to discharge any stray capacitance that could cause audio pop.

Pin Configuration

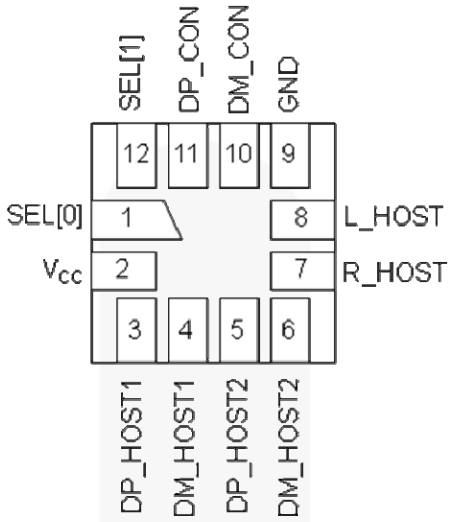


Figure 3. 12-Pin, UMLP Pin Assignments (Top-Through View)

Pin Descriptions

Name	Pin #	Description
USB, UART Interface		
DP_HOST1	3	D+ signal, dedicated USB port to be connected to the resident USB or UART transceiver on the phone.
DM_HOST1	4	D- signal, dedicated USB port to be connected to the resident USB or UART transceiver on the phone.
DP_HOST2	5	D+ signal, dedicated USB port to be connected to the resident USB or UART transceiver on the phone.
DM_HOST2	6	D- signal, dedicated USB port to be connected to the resident USB or UART transceiver on the phone.
Audio Interface		
R_HOST	7	Right audio channel from phone audio codec.
L_HOST	8	Left audio channel from phone audio codec.
Power Interface		
V_{CC}	2	Input voltage supply pin to be connected to the phone battery output.
Connector Interface		
GND	9	Ground
DP_CON	11	Connected to the USB connector D+ pin; depending on the FSA806 signaling mode, this pin can share DP_HOST1, DP_HOST2 or R_HOST signals.
DM_CON	10	Connected to the USB connector D- pin; depending on the FSA806 signaling mode, this pin can share DM_HOST1, DM_HOST2 or L_HOST signals.
Switch Control		
SEL[1:0]	12, 1	Switch selection pins; *refer to Table 1 for truth table.*

Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Parameter			Min.	Max.	Unit
V_{CC}	Supply Voltage from Battery / Baseband			-0.5	6.0	V
V_{SW}	Switch I/O Voltage	USB		-0.5	V_{BUS}+0.5	V
		Stereo/Mono Audio Path Active		Vcc-8.5	V_{CC} +0.5	
		All Other Channels		-0.5	V_{CC} +0.5	
I_{IK}	Input Clamp Diode Current			-50		mA
I_{SW}	Switch I/O Current (Continuous)	USB			50	mA
		Audio			60	
		All Other Channels			50	
I_{SWPEAK}	Peak Switch Current (Pulsed at 1ms Duration, <10% Duty Cycle)	USB			150	mA
		Audio			150	mA
		All Other Channels			150	mA
T_{STG}	Storage Temperature Range			-65	+150	°C
T_J	Maximum Junction Temperature				+150	°C
T_L	Lead Temperature (Soldering, 10 Seconds)				+260	°C
ESD	IEC 61000-4-2 System	USB Connector Pins (D+, D-, V_{BUS})	Air Gap		15	kV
			Contact		8	
	Human Body Model, JEDEC JESD22-A114		All Pins		3	
	Charged Device Model, JEDEC JESD22-C101		All Pins		2	

Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to Absolute Maximum Ratings.

Symbol	Parameter		Min.	Max.	Unit
V_{CC}	Battery Supply Voltage		2.7	4.4	V
V_{SW}	Switch I/O Voltage	USB/UART Path Active	0	4.4	V
		Audio Path Active	V_{CC}-7	2.0	V
T_A	Operating Temperature		-40	+85	ºC

Switch Path DC Electrical Characteristics

All typical values are at 25ºC unless otherwise specified.

Symbol	Parameter	V_{CC} (V)	Conditions	T_A = -40 to +85°C			Unit
				Min.	Typ.	Max.	
Host Interface Pins (SEL[2:0])							
V_{IH}	Input High Voltage	3.2 to 4.4		1.3			V
V_{IL}	Input Low Voltage	3.2 to 4.4				0.7	V
I_{IN}	Control Input Leakage	0 to 4.4	V_{SW}=0 to V_{CC}	-1		1	µA
I_{OZ}	Off-State Leakage	4.4	0 ≤ DP_CON, DM_CON, DP_HOSTn, DM_HOSTn, R_HOST, L_HOST ≤ 3.6V	-2		2	µA
Switch Off Characteristics							
I_{OFF}	Power-Off Leakage Current	0	All Ports Except MIC & Audio path V_{SW}=0V to 4.4V, Figure 8			10	µA
USB Switch On Paths							
R_{ONUSB}	HS USB Range Switch On Resistance	3.2 to 4.4	V_{DP_CON/DM_CON}=0V, 0.4V, I_{ON}=8mA, Figure 7		6	9	Ω
R_{ONUART}	UART Range Switch On Resistance	3.2 to 4.4	V_{DP_CON/DM_CON} =0V, 3.2V, I_{ON}=8mA, Figure 7		8		Ω
Audio R/L Switch On Paths							
R_{ONAUD}	Audio Switch On Resistance	3.2 to 4.4	$V_{L/R}$=-0.8V, 0.8V, I_{ON}=30mA, Figure 7			3	Ω
R_{FLAT}	Audio R_{ON} Flatness(1)	3.8			0.16		Ω
R_{TERM}	Internal Termination Resistors				1		kΩ
Total Switch Current Consumption							
I_{CCSL}	Battery Supply Sleep Mode Average Current	3.2 to 4.4	Static Current During Sleep Mode (SEL[2:0]=0)			1	µA
I_{CCWK}	Battery Supply Active Mode Average Current	3.2 to 4.4	USB/UART Mode		20	35	µA
			Audio Mode			1	µA
I_{CCSELT}	Increase in I_{CCSL}/I_{CCWK} Current per Control Voltage and V_{CC}	3.2 to 4.4	V_{SEL}=2.8V and V_{CC}=4.4V			8	µA
			V_{SEL}=1.8V and V_{CC}=4.4V			10	µA

Note:

3. Flatness is defined as the difference between the maximum and minimum values of on resistance over the specified range of conditions.

Switch Path AC Electrical Characteristics[4]

All typical value are for V_{CC} =3.8V at 25ºC unless otherwise specified.

Symbol	Parameter		V_{CC} (V)	Conditions	TA = -40 to +85°C			Unit	Figure
					Min.	Typ.	Max.		
Xtalk	Active Channel Crosstalk DP_CON to DM_CON	Audio Mode	3.8	f=20kHz, R_T=32Ω, C_L=0pF		-95		dB	Figure 10
		USB Mode	3.8	f=1MHz, R_T=50Ω, C_L=0pF		-75			
				f=240MHz, R_T=50Ω, C_L=0pF		-36			
O_{IRR}	Off Isolation Rejection Ratio	Audio Rejection L_HOST to DM_CON, R_HOST to DP_CON	3.8	f=20kHz, R_T=32Ω, C_L=0pF		-100		dB	Figure 9
		USB Rejection DM_HOST to DM_CON, DP_HOST to DP_CON	3.8	f=1 MHz, R_T=50Ω, C_L=0pF		-85			
				f=240MHz, R_T=50Ω, C_L=0pF		-35			
THD+N	Total Harmonic Distortion + Noise (Audio Path)		3.8	20Hz to 20kHz, R_L=16Ω, Input Signal Range 1.6V_{PP}		0.10		%	Figure 14
				20Hz to 20kHz, R_L=32Ω, Input Signal Range 1.6V_{PP}		0.07		%	Figure 14

Note:

4. Guaranteed by characterization; not production tested.

Capacitance

Symbol	Parameter	V_{CC} (V)	Conditions	T_A = -40 to +85°C			Unit	Figure
				Min.	Typ.	Max.		
C_{IN}	Select Pins Capacitance[5]	0	V_{BIAS}=0.2V		2.5		pF	Figure 12
$C_{OFF(D+, D-)}$	D+, D- On Capacitance (HS USB Mode)[5]	3.8	V_{BIAS}=0.2V, f=1MHz		4.0		pF	Figure 12
$C_{ON(D+, D-)}$	D+, D- On Capacitance (HS USB Mode)[5]	3.8	V_{BIAS}=0.2V, f=1MHz		6.8		pF	Figure 13

Note:

5. Guaranteed by characterization; not production tested.

High-Speed USB Eye Compliance Results

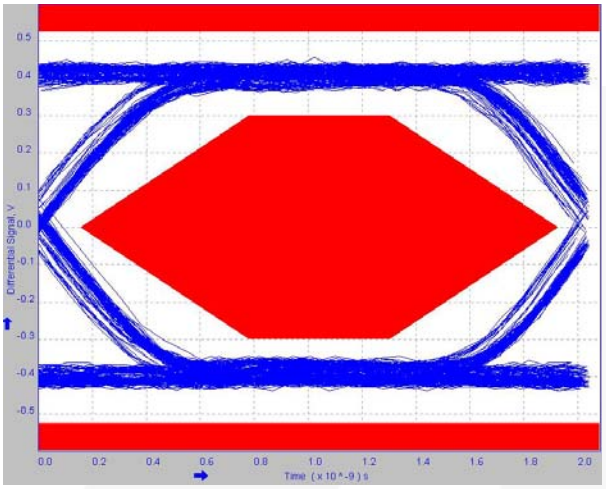


Figure 4. High-Speed Test Results (DP_CON/DM_CON – DP_HOST1/DM_HOST1)

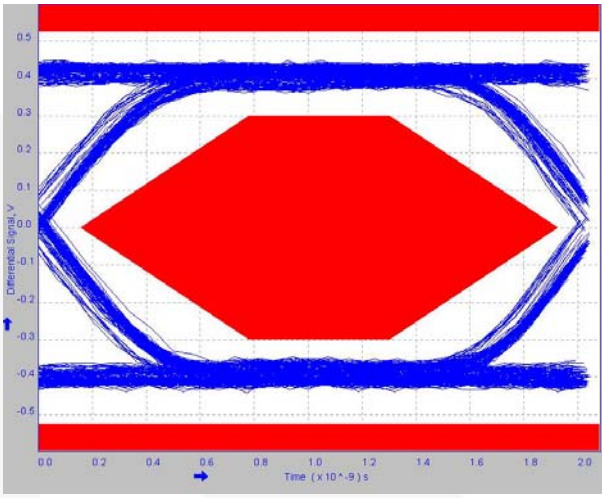


Figure 5. High-Speed Test Results (DP_CON/DM_CON – DP_HOST2/DM_HOST2)

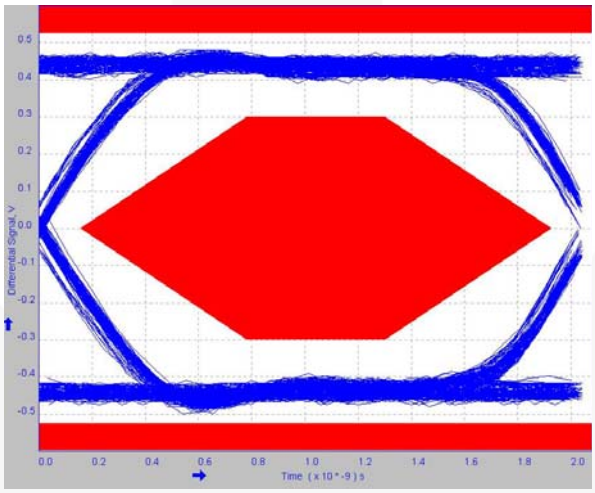


Figure 6. High-Speed Eye Compliance Input Signal

Test Diagrams

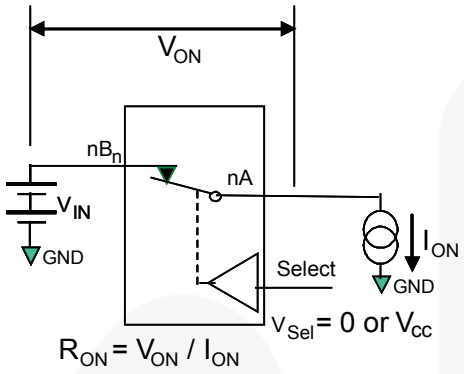


Figure 7. On Resistance

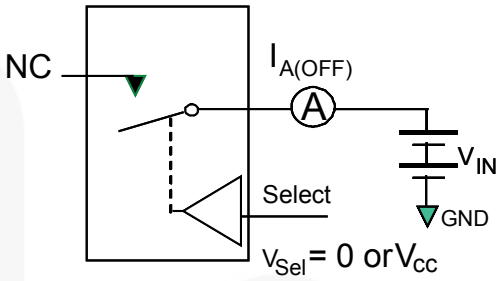


Figure 8. Off Leakage

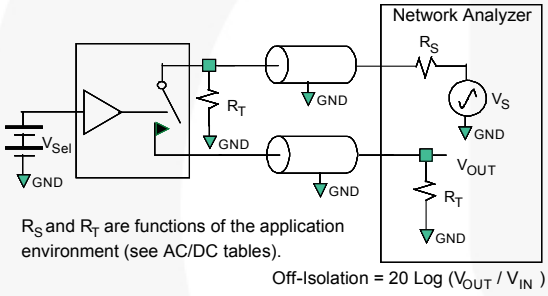


Figure 9. Channel Off Isolation

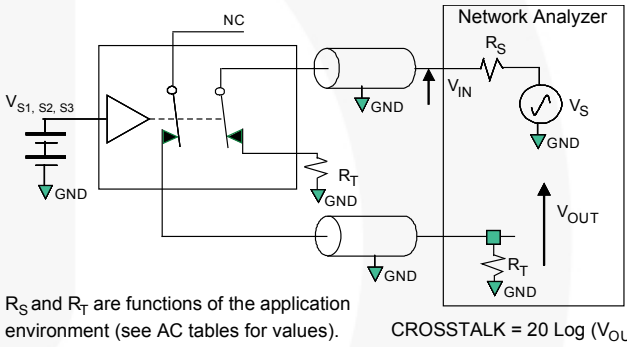
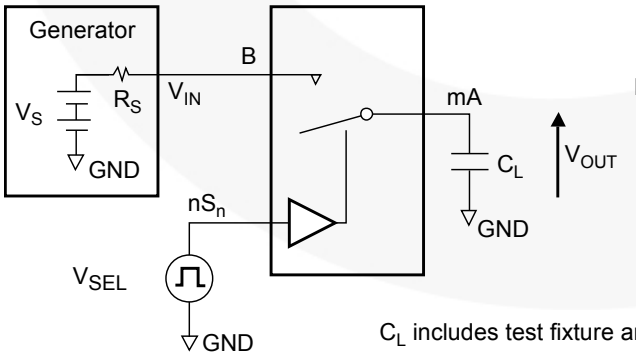


Figure 10. Active Channel Crosstalk



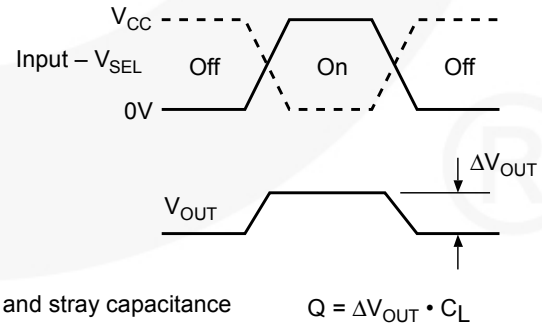


Figure 11. Charge Injection Test

Test Diagrams (Continued)

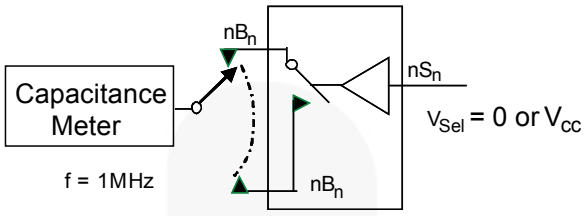


Figure 12. Channel Off Capacitance

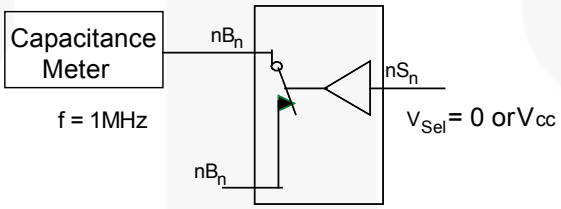
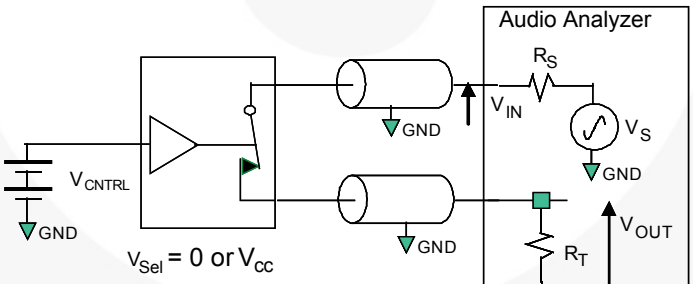


Figure 13. Channel On Capacitance



R_S and R_T are functions of the application environment (see AC Tables for specific values).

Figure 14. Total Harmonic Distortion + Noise

Physical Dimensions

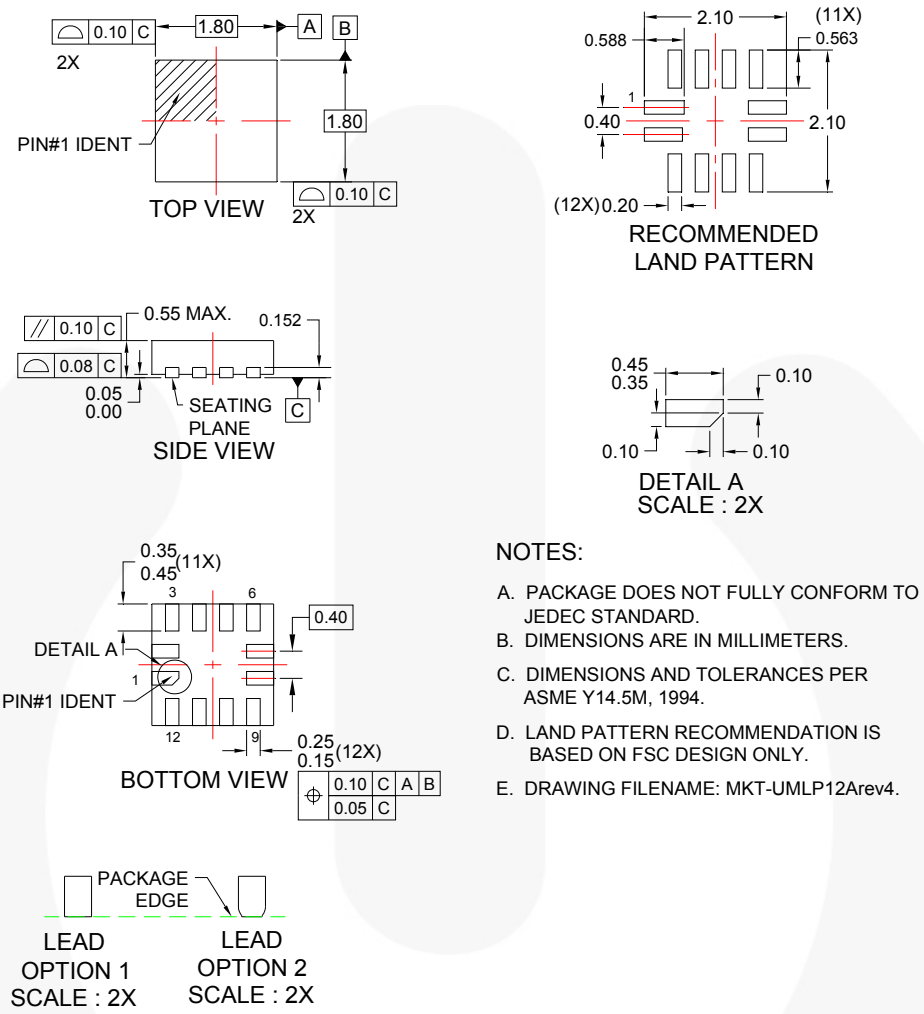


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Figure 15. 12-Lead, Ultrathin Molded Leadless Package (UMLP)

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Rev. I62

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