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September 2014

FSA9591 — USB Accessory Detection Switch with Integrated Linear Battery Charger

Features

- Detection:
  - USB Data Cable
  - UART Serial Link
  - Charger Detection (CDP, DCP)
  - Factory-Mode Cables
  - Teletype (TTY) Converter
- Linear Charger with up to 950 mA Charging Current Full-Speed and High-Speed 2.0 Compliant
- Automatic Switching with Available Interrupt
- UART: RxD & TxD
- USB: FS and HS 2.0 Compliant
- Switch Type: USB, UART

Description

The FSA9591 is a USB accessory detection switch with an integrated lithium ion (Li+) linear battery charger. The FSA9591 is capable of detecting factory test modes, car kit type 1 and travel adapter charger, USB data port, and USB chargers. Compliant with the USB battery charging rev. 1.1 specification, the FSA9591 can detect USB Standard Downstream Ports (SDP), Dedicated Charging Ports (DCP), and Charging Downstream Ports (CDP).

The integrated linear charger uses constant current, constant voltage, and thermal control loops to charge Li+ batteries and provide protection. The FSA9591 also includes two programmable LDOs, capable of supplying 300mA each, for powering other devices in mobile phones. Battery presence detection via DETBAT_N and charging current sensing through VICHG are also provided. V_{BUS_IN} pin can tolerate up to 28 V.

Applications

- Cell Phones, Smart Phones, PDAs
- Tablets, Portable Media Players
- Gaming Devices, Digital Cameras

Ordering Information

Part Number	Operating Temperature Range	Top Mark	Package
FSA9591UCX (1)	-40 to +85°C	NT	30-Lead WLCSP (2.38 mm x 1.98 mm x 0.625 mm, 0.4 mm Pitch)

Note:

1. Includes backside lamination.

Typical Application

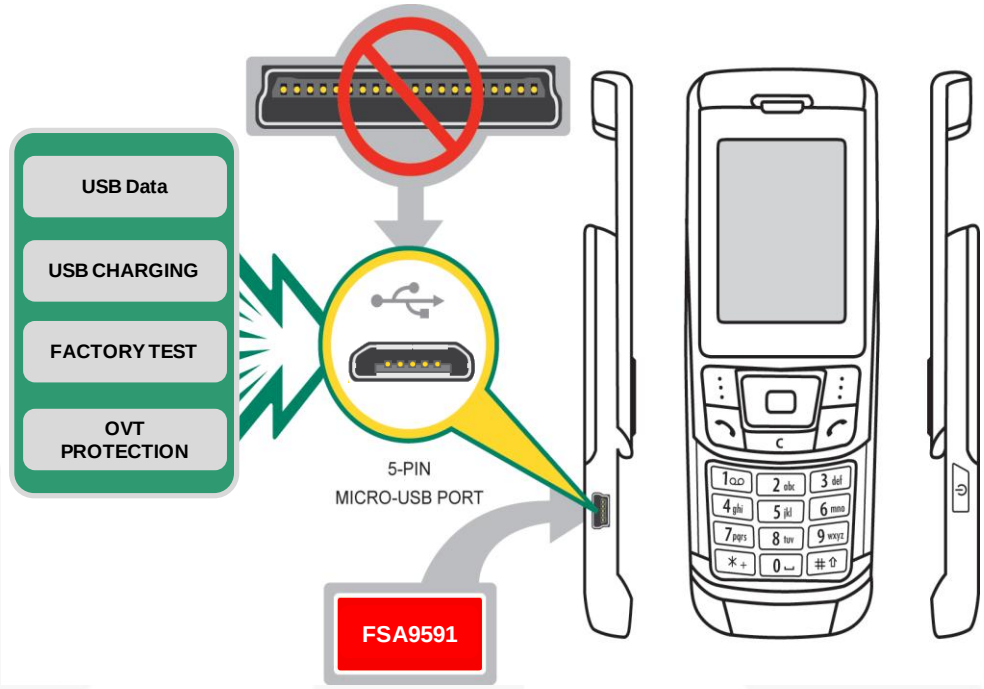


Figure 1. Mobile Phone Example

Block Diagram

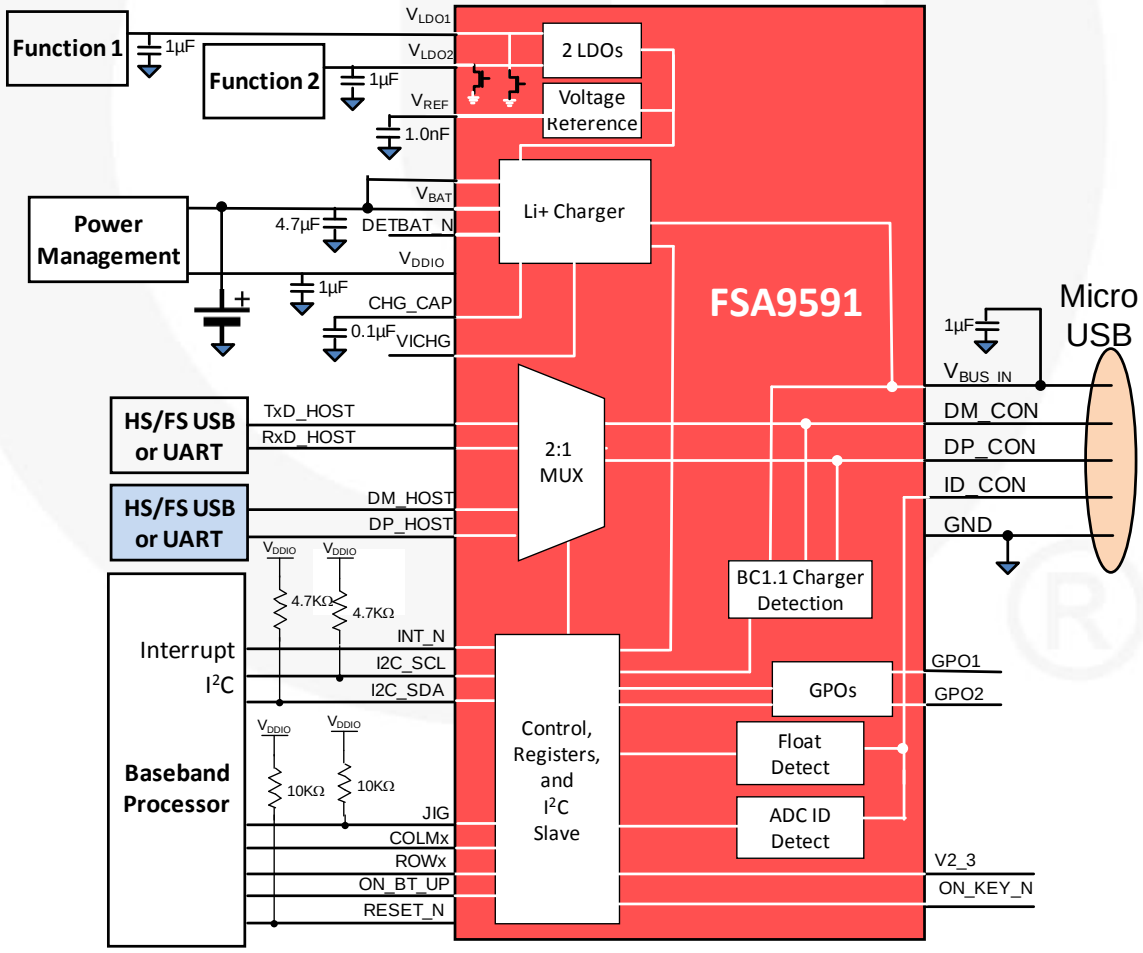


Figure 2. Block Diagram

Pin Configuration

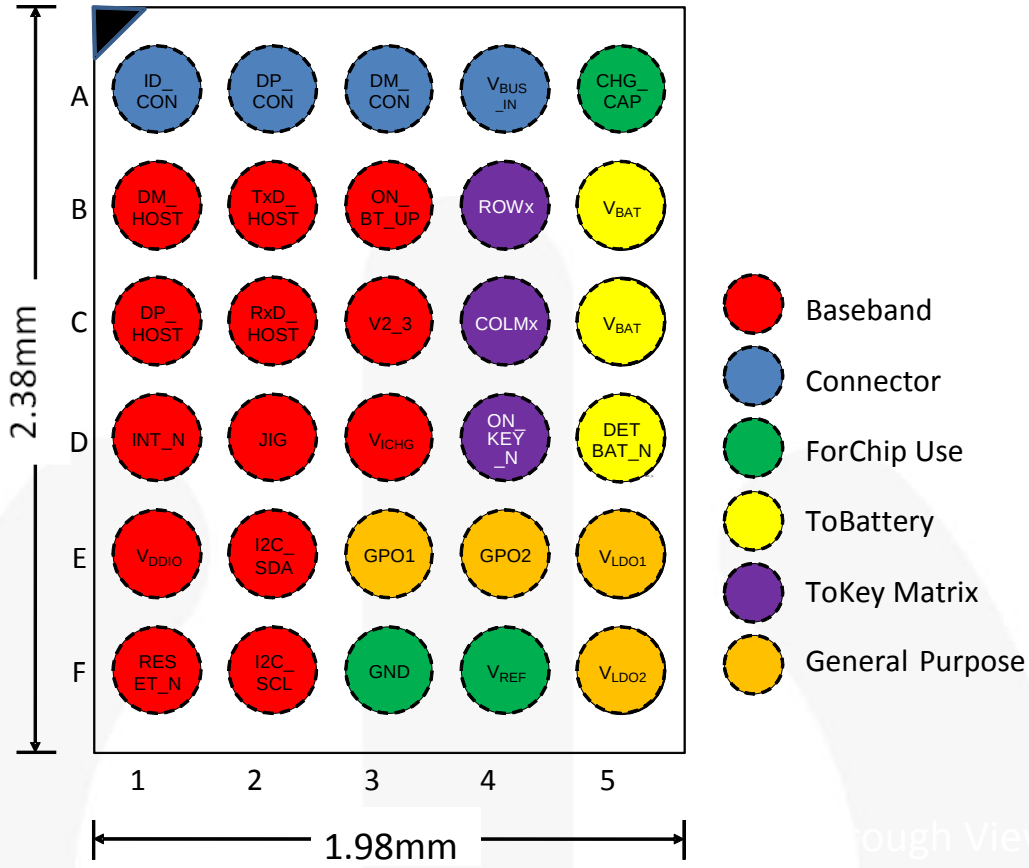


Figure 3. Pin Assignment (Top Through View)

Pin Descriptions

Name	Ball	Type	Default State	Description
USB Interface				
DP_HOST	C1	Signal Path	Open	D+ signal switch path; dedicated USB port to be connected to the USB transceiver on the phone
DM_HOST	B1	Signal Path	Open	D- signal switch path; dedicated USB port to be connected to the USB transceiver on the phone
UART Interface				
TxD_HOST	B2	Signal Path	Open	Transmitter (Tx) switch path from UART on the phone to the D- pin of the USB connector
RxD_HOST	C2	Signal Path	Open	Receiver (Rx) switch path from UART on the phone to the D+ pin of the USB connector
Connector Interface				
GND	F3	Ground	N/A	Ground
ID_CON	A1	Signal Path	Pull-Up Current	Connected to the USB connector ID pin and used for detecting accessories
DP_CON	A2	Signal Path	Open	Connected to the USB connector D+ pin; depending on the signaling mode, this pin can be switched to DP_HOST or RxD_HOST pins
DM_CON	A3	Signal Path	Open	Connected to the USB connector D- pin; depending on the signaling mode, this pin can switched to DM_HOST or TxD_HOST pins
V_{BUS_IN}	A4	Power Path	N/A	Input voltage supply pin to be connected to the VBUS pin of the USB connector

<table>
<tr><th>Name</th><th>Ball</th><th>Type</th><th>Default State</th><th>Description</th></tr>
<tr><td colspan="5">Power Interface</td></tr>
<tr><td>V_{DDIO}</td><td>E1</td><td>Power</td><td>N/A</td><td>Factory and I^2C interface I/O supply pin</td></tr>
<tr><td>V_{BAT}</td><td>B5,C5</td><td>Power Path</td><td>N/A</td><td>Battery charger output and chip supply pin to be connected to mobile phone battery</td></tr>
<tr><td>V_{LDO1}</td><td>E5</td><td>Power</td><td>Hi-Z</td><td>Programmable first LDO regulator output</td></tr>
<tr><td>V_{LDO2}</td><td>F5</td><td>Power</td><td>Hi-Z</td><td>Programmable second LDO regulator output</td></tr>
<tr><td>V_{REF}</td><td>F4</td><td>Power</td><td>Hi-Z</td><td>0.6 V voltage reference for internal use. Can output a maximum of 1 mA external load. Needs to be enabled for LDO operation.</td></tr>
<tr><td>CHG_CAP</td><td>A5</td><td>Power</td><td>Hi-Z</td><td>Bypass capacitor for charger that forms a low-voltage power supply for internal circuitry (0.1 µF typical value)</td></tr>
<tr><td>V_{ICHG}</td><td>D3</td><td>Power</td><td>Hi-Z</td><td>Analog signal proportional to the charging current flowing to battery from V_{BUS_IN}</td></tr>
<tr><td colspan="5">Other Interface</td></tr>
<tr><td>JIG</td><td>D2</td><td>Open-Drain Output (V_{DDIO})</td><td>Hi-Z</td><td>Output control signal driven by the FSA9591 and used by the processor for factory test modes (active LOW open drain output)</td></tr>
<tr><td>ON_KEY_N</td><td>D4</td><td>Input (Comparator)</td><td>N/A</td><td>Input that indicates whether the phone ON key has been pressed (active LOW)</td></tr>
<tr><td>ON_BT_UP</td><td>B3</td><td>Switched Path</td><td>Hi-Z</td><td>Switch connected to the V2_3 pin to boot up the processor during factory mode or when the ON_KEY_N signal is asserted
<table>
<tr><th>VBUS</th><th>ON_KEY_N</th><th>JIG</th><th>ON_BT_UP =</th></tr>
<tr><td>Valid VBUS</td><td>X</td><td>X</td><td>V2_3</td></tr>
<tr><td>LOW</td><td>LOW</td><td>X</td><td>V2_3</td></tr>
<tr><td>LOW</td><td>HIGH</td><td>LOW</td><td>V2_3</td></tr>
<tr><td>LOW</td><td>HIGH</td><td>Hi-Z</td><td>Hi-Z</td></tr>
</table></td></tr>
<tr><td>V2_3</td><td>C3</td><td>Switched Path</td><td>Hi-Z</td><td>Pin switched to ON_BT_UP for realizing ON_BT_UP functionality (see ON_BT_UP description)</td></tr>
<tr><td>COLMx</td><td>C4</td><td>Switched Path</td><td>Hi-Z</td><td>Used to translate the ON key signal from a high-voltage signal into a low-voltage closed switch in the processor key matrix circuitry. Switches to ROWx.
<table>
<tr><th>V_{BAT}</th><th>ON_KEY_N</th><th>COLMx/ROWx</th></tr>
<tr><td>LOW</td><td>X</td><td>OPEN</td></tr>
<tr><td>VALID</td><td>HIGH</td><td>OPEN</td></tr>
<tr><td>VALID</td><td>LOW</td><td>SHORT</td></tr>
</table></td></tr>
<tr><td>ROWx</td><td>B4</td><td>Switched Path</td><td>Hi-Z</td><td>Used to translate ON key signal from a high-voltage signal into a low-voltage closed switch in the processor key matrix circuitry. Switches to COLMx.
<table>
<tr><th>V_{BAT}</th><th>ON_KEY_N</th><th>COLMx/ROWx</th></tr>
<tr><td>LOW</td><td>X</td><td>OPEN</td></tr>
<tr><td>VALID</td><td>HIGH</td><td>OPEN</td></tr>
<tr><td>VALID</td><td>LOW</td><td>SHORT</td></tr>
</table></td></tr>
<tr><td>RESET_N</td><td>F1</td><td>Open-Drain Output (V_{DDIO})</td><td>N/A</td><td>Output to synchronize the processor with detected accessories. The threshold is 1.4 V rising edge and 1.2 V falling edge and the pulse lasts for 250 ms.</td></tr>
<tr><td>GPO1</td><td>E3</td><td>Output (V_{DDIO})</td><td>N/A</td><td>General purpose; first output programmed from register bit GPO [GPO1]. This can be push/pull or open drain based on the register bit GPO [GPO1_OD].</td></tr>
<tr><td>GPO2</td><td>E4</td><td>Output (V_{DDIO})</td><td>N/A</td><td>General purpose; second output programmed from register bit GPO [GPO2]. This can be push/pull or open drain based on the register bit GPO [GPO2_OD].</td></tr>
<tr><td>DETBAT_N</td><td>D5</td><td>Input (Comparator)</td><td>N/A</td><td>Detect battery input to determine the battery presence in the phone;
DETBAT_N=HIGH when battery is not present.
DETBAT_N=LOW when battery is present or when charger is enabled, regardless of battery presence. Internally pulled up.</td></tr>
</table>

Name	Ball	Type	Default State	Description
I^2C Interface				
I2C_SCL	F2	Input (V_{DDIO})	N/A	I^2C serial clock signal to be connected to the phone-based I^2C master
I2C_SDA	E2	Open-Drain I/O (V_{DDIO})	Hi-Z	I^2C serial data signal to be connected to the phone-based I^2C master
INT_N	D1	CMOS Output (V_{DDIO})	Low	Interrupt active LOW output used to prompt the phone baseband processor to read the I^2C register bits or indicate a change in ID_CON pin status or accessories' attach status

1. Functionality

The FSA9591 is USB port accessory detector and switch with integrated 28 V over-voltage tolerance. Fully controlled using I^2C, FSA9591 enables high-speed USB 2.0 Standard Downstream Port (SDP), USB Charging Downstream Port (CDP) battery charger, USB Dedicated Charging Port (DCP) charger data cables to use a common connector micro or mini USB 2.0 port. Factory-mode cables can be detected and switched to use either the UART or USB data path. The FSA9591 can be programmed for manual switching or automatic switching of data paths.

1.1. Functional Overview

The FSA9591 is designed for minimal software requirements for proper operation. The flow diagram in Figure 4 walks through the fundamental steps of operation and contains references to more detailed information.

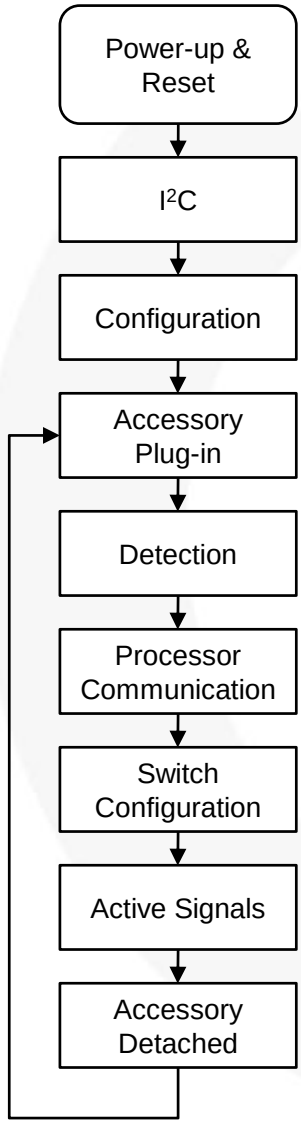


Figure 4. Basic Operation Flow

State	Datasheet Section	Description
Power-Up & Reset	*Section 2*	Applies power to the device and resets state of the device
I^2C	*Section* 3	Communication with device through I^2C
Configuration	*Section* 4	Configures the device using I^2C and the internal registers (which can be bypassed during power-up)
Detection	*Section 5*	Manages accessory detection, including attachment and detachment
Processor Communication	*Section 1*	How the detection of the accessory is indicated to the processor
Switch Configuration	*Section 7*	Configuration of switches based on detection
Active Signal	*Section 11*	Signal performance of selected configuration

2. Power-Up & Reset

The FSA9591 does not need special power sequencing for correct operation. The main power for accessory detection is provided by V_{BAT} only. V_{DDIO} is only used for I^2C interface and interrupt processing. The linear charger power is provided by V_{BUS_IN}.

Table 1 summarizes the enabled features of each power state. The valid voltages levels for each power supply can be found in Section 12.2

Table 1. Power States Summary

Valid V_{BUS_IN}	Valid V_{BAT}	Valid V_{DDIO}[2]	Power State	Enabled Functionality			
				Processor Communication (I^2C & Interrupts)	Detection/ Switching	Charging	LDO
N	N	N	Power Down	NO			
N	N	Y[3]	Not Typical	Illegal State			
N	Y	N	Detection/Switching Active	NO	YES	NO	YES
N	Y	Y	Detection/Switching Active	YES	YES	NO	YES
Y	N	N	Charging Only	NO	NO	YES	NO
Y	N	Y[3]	Not Typical	NO	NO	YES	NO
Y	Y	N	Powered On State	NO	YES	YES	YES
Y	Y	Y	Powered On State	YES	YES	YES	YES

Notes:

2. V_{DDIO} is expected to be the same supply used by the baseband I/Os.
3. Typically V_{DDIO} is only present when V_{BAT} is valid.
4. X=Don't care.

2.1. Reset

When the device is reset, all the registers are initialized to the default values shown in Section 12.14 and all switch paths are open. After reset or power up, FSA9591 enters Standby Mode and is ready to detect accessories sensed on the V_{BUS_IN} or ID_CON pins.

2.1.1. Hardware Reset

Power-On Reset (POR) is caused by the initial rising edge of V_{BAT} or V_{BUS_IN}.

2.1.2. Software Reset

The device can be reset through software by writing to the Reset bit in the Register (1BH).

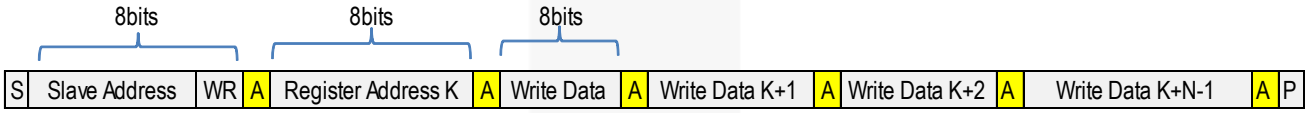
3. I²C

The FSA9591 integrates a full fast-mode I²C slave controller compliant with the I²C specification version 2.1. The FSA9591 I²C interface runs up to 400 kHz.

The slave address is shown in Table 2. Status information and configuration occurs via the I²C interface. *Please see Section 12.12 for more information.*

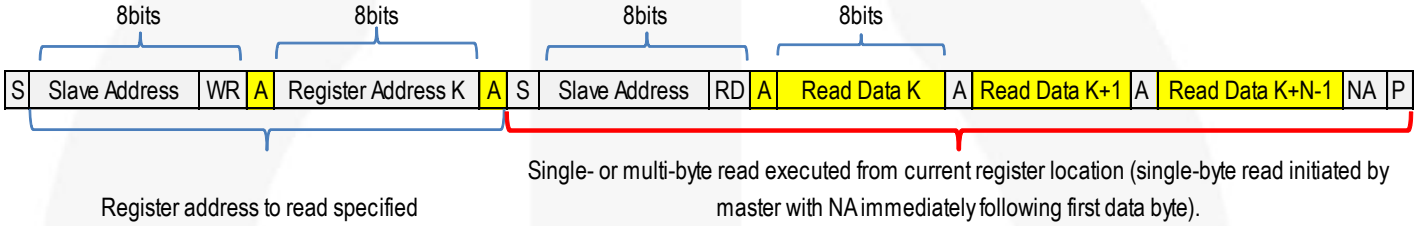
Table 2. I²C Slave Address

Name	Size (Bits)	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Slave Address	8	0	1	0	0	1	0	1	Read / Write



Note: A single-byte write is initiated by the master with P immediately following first data byte.

Figure 5. I²C Write Sequence



Note: If no register specified, master reads from the current register. In this case, only sequence in red bracket is needed.

Figure 6. I²C Read Sequence

Legend

	From Master to Slave	**S**	Start Condition	**NA**	NOT Acknowledge (SDA HIGH)	**RD**	Read=1
	From Slave to Master	**A**	Acknowledge (SDA LOW)	**WR**	Write=0	**P**	Stop Condition

4. Configuration

FSA9591 requires minimal configuration for proper detection, charging and reporting. Follow these steps for full configuration:

1. Write Control register (02h) to configure manual or automatic switching modes.
   a. If using manual switching modes, write Manual SW 1 register (13h) to configure switches.
2. Write Control register (02h) to clear INT Mask bit. This enables interrupts to the baseband.

The linear charger defaults to automatic charging at either 90mA or 450mA based on the accessory that was detected.

5. Detection

The FSA9591 monitors both V_{BUS_IN} and ID_CON to detect accessories. The ID_CON detection is a "resistive detection" that reads the resistance to GND on the ID_CON pin to determine the accessory attached. Table 3 shows assignment of accessories based on resistor values. FSA9591 can also detect accessories with ID resistances outside the specified ranges; these are detected in the same manner as the defined accessories. FSA9591 interrupts the baseband processor and provides the correct ADC value, as shown in Table 3.

Table 3. ID_CON Accessory Detection

ADC Code					Equivalent R_{ID}[6]			Description
4	3	2	1	0	Min.	Target	Max.	
1	0	1	0	1	117.4 kΩ	121 kΩ	124.6 kΩ	Unknown Accessory
1	0	1	1	0	145.5 kΩ	150 kΩ	154.5 kΩ	Unknown Accessory
1	0	1	1	1	176.4 kΩ	200 kΩ[5]	206.0 kΩ	Travel Adapter (TA) or Car Kit Type 1 Charger
1	1	0	0	0	247.3 kΩ	255 kΩ	262.7 kΩ	Factory Mode Boot OFF-USB
1	1	0	0	1	291.9 kΩ	301 kΩ	310.1 kΩ	Factory Mode Boot ON-USB
1	1	0	1	0	354.0 kΩ	365 kΩ	375.9 kΩ	Unknown Accessory
1	1	0	1	1	428.7 kΩ	442 kΩ[5]	455.3 kΩ	Unknown Accessory
1	1	1	0	0	507.3 kΩ	523 kΩ	538.7 kΩ	Factory Mode Boot OFF-UART
1	1	1	0	1	600.4 kΩ	619 kΩ	637.6 kΩ	Factory Mode Boot ON-UART
1	1	1	1	0	750.0 kΩ	1000 kΩ	1030.0 kΩ	Unknown Accessory
Not 'h1F or any code above					3 MΩ	None of the above ranges		Unknown Accessory

Note:
5. These accessories need V_{BUS} to be valid to be detected since they are charger accessories.
6. For resistances between the defined regions, the FSA9591 detects the ADC value above OR below the given resistance.

Factory modes are initiated with the attachment of special test hardware, called a "JIG box," for factory testing. The FSA9591 automatically configures switch paths to any of the factory-mode accessories when the appropriate resistor is sensed on the ID_CON pin. A change of resistor on the ID_CON pin dynamically switches between factory modes and auto-configures the appropriate switch paths without detaching and attaching the cable.

The different factory mode accessories with the associated resistor values (1% standard resistors) on the ID_CON pin and The switch paths for factory modes are listed in Table 4. The FSA9591 allows HS USB, FS USB, and UART signals to be passed on both ports with equal performance. This allows greater flexibility when designing with the FSA9591.

Table 4. ID_CON Factory Cable Detection

Configuration Type		DP_CON	DM_CON	ID_CON		
Factory Mode Jig: UART	Boot_On	DP_HOST1	DM_HOST1	600 kΩ	619 kΩ	637 kΩ
	Boot_Off	DP_HOST1	DM_HOST1	507 kΩ	523 kΩ	538 kΩ
Factory Mode Jig: USB	Boot_On	DP_Host	DM_Host	292 kΩ	301 kΩ	310 kΩ
	Boot_Off	DP_Host	DM_Host	247 kΩ	255 kΩ	262 kΩ

The FSA9591 detection algorithms monitor both the V_{BUS} and ID pins of the USB interface. Based on the detection results, multiple registers are updated and the INTB pin is asserted to indicate to the baseband processor that an accessory was detected and to read the registers for the complete information. The detection algorithm allows the application to control the timing of the detection algorithm and the configuration of the internal switches. The flow diagram in Figure 8 shows the operation of the detection algorithm.

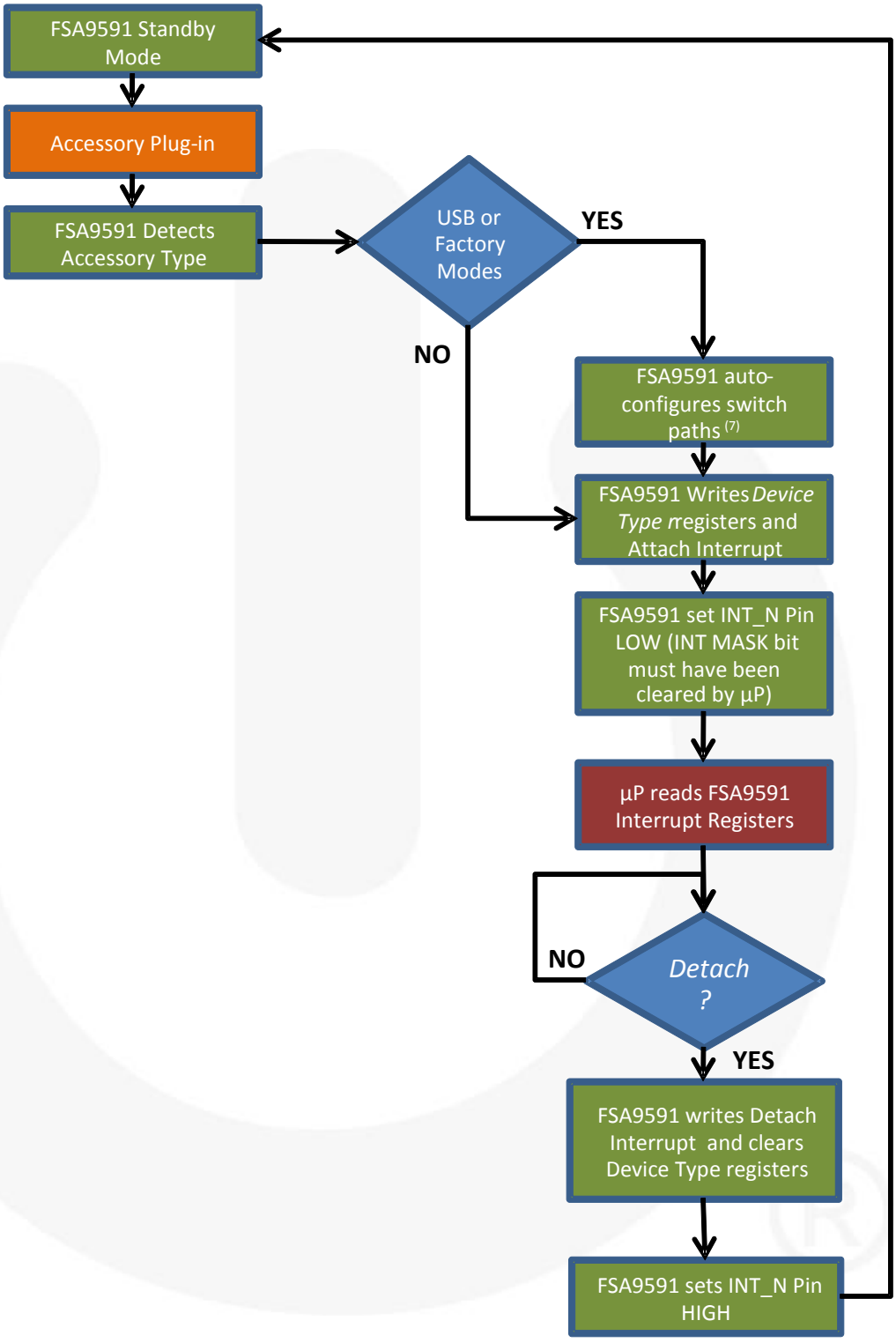


Figure 7. Factory Cable Detection

Note:

7. Factory modes require V_{DDIO}=HIGH before configuring the switches. Refer to the factory mode flow diagram in Figure 8 for details.

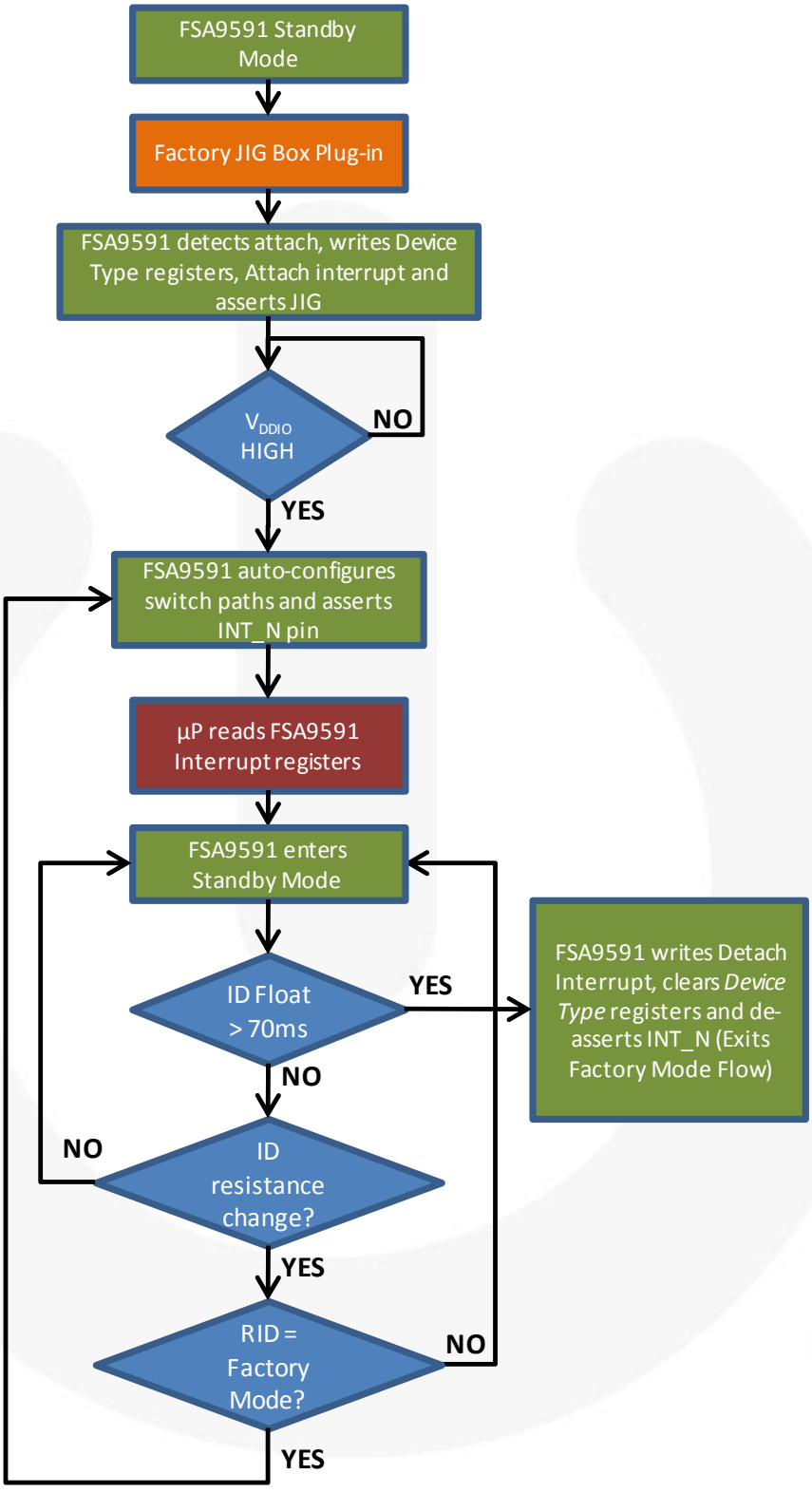


Figure 8. Factory Cable Detection Flow Chart

5.1. USB Port Detection

The types of USB 2.0 ports the FSA9591 can detect are summarized in Table 5.

Table 5. ID_CON and VBUS Detection Table for USB Devices

V_{BUS_IN}	DP_CON	DM_CON	ID_CON Resistance to GND			Accessory Detected[8]
			Min.	Typ.	Max.	
5V	Not Checked	Not Checked	174.6 kΩ	200 kΩ	206 kΩ	TA (Travel Adapter) Charger (180 kΩ) and Car Kit Charger Type 1 only (200 kΩ)[9]
5V	Shorted to DM_CON	Shorted to DP_CON	3 MΩ	Open	Open	USB Dedicated Charging Port, Travel Adapter or Dedicated Charger (DCP)[9]
5V	DP_HOST	DM_HOST	3 MΩ	Open	Open	USB Charging Downstream Port (CDP)[9]
5V	DP_HOST	DM_HOST	3 MΩ	Open	Open	USB Standard Downstream Port (SDP)[9]

Notes:
8. The accessory type is reported in the Device Type 1 (0Ah) register for each valid accessory detected.
9. The FSA9591 follows the battery charging 1.1 specification, which uses DP_CON and DM_CON to determine the USB accessory attached. *Refer to Battery Charging 1.1 specification for further details.*

For SDP and CDP USB accessories, the following pin mapping is automatically configured:

- DP_HOST=DP_CON
- DM_HOST=DM_CON

For DCP charger, the DP_HOST and DM_HOST switches are open. For all USB accessories, V_{BUS_IN} has Over-Voltage Tolerance (OVT) up to 28 V.

6. Processor Communication

Typical communication steps between the processor and the FSA9591 during accessory detection are:

1. INTB is asserted LOW, indicating a change in accessory detection.
2. Processor reads the Interrupt 1 (03h) register to determine if an attach or detach event was detected.
3. Processor reads the Status registers to determine the exact accessory detected.
   a. Device Type 1 (09h): Indicates which USB, Car Kit CDP, or DCP accessory was detected.
   b. Device Type 2 (0Ah): Indicates which factory mode or unknown accessory was detected.

7. Switch Configuration

FSA9591 devices have two methods of configuring the internal switches: it can auto-configure the switches or the switches can be configured manually by the processor. Typical applications use Auto-Configuration Mode and do not require interaction with the baseband to configure the switches correctly.

7.1. Manual Switching

Manual switching is enabled by writing the following registers:

- Manual Switch (13h): Configures the switches for DM_CON and DP_CON in addition to manual control of the JIG output.

8. GPOs

The FSA9591 has two general-purpose outputs (GPOs) that typically turn on the functionality powered by the LDOs. The default state for the GPOs is push-pull outputs with GPO1_OD and GPO2_OD set LOW. If open-drain outputs are required, GPO1_OD and GPO2_OD should be set HIGH.

9. LDOs

The two Low Drop Out (LDO) regulators, which are powered from V_{BAT}, are programmable from 1.8 V to 3.6 V in increments of 100 mV. A 0.6 V reference on VREF must be enabled by writing the register bit GPO[REF_EN] to turn it on. This reference needs to turn on at least 20ms prior to the LDOs turning on to allow time to stabilize the reference if 0.1 nF bypass capacitance is used.

10. ON_KEY Keypad Functionality

The functionality of ON_BT_UP is described in Table 6.

Table 6. ON_KEY_N and ON_BT_UP Truth Table

VBUS	ON_KEY_N	JIG	ON_BT_UP
Valid VBUS	X	X	V2_3
LOW	LOW	X	V2_3
LOW	HIGH	LOW	V2_3
LOW	HIGH	Hi-Z	Hi-Z

How to translate ON_KEY_N to a position in the row and column matrix of the processor keypad is shown in Figure 9.

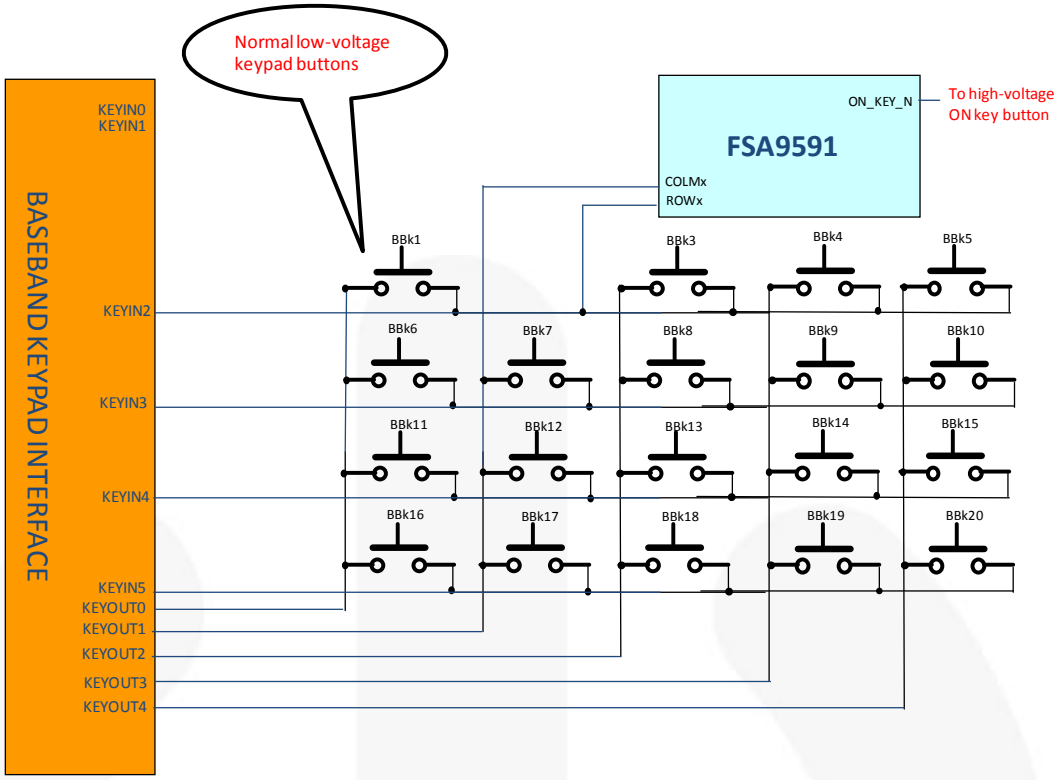


Figure 9. On Key to COLMx and ROWx Mappings

This is the way the FSA9591 translates the ON_KEY_N pin, where the COLMx and ROWx create a virtual button that would have occupied the missing BBk2 switch in the matrix above. Internal to the FSA9591, there is an analog switch that connects COLMx to ROWx based on ON_KEY_N as outlined in Table 7. With ON_KEY_N pulled HIGH to V_{BAT}, a valid V_{BAT} must be present for the keypad functionality to work properly.

Table 7. COLMx/ROWx Truth Table

V_{BAT}	ON_KEY_N	COLMx/ROWx
LOW	X	OPEN
VALID	HIGH	OPEN
VALID	LOW	SHORT

11. Linear Charger

11.1. Charging

Figure 10 shows the different stages of the Li+ linear charger when a charger is connected to the USB pins and a battery is present and discharged below 2.5 V. Generally, the prequalification (called “PRE-CHARGE” in Figure 10) stage is when the battery voltage is below 2.5 V when an I_{SHORT} current of 90 mA charges the battery to V_{SHORT} voltage of 2.5 V. Then the Fast Charge stage starts if a battery charger is detected and the current is increased considerably to a programmable $I_{OCHARGE}$ level (“CURRENT REGULATION” in Figure 10). The battery voltage climbs quickly based on the drop caused by the current across the load elements of the battery. Then the voltage climbs linearly until the constant voltage stage is reached at the programmable voltage of V_{OREG}. The current is monitored during this stage (“VOLTAGE REGULATION” in the figure) and, when it reaches the end of current I_{TERM}, charging either halts or progresses to the top off charging if enabled.

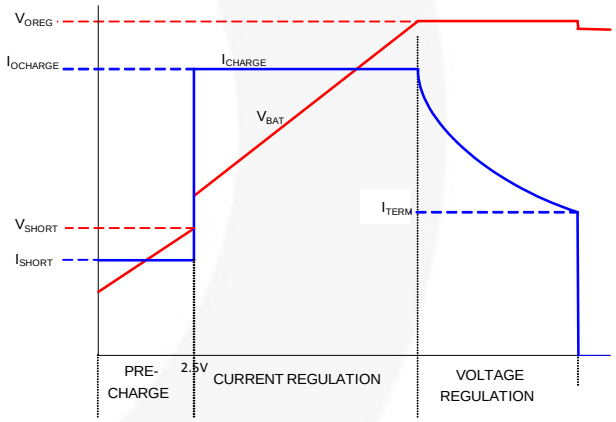


Figure 10. Default Charging Profile

11.1.1. Pre-Qualification Charging Stage

A typical battery has a protection circuit within the battery pack to disconnect the terminals below 2.7 V external to the FSA9591. If it gets below 2.7 V, the battery pack terminals are disconnected externally with the load switch within the battery pack, causing battery voltage V_{BAT} to decay quickly to ground since all that is holding V_{BAT} up is the decoupling capacitors externally. Another way that V_{BAT} can get so low is if V_{BAT} is shorted to ground accidentally. Both of these occurrences are very rare in a typical system since a dead battery is typically above 3 V and only goes below 3V over a long period of time via leakage.

When VBUS_IN is first detected as being within its valid range, two timers are started, a 30-minute timer for the dead battery provision (if that is enabled) via the Charger Ctrl1[DBP_EN] bit (enabled by default since the processor is usually not operating at this low battery voltage range) and a programmable timer for total charging elapsed time enabled (enabled by default as a 5-hour timer via the Charger Ctrl1 [TC_EN] and Charger Ctrl1 [TC_Time] bits).

The linear charger is expected to always take its power from VBUS_IN while monitoring V_{BAT} to determine the optimal charging profile for the shortest charging cycle.

If VBUS_IN is detected when V_{BAT} is below 2.5 V, a charging current of 90mA is used to trickle charge the battery. If it is not a short circuit, V_{BAT} should recover very quickly above 2.5 V since it is only charging decoupling capacitors. V_{DDIO} and V_{BAT} are below the operational voltage of the detection portion, so detection is not performed, nor does FSA9591 communicate over the I^2C lines as the linear charger charges the battery above the pre-qualification stage.

If there is a short circuit and the charger Ctrl1 [DBP_EN] bit is enabled (default case), the timer continues up to 30 minutes and expires, shutting down the charger. This limits the short-circuit current of 90mA to be drawn only for 30 minutes. The only way to recover from this fault condition is to remove the short circuit. If the short circuit is not removed, detaching and re-attaching the charger restarts the dead battery provision timer for another 30 minutes before shutting off again.

11.1.2. Constant Current/Constant Voltage Charging Stage

In this stage, V_{BAT} is above the pre-qualification voltage of 2.5 V, but below the programmed Charger Ctrl5 [CV_Voltage] value. The charger detection interrogates the DP_CON, DM_CON, and ID_CON lines to determine if a Dedicated Charger Port (DCP), Charging Downstream Port (CDP), car kit charger (200 kΩ on ID_CON), or a Travel Adapter (T_A, 180 kΩ on ID_CON) has been detected. If a charger is detected, the default charging current stays at the fast charge current of 450 mA (default) specified in Charger Ctrl3 [FC_Current] bits. Soft-start techniques are used to gradually increase current to minimize undesirable transients. If a charger is not detected and a USB Standard Downstream Port (SDP) is detected, the fast charge current drops to 90 mA like the pre-qualification current and continues to charge up the battery. This is summarized in Table 8.

Table 8. Default Charging Currents

FC_Override	Auto_FC	Accessory Detected	Fast Charge Current
1	X	X	FC_Current
0	0	X	90 mA
0	1	CDP / DCP/ Car Kit Type 1	FC_Current
0	1	SDP / Unknown / Factory	90mA

Thermal issues are also considered *(see Thermal Regulation section below)* since this is the stage when there is the maximum voltage difference between V_{BUS_IN} and V_{BAT}. Similar to the pre-qualification stage, communication with the baseband is not possible, at least initially, when V_{BAT} is between 2.5 V and the weak-battery threshold (Charger Ctrl2 [WB_Threshold]) so the FSA9591 must be able to charge the battery properly without interaction with the baseband. The 30-minute dead-battery provision timer continues during this stage. When this timer expires and V_{BAT} does not exceed the weak battery threshold, the charger is disabled in compliance with the Battery Charging USB specifications for Dead Battery Provision (DBP). If the processor wakes up prior to the weak-battery threshold, it can change the weak-battery threshold via the Charger Ctrl2 [WB_Threshold] bits to a value consistent with actual wake up voltage and/or disable the dead battery timer via the Charger Ctrl1 [DBP_EN] bit.

Beyond the weak-battery threshold, the processor is expected to be up and controlling the charging process. The constant current is expected to be increased to match the battery charge capacity and the timers for total elapsed charging time can be changed accordingly. The constant voltage threshold is also expected to be set based on battery type and battery temperature, which should be monitored by the processor via separate controls. Thermal regulation within the FSA9591 may have little correlation to the battery temperature since the heat dissipation of the PCB that the FSA9591 is soldered to may be completely different from the heat dissipation within the battery pack.

When the programmed constant voltage threshold (programmed by Charger Ctrl5[CV_Voltage] bits) is approached, the fast charging current loop is gradually changed to a constant voltage loop where the current is allowed to decay. Charging continues until the end of charge current (set by Charger Ctrl4 [EC_Current] bits) is crossed.

If the top-off timer (set by Charger Ctrl1 [TopOff_EN] bit) is disabled and Charger Ctrl1 [AutoStop] bit is set, all charging stops and the charger monitors V_{BAT}. If V_{BAT} falls 150 mV below the programmed constant voltage, the fast charge charging cycle starts again. A debounce time of 60 ms prior to restarting this cycle prevents glitches or temporary GSM current load of up to 2 A for <1 ms. If the top-off timer is enabled and the AutoStop bit is set; for 30 minutes after the end of charge current threshold has been crossed, the constant voltage charge cycle continues. After that, all charging is stopped and V_{BAT} is monitored again for a drop of 150 mV. If the Charger Ctrl1 [AutoStop] bit is not set, the constant voltage state is never left and the charger keeps trickle charging the battery to keep the voltage at the programmed Charger Ctrl5 [CV_Voltage] voltage.

The FSA9591 maintains this constant voltage with ±0.5% at room temperature to ensure optimal battery performance. The timer measuring the total charging elapsed time continues until the end of charge current threshold is crossed and does not include the top-off timer. If the total time exceeds the time in the Charger Ctrl2 [TC_Time] bits, charging is stopped and the processor (if the voltage is high enough for the processor to function) can interrogate the source of the problem, correct it, then disables and re-enables the charger again to restart charging. If the voltage is not high enough for the processor to function, the problem with the battery needs to be solved and the USB cable needs to be unplugged and plugged back in again.

11.1.3. Timers

The FSA9591 contains multiple timers to ensure that the battery is safely charged under all conditions. These timers include the dead-battery provision timer of 30 minutes, the total-charge timer of 5 to 7 hours, and the top-off timer of 30 minutes. Each timer can be enabled or disabled through I^2C register accesses. The total-charge timer value can be programmed through I^2C also.

The timers do not reset when an OVP event occurs. If V_{BAT} is above the weak-battery threshold and the baseband is active, the FSA9591 causes an interrupt when the OVP occurs and when the OVP event is disabled. This allows the baseband to control the timers based on the system needs. When OVP is detected, charging stops until the OVP event has recovered.

If V_{BAT} is below the weak-battery threshold and the dead-battery timer is active, FSA9591 takes the most conservative approach and keeps the DBP timer running when OVP is detected.

11.1.4. Thermal Regulation

The FSA9591 contains a thermal regulation loop that is enabled when the junction temperature exceeds 120°C. When this temperature is exceeded, the FSA9591 starts to regulate the current to lower the temperature. It does this by reducing the fast charge current to 90 mA (it is most likely to be in the fast charge cycle since that is when there's maximum power consumption by the linear charger), waits 1 ms, increases the current to 200 mA, waits 1ms, continues along the fast charge currents specified in the Charger Ctrl3 [FC_Current] where the wait between fast charge current steps is 1ms. This algorithm allows for the fastest recovery from a thermal regulation event while still averaging a current that keeps the temperature below 120°C.

The FSA9591 also terminates charging completely if the junction temperature exceeds 140°C. In both cases, the FSA9591 indicates which temperature event occurred via the Interrupt 1 [TREG_EN] and Interrupt 1 [TSD_EN] bits and indicates the removal of these conditions via the Interrupt2 [TREG_DIS] and Interrupt2 [TSD_DIS] bits. Temperature is continuously monitored whenever the charger is enabled.

11.1.5. OVP, OCP, VBUS_IN Regulation

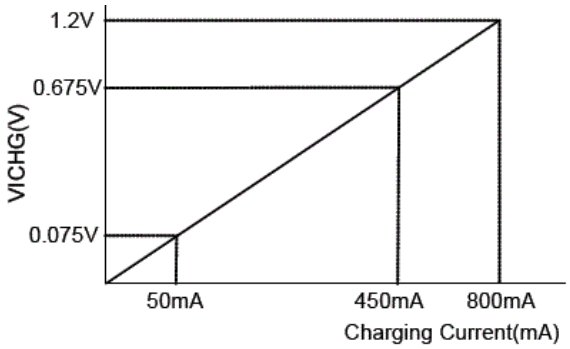
The FSA9591 contains programmable over-voltage protection (OVP) on VBUS_IN, ranging from 6.5 V to 8.0 V, as specified in the Charger Ctrl2 [OVP_Threshold] bits with the default setting of 7 V. If OVP is detected, the FSA9591 terminates charging functionality if charging is active when OVP is detected. The FSA9591 interrupts the processor when the OVP event via the Interrupt 1[OVP_EN] bit is detected and when the OVP event is removed via the Interrupt 1[OVP_DIS] bit. The FSA9591 VBUS_IN can tolerate voltages up to 28 V to handle the worst-case automotive scenarios for USB VBUS voltage.

V_{BUS_IN} is typically 5 V ±5-10%, depending on the charging current. If the FSA9591 linear charger is programmed to a higher current than the charger can support, a V_{BUS_IN} control loop actively regulates the charging current to maintain at least 4.3 V (typical) on V_{BUS_IN}. The FSA9591 attempts to lower the charger current to allow V_{BUS_IN} to recover to at least 4.3 V. In cases where the charger V_{BUS_IN} is not limited by the charger current, the FSA9591 attempts to lower the current until it reaches the minimum current level and then disables the charger. This V_{BUS_IN} regulation loop is enabled by default and controlled by the Vbus_Reg_Dis bit in the Charger_Ctrl1 register.

If the V_{BUS_IN} regulation loop is disabled, the charging cycle is stopped when V_{BUS_IN} falls below the V_{BUS_IN} valid falling threshold of 3.5 V. Charging remains stopped until the V_{BUS_IN} voltage rises above the rising V_{BUS_IN} valid threshold of 3.7 V and stays above this threshold.

11.2. VICHG

The VICHG is utilized by the host system to identify the amount of current flowing through the charger FET. VICHG is enabled by writing the VICHG_EN bit in the register. When disabled, VICHG has an internal pull-down of 15 kΩ. V_{ICHG} should not exceed 2.0 V when enabled.



V_{I_CHG}=Charging Current • 1.5

Figure 11. VI_CHG Characteristic

11.3. DETBAT_N

For a typical battery pack, there is an extra terminal with a thermistor NTC resistor between this terminal and ground, which is expected to be much less than 100 kΩ. This terminal is tied to the DETBAT_N pin for a system to disable the charger whenever a battery is not present. DETBAT_N internally has a current source that detects the absence of any path to ground that is >100 kΩ on the DETBAT_N pin. Once a HIGH is detected on DETBAT_N, the charger is immediately disabled.

Some systems, for factory operation or other uses, may leave the charger enabled regardless of whether the battery pack is present or not. In these systems, it is expected that DETBAT_N is tied LOW — always with a resistance to ground of 10 kΩ.

11.4. RESET_N

RESET_N output is used as a system-level Power-On Reset (POR) triggered when V_{DDIO} is above 1.4 V. This RESET_N open-drain output is pulled-down upon FSA9591 power up and released to HIGH after 250 ms (typically from when V_{DDIO} crosses 1.4 V on its rising edge). RESET_N requires a valid V_{BAT} for RESET_N to be actively pulled LOW after power up. This is a tight threshold comparator of V_{DDIO} with a hysteresis of 200 mV to accommodate a slowly rising signal. When V_{DDIO} falls below 1.2 V, RESET_N is pulled LOW again. This timing is shown in Figure 12. RESET_N is not reset on a software reset and is not intended to be a system-level reset, but a POR on VDDIO. The 250 ms timer is reset if V_{DDIO} triggers the falling-edge reset.

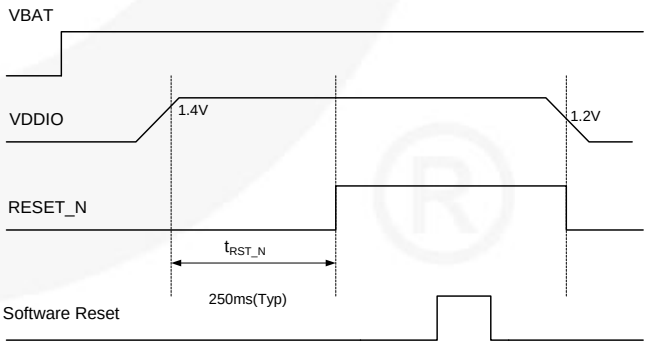


Figure 12. RESET_N Timing

12. Product Specifications

12.1. Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Parameter			Min.	Max.	Unit
V_{BAT}	Supply Voltage from Battery			-0.5	6.0	V
V_{BUS_IN}	Supply Voltage from USB Connector			-0.5	28.0	V
V_{DDIO}	Supply Voltage from Baseband			-0.5	6.0	V
V_{SW}	Switch I/O Voltage	USB		-1.0	6.0	V
		UART		-1.0	6.0	
V_{IO}	I/O Voltage	I2C_SDA, I2C_SCL, INT_N, GPO1, GPO2, RESET_N		-0.3	V_{DDIO} + 0.3	V
		JIG, DETBAT_N, ON_KEY_N		-0.3	V_{BAT} + 0.3	V
I_{IK}	Input Clamp Diode Current			-50		mA
I_{SW}	Switch I/O Current (Continuous)	USB at T_A=85°C			25	mA
		UART at T_A=85°C			12	
I_{SWPEAK}	Peak Switch Current (Pulsed at 1ms Duration, <10% Duty Cycle)				150	mA
T_{STG}	Storage Temperature Range			-65	+150	°C
T_J	Maximum Junction Temperature				+150	°C
T_L	Lead Temperature (Soldering, 10 Seconds)				+260	°C
ESD	IEC 61000-4-2 System	USB Connector Pins (DP_CON, DM_CON, V_{BUS_IN}, ID_CON) to GND	Air Gap	15.0		kV
			Contact	8.0		
	Human Body Model, JEDEC JESD22-A114		USB Pins	4.0		
			All Others	2.0		
	Charged Device Model, JEDEC JESD22-C101		All Pins	1.5		
Surge	IEC 61000-4-5 Surge Test[10]		V_{BUS_IN}	24		V
			DP_CON/DM_CON	10		

Note:

10. Modified voltage requirements: voltage impulse into an open-circuit with a 1.2 µs ramp-up rate and a 50 µs ramp-down rate.

12.2. Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to Absolute Maximum Ratings.

Symbol	Parameter		Min.	Typ.	Max.	Unit
V_{BAT}	Battery Supply Voltage		2.7		4.4	V
V_{BUSIN_DET}	V_{BUS_IN} Voltage for Valid Detection		4.0	5.0	6.0	V
V_{BUSIN_CHG}	V_{BUS_IN} Voltage for Valid Charging		4.35	5.00	6.00	V
V_{BUS}-V_{BAT}	V_{BUS_IN} – V_{BAT} Voltage for Valid Charging		200			mV
V_{DDIO}	I/O Supply Voltage		1.6	1.8	3.6	V
V_{SW}	Switch I/O Voltage	USB Path Active	0		3.6	V
		UART Path Active	0		3.6	
ID_{CAP}	Capacitive Load on ID_CON Pin for Reliable Accessory Detection				1.0	nF
T_A	Operating Temperature		-40		+85	ºC
T_J	Junction Temperature		-40		+125	ºC
Θ_{JA}	Thermal Resistance Junction-to-Ambient			60		ºC/W

12.3. Switch Path DC Electrical Characteristics

Unless otherwise specified, recommended T_A and T_J temperature ranges (T_A=-40 to +85°C, T_J=-40 to +125°C). All typical values are at T_A=25°C unless otherwise specified.

12.3.1. IO Specifications

Symbol	Parameter	Voltage	Conditions	Min.	Typ.	Max.	Unit
INT_N (Push-Pull)		**V_{DDIO} (V)**					
V_{OH}	Output High Voltage	1.6 to 3.6	I_{OH}=-3 mA	0.8•V_{DDIO}			V
V_{OL}	Output Low Voltage	1.6 to 3.6	I_{OL}=3 mA			0.2•V_{DDIO}	V
JIG, RESET_N (Open-Drain)		**V_{DDIO} (V)**					
V_{OL}	Output Low Voltage	1.6 to 3.6	I_{OL}=3 mA			0.2•V_{DDIO}	V
RESET_N Generation		**V_{BAT} (V)**					
V_{RSTN}	V_{DDIO} Threshold for Generating RESET_N Output	3.0 to 4.4			0.2•V_{BAT}		V
t_{RSTN}	RESET_N Active Timeout Period; from V_{DDIO}≥1.4V to RESET_N=HIGH(11)	3.0 to 4.4	RST_TO=00	200	250	300	ms
General-Purpose Outputs (GPO1 and GPO2)		**V_{DDIO} (V)**					
V_{OH}	Output High Voltage, GPO [GPOx_OD]=0	1.6 to 3.6	I_{OH}=-3 mA	0.8•V_{DDIO}			V
V_{OL}	Output Low Voltage, GPO [GPOx_OD]=X	1.6 to 3.6	I_{OL}=3 mA			0.2•V_{DDIO}	V
Comparator Input (ON_KEY_N)		**V_{BAT} (V)**					
V_{IH}	High-Level Input Voltage	3.0 to 4.4		1.1			V
V_{IL}	Low-Level Input Voltage	3.0 to 4.4				0.4	V
I^2C Interface Pins – Fast Mode (I2C_SDA,I2C_SCL)		**V_{DDIO} (V)**					
V_{IL}	Low-Level Input Voltage	1.6 to 3.6				0.3•V_{DDIO}	V
V_{IH}	High-Level Input Voltage	1.6 to 3.6		0.7•V_{DDIO}			V
V_{HYS}	Hysteresis of Schmitt Trigger Inputs	1.6 to 3.6	V_{DDIO}>2 V	0.05•V_{DDIO}			V
			V_{DDIO}<2 V	0.1•V_{DDIO}			V
I_{I2C}	Input Current of I2C_SDA and I2C_SCL Pins	1.6 to 3.6	Input Voltage 0.26 V to 2.34 V	-10		10	µA
V_{OL1}	Low-Level Output Voltage at 3 mA Sink Current (Open-Drain)	3.0 to 4.4	V_{DDIO}>2 V	0		0.4	V
			V_{DDIO}<2 V			0.2V_{DDIO}	V

12.4. Switches

Symbol	Parameter	V_{BAT} (V)	Conditions	T_A=-40 to +85°C, T_J=-40 to +125°C			Unit
				Min.	Typ.	Max.	
I_{OFF}	Power-Off Leakage Current	0	All Data Ports, V_{SW}=1 V to 4.4 V			10	µA
$I_{NO(OFF)}$	Off Leakage Current	4.4	I/O pins=0.3 V, 4.1 V, or Floating	-0.100	0.006	0.100	µA
I_{IDSHRT}	Short Circuit Current(11)	3.0 to 4.4	Current Limit if ID_CON=0 V		20		µA
USB Switch ON Path							
USB Analog Signal Range		3.0 to 4.4		0		3.6	V
R_{ONUSB}	USB Switch On Resistance(12)	3.0 to 4.4	HS-USB $V_{D+/D-}$=0 V, 0.4 V, I_{ON}=8 mA,		8.0	16.0	Ω
			FS-USB V_{SW}=0 V, 3.6 V, I_{ON}=24 mA		11.5	19.0	
UART Switch ON Paths							
V_{AR}	Analog Signal Range	3.0 to 4.4		0		3.6	V
R_{ONUART}	UART Switch On Resistance(12)	3.0 to 4.4	HS-USB $V_{D+/D-}$=0 V, 0.4 V, I_{ON}=8 mA		8.0	16.0	Ω
			FS-USB V_{SW}=0 V, 3.6 V, I_{ON}=24 mA		11.5	19.0	
ON_BT_UP to V2_3 Switch and COLMx to ROWx Switch Characteristics							
R_{ONMISC}	Switch On Resistance(12)	3.0 to 4.4	V_{SW}=0V to 4.4 V, I_{ON}=1 mA		36		Ω

Notes:
11. Limits based on electrical characterization data.
12. On resistance is the voltage drop between the two terminals at the indicated current through the switch.

12.5. LDOs

Symbol	Parameter	V_{BAT} (V)	Conditions	T_A=-40 to +85°C, T_J=-40 to +125°C			Unit
				Min.	Typ.	Max.	
V_{LDO}	LDO Output Voltage Programmable Range	3.0 to 4.4	I_{LDO}=300 mA	1.8		3.6	V
V_{STEP}	LDO Voltage Steps	3.0 to 4.4	See LDOx_Ctrl [LDOx_Voltage] for Exact Values		100		mV
V_{DROP}	Dropout Voltage	3.0 to 4.4	I_{LDO}=300 mA		250		mV
I_{LDOMIN}	Minimum Output Current	3.0 to 4.4		0			mA
I_{LDOMAX}	Maximum Output Current	3.0 to 4.4		300			mA
d_{VLDOR}	Output Voltage Accuracy	3.0 to 4.4	Over Range of LDO Output Voltage at T_A=25°C	-2.0		2.0	%
d_{VLDOF}	Output Voltage Accuracy Over Full Range	3.0 to 4.4	Over Range of LDO Output Voltage	-3.0		3.0	%
d_{LINE}	Line Regulation(13)	*See Conditions*	V_{BAT}=$V_{LDO1(NOM(}$ +0.5 V to 3.6 V, I_{LDO}=1 mA		0.15	3.00	%/V
d_{LOAD}	Load Regulation(13)	3.8	I_{LDO}=1 mA to 300 mA		12	70	µV/mA
I_{LDO_SC}	Maximum Current Limit	3.0 to 4.4	Short-Circuit Current Limit or Startup Peak Current		620	900	mA
PSRR	Power Supply Rejection Ratio(13)	3.0 to 4.4	f=1 kHz		50		dB
e_N	Output Noise Voltage(13)	3.0 to 4.4	f=10 Hz to 100 kHz		100		μV_{RMS}
t_{ON}	Turn-On Time	3.0 to 4.4	From LDOx_EN I^2C Command to Start Ramp, GPO[REF_EN]=1		100		µs

Continued on the following page…

Symbol	Parameter	V_{BAT} (V)	Conditions	T_A=-40 to +85°C, T_J=-40 to +125°C			Unit
				Min.	Typ.	Max.	
V_{OST}	Startup Overshoot[13]	3.0 to 4.4	I_{LDO}=1 mA		0		%
PkV_{LINE}	Line Transient Response[13]	3.0 to 4.4	600 mV, Rise=Fall=30 µs		±85		mV
PkV_{LOAD}	Load Transient Response[13]	3.0 to 4.4	I_{LDO}=1-300 mA-1 mA, Rise=Fall=1 µs		±200		mV
V_{REF}	Reference Output Voltage for Internal Use	3.0 to 4.4	I_{REF}<1 µA		0.6		V
R_{DSCHG}	Discharge Programmable Turn-On Resistor	3.0 to 4.4	LDOx_ctrl [LDOx_DSCHG]=1		100		Ω
			LDOx_ctrl [LDOx_DSCHG]=0	3.4	4.8		MΩ
T_{SHTDN}	Thermal Shutdown Temperature[13]	3.0 to 4.4			148		°C
			Hysteresis		12		°C

Note:
13. Limits based on electrical characterization data.

12.6. Power Path

Symbol	Parameter		T_A=-40 to +85°C, T_J=-40 to +125°C			Unit
			Min.	Typ.	Max.	
V_{BUS_REG}	V_{BUS_IN} Threshold for Active V_{BUS_IN} Regulation		4.1	4.3	4.7	V
V_{BUSVTR}	V_{BUS_IN} Valid Rising Threshold for Charging when V_{BUS_IN} Regulation is Disabled		3.4	3.7	4.0	V
V_{BUSVTF}	V_{BUS_IN} Valid Falling Threshold for Charging when V_{BUS_IN} Regulation is Disabled			3.6		V
V_{BUSOVP}	V_{BUS_IN} Over-Voltage Protection (Programmable OVP = 7.0 V)		6.5	7.0	7.6	V
	Hysteresis (Programmable OVP = 7.0 V)			150		mV
I_{VBUS}	V_{BUS_IN} Current	V_{BUS}=5.5 V, Charger Ctrl1[Charger_EN]=0, LDO1_Ctrl[LDO1_EN]=0, LDO2_Ctrl[LDO2_EN]=0			1000	µA

12.7. Linear Charger

Symbol	Parameter	Conditions	T_A=-40 to +85°C, T_J=-40 to +125°C			Unit
			Min.	Typ.	Max.	
V_{OREG}	Constant Voltage Regulation Accuracy	T_A=25°C	-1.0		1.0	%
		T_A=-40°C to 85°C	-2.0		2.0	%
	Constant Voltage Regulation Range		4.00		4.35	V
I_{SHORT}	Pre-Charge Accuracy		-15		15	%
	Pre-Charge Current		65		98	mA
V_{SHORT}	Pre-Charge Termination Voltage	V_{BAT} Rising	2.2	2.5	2.8	V
	Pre-Charge Hysteresis			150		mV
t_{OCHG}	Soft-Start Ramp Time	Pre-qualified Current of 90 mA to Fast Charge Current		1.2		ms
$I_{OCHARGE}$	Fast Charge Current at Low Current	Charger Ctrl3[Auto_FC]=0	80	92	108	mA
	Fast Charge Current Accuracy		-10		10	%
	Fast Charge Current Range	Charger Ctrl3[Auto_FC]=1 Charger Ctrl3[FC_Current] Bit's Control Current	200		950	mA

Symbol	Parameter	Conditions	T_A=-40 to +85°C, T_J=-40 to +125°C			Unit
			Min.	Typ.	Max.	
I_{TERM}	End of Charge Current Accuracy Based on Fast Charge Current setting	EOC>120 mA	-1		1	%
V_{TERM}	Recharge Threshold, $V_{BAT} – V_{OREG}$	Charger Ctrl1[Recharge]=1		-150		mV
t_{TERM}	Recharge Debounce Time	Charger Ctrl1[Recharge]=1		60		ms
t_{ACC}	Timer Tolerance		-10		+10	%
t_{TOPOFF}	Top-Off Timer	Charger Ctrl2[TopOff_EN]=1		30		min
t_{DBP}	Dead-Battery Provision Timer	Charger Ctrl1[DBP_EN]=1		30	45	min
$t_{ELAPSED}$	Total Elapsed Charging Time	Charger Ctrl2[TC_Time]=00		5		hrs
		TC_Time=01		6		hrs
		TC_Time=10		7		hrs
		TC_Time=11		Disabled		
V_{WB}	Weak-Battery Threshold	Charger Ctrl2[WB_Threshold]=001	2.5	2.7	2.9	V
		Charger Ctrl2[WB_Threshold]=010	2.7	2.9	3.1	
		Charger Ctrl2[WB_Threshold]=011 (Default Setting)	2.9	3.1	3.3	
		Charger Ctrl2[WB_Threshold]=100	3.1	3.3	3.5	
		Charger Ctrl2[WB_Threshold]=101	3.3	3.5	3.7	
		Charger Ctrl2[WB_Threshold]=110	3.5	3.7	3.9	
$T_{SHUTDOWN}$	Thermal Shutdown(14)			145		°C
	Hysteresis(14)			5		°C
T_{REG}	Thermal Regulation(14)			120		°C
R_{VICHG}	VICHG Internal Resistance			15		kΩ
I_{VICHG}	VBUS Current-to-Voltage Translation for VICHG	I_{BAT}=50 mA		88		mV
		I_{BAT}=500 mA		875		mV

Note:
14. Limits based on electrical characterization data.

12.8. Current Consumption

Symbol	Parameter	V_{BAT} (V)	Conditions	T_A=-40 to +85°C			Unit
				Min.	Typ.	Max.	
I_{BATS}	Battery Supply Standby Mode Current	3.0 to 4.4	No Accessory Attached, V_{BUS}=0 V, LDO1_EN=0, LDO2_EN=0, REF_EN=0		15	25	µA
I_{BATSA}	Battery Supply Standby Mode Current with Accessory Attached	3.8	ID Not Floating, No VBUS, LDOs Off, GPOs Off, All Switches Open, Accessory Attached (Excluding Factory Modes)		30		µA
I_{BATSL}	Battery Supply Standby Mode Current with One LDO On	3.8	ID Floating, No VBUS, One LDO On (3.3 V), Other LDO Off, GPOs Off, All Switches Open, No Accessory Attached		65		µA

12.9. Timing

Symbol	Parameter	Reference Diagram	T_A=-40 to +85°C, T_J=-40 to +125°C			Unit
			Min.	Typ.	Max.	
t_{SW}	Time After *INT Mask* Cleared to “0” until INT_N Goes LOW to Signal the Interrupt after Interruptible Event while *INT Mask* Bit Set to 1	Figure 7, Figure 8		10		ms
t_{SDPDET}	Time from V_{BUS_IN} Valid to USB Switches Closed for USB Standard Downstream Port	Figure 13		130		ms
t_{IDDET}	Time from ID Based Accessory Attached to INT_N Driven LOW			5		ms
t_{CHRG_DET}	Time from V_{BUS_IN} Valid to USB Switches Closed for USB Charging Downstream Port (CDP)	Figure 14		170		ms
t_{VBUS_CHG}	Time from V_{BUS_IN} Valid to Charger Active, Assuming Charger Enabled	Figure 14	150			ms
t_{CHG_EN}	Time from Charger_EN=1 to Charger Active with V_{BUS} Valid			20		ms
t_{DCD}	Time from V_{bus_valid} to DCD Detection Complete, Assuming Contact	Figure 14		20		ms
t_{CHRG_FLOW}	Time from DCD Complete to Charger Detection Complete	Figure 14		150		ms
t_{ID_FLOW}	Time from DCD Complete to ID Detection Complete			200		ms
$t_{JIGVBUS}$	Time from V_{BUS_IN} Valid to JIG LOW for Both Factory Mode Operation with V_{BUS_IN} Present	Figure 15		200		ms
$t_{JIGNOVBUS}$	Time from ID Attach to JIG LOW for Factory Mode Operation without V_{BUS_IN} Present	Figure 16		200		ms

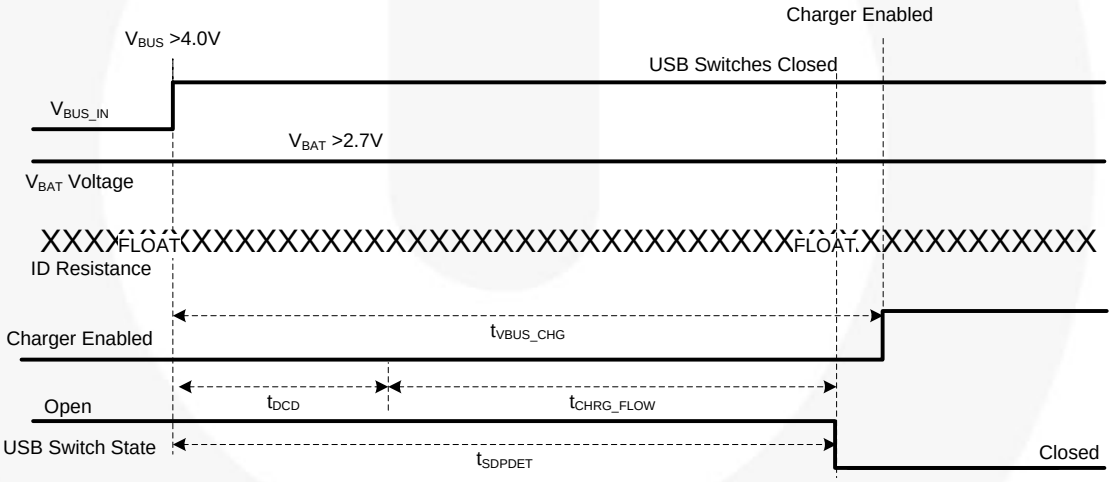


Figure 13. USB Standard Downstream Port Attach Timing

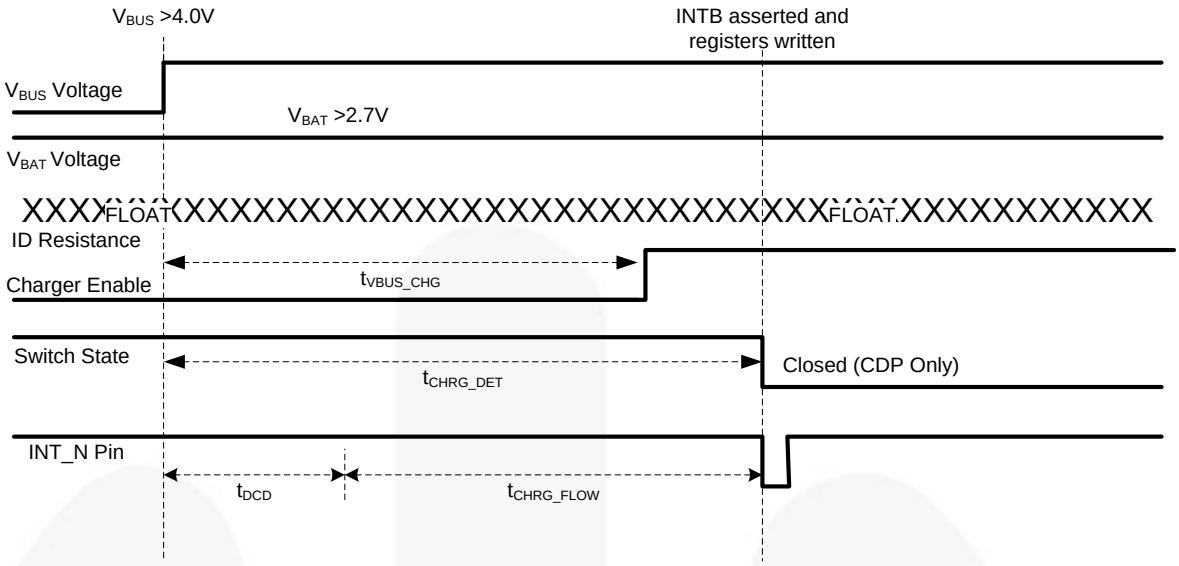


Figure 14. USB Charging Ports (DCP, CDP) Attach Timing

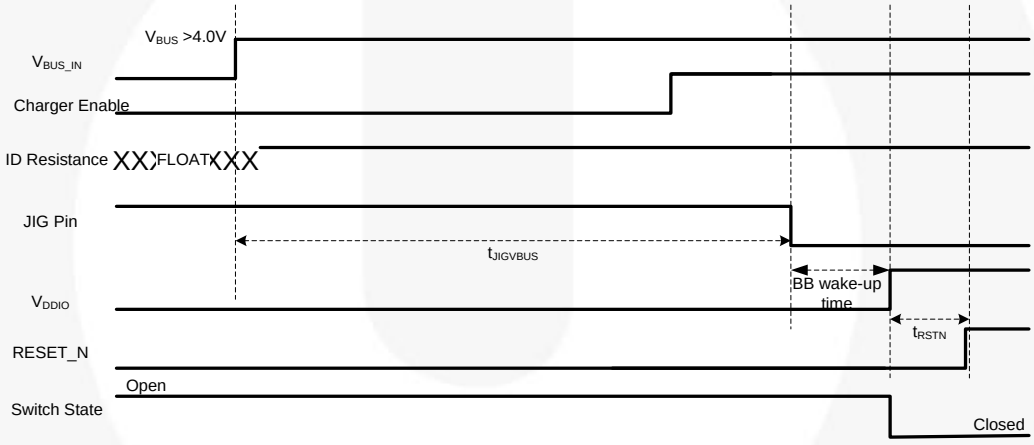


Figure 15. Jig Box Attach Timing (V_{bus_IN} Valid)

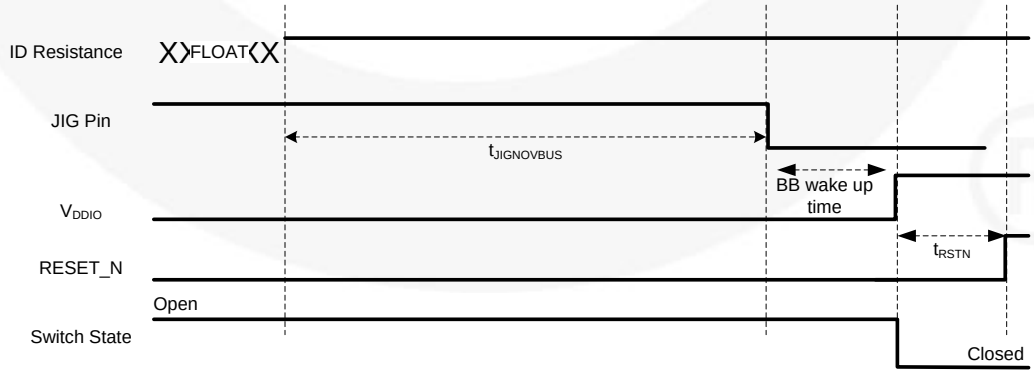


Figure 16. JIG Box Attach Timing without V_{BUS_IN}

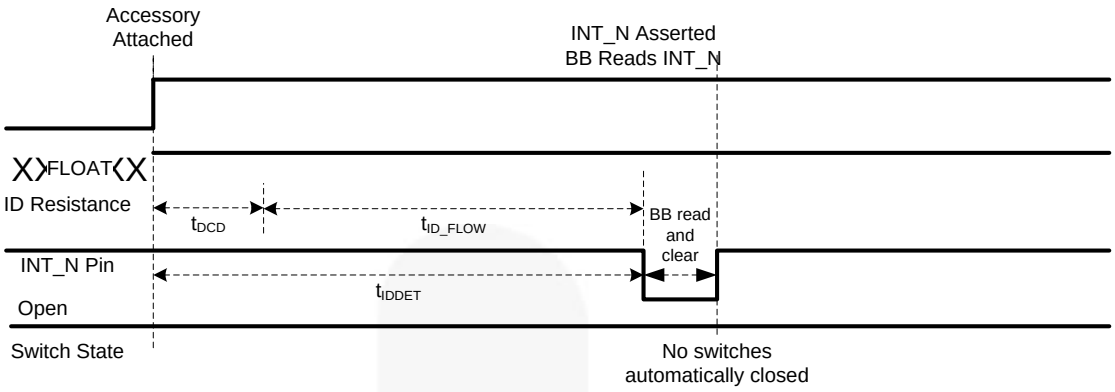


Figure 17. Unknown ID Timing

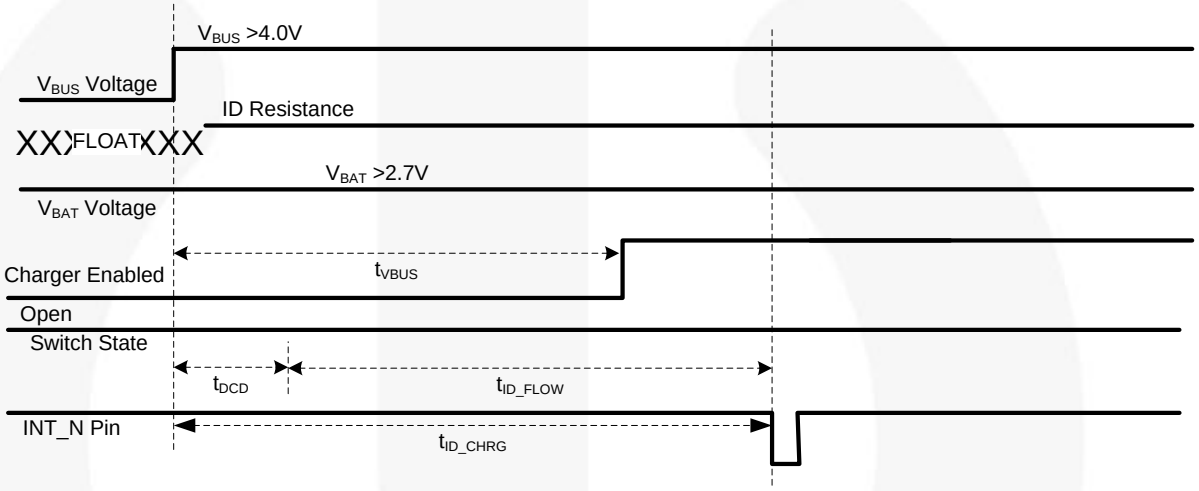


Figure 18. Car Kit Charger and TA Timing

12.10. AC Characteristics

Unless otherwise specified: recommended T_A and T_J temperature ranges. All typical values are at T_A=25°C unless otherwise specified.

Symbol	Parameter	Conditions	T_A=-40 to +85°C			Unit
			Min.	Typ.	Max.	
Xtalk	Active Channel Crosstalk DP_CON to DM_CON(15)	f=1 MHz, R_T=50 Ω, C_L=0 pF		-60		dB
		f=240 MHz, R_T=50 Ω, C_L=0 pF		-30		
O_{IRR}	Off Isolation Rejection Ratio, DM_HOST to DM_CON, DP_HOST to DP_CON(15)	f=1 MHz, R_T=50 Ω, C_L=0 pF		-60		dB
		f=240 MHz, R_T=50 Ω, C_L=0 pF		-30		dB

Note:
15. Limits based on electrical characterization data.

12.11. Capacitance

Symbol	Parameter	V_{BAT} (V)	Conditions	T_A=-40 to +85°C			Unit
				Min.	Typ.	Max.	
C_{ONUSB}	DP_CON, DM_CON ON Capacitance (USB Mode) (16)	3.8	V_{BIAS}=0.2 V, f=1 MHz		8		pF
		3.8	V_{BIAS}=0.2 V, f=240 MHz		8		pF
C_I	Capacitance for Each I/O Pin(16)	3.8	f=1 MHz		5		pF

Note:
16. Limits based on electrical characterization data.

12.12. I²C AC Electrical Characteristics

Symbol	Parameter	Fast Mode		Unit
		Min.	Max.	
f_{SCL}	I2C_SCL Clock Frequency	0	400	kHz
$t_{HD;STA}$	Hold Time (Repeated) START Condition	0.6		µs
t_{LOW}	LOW Period of I2C_SCL Clock	1.3		µs
t_{HIGH}	HIGH Period of I2C_SCL Clock	0.6		µs
$t_{SU;STA}$	Set-up Time for Repeated START Condition	0.6		µs
$t_{HD;DAT}$	Data Hold Time	0	0.9	µs
$t_{SU;DAT}$	Data Set-up Time(17)	100		ns
t_r	Rise Time of I2C_SDA and I2C_SCL Signals(17,18)	20+0.1C_b	300	ns
t_f	Fall Time of I2C_SDA and I2C_SCL Signals(17,18)	20+0.1C_b	300	ns
$t_{SU;STO}$	Set-up Time for STOP Condition	0.6		µs
t_{BUF}	BUS-Free Time between STOP and START Conditions	1.3		µs
t_{SP}	Pulse Width of Spikes that Must Be Suppressed by the Input Filter	0	50	ns

Notes:

17. A fast-mode I²C Bus® device can be used in a Standard-Mode I²C Bus system, but the requirement $t_{SU;DAT} \geq$ 250 ns must be met. This is automatically the case if the device does not stretch the LOW period of the I2C_SCL signal. If a device does stretch the LOW period of the I2C_SCL signal, it must output the next data bit to the I2C_SDA line $t_{r\_max} + t_{SU;DAT}$=1000 + 250=1250 ns (according to the Standard-Mode I²C bus specification) before the I2C_SCL line is released.
18. C_b equals the total capacitance of one bus line in pF. If mixed with high-speed devices, faster fall times are allowed by the I²C specification.

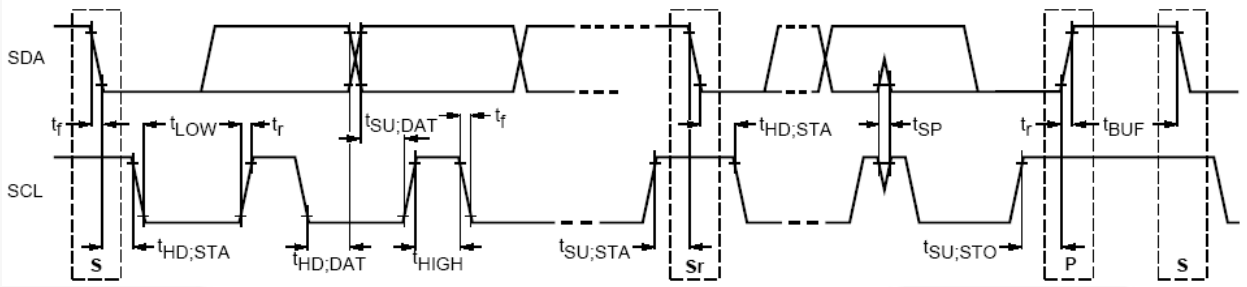


Figure 19. Definition of Timing for Full-Speed Mode Devices on the I2C Bus®

Table 9. I²C Slave Address

Name	Size (Bits)	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Slave Address	8	0	1	0	0	1	0	1	R/W

12.13. USB Eye Compliance

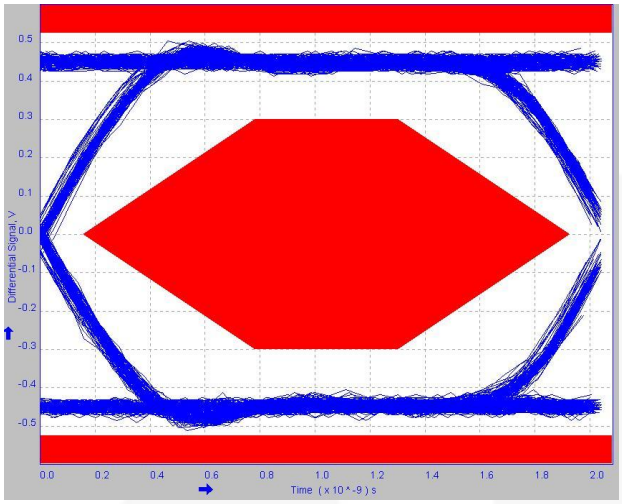


Figure 20. HS Pass-Through Eye Compliance Testing Input Signal

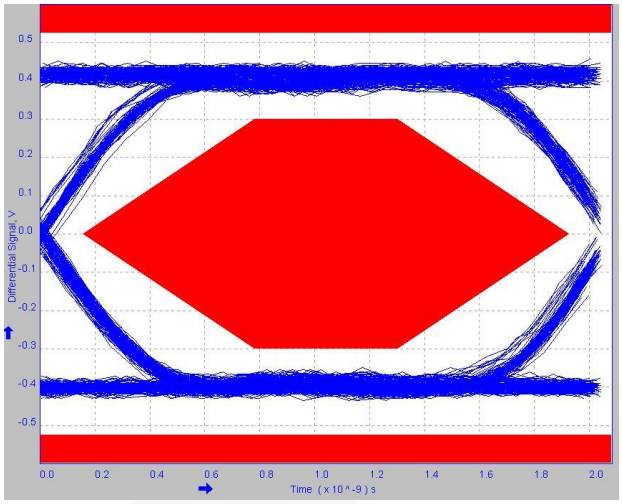


Figure 21. HS USB 2.0 Eye Compliance Test Results at Output (T_A=85°C)

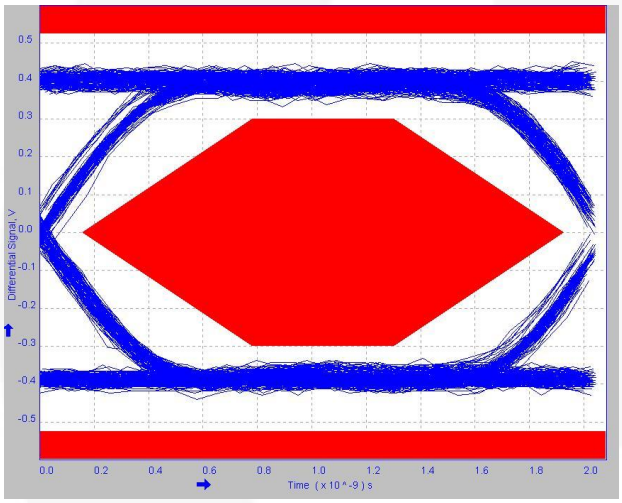


Figure 22. HS USB 2.0 Eye Compliance Test Results at Output (T_A=25°C)

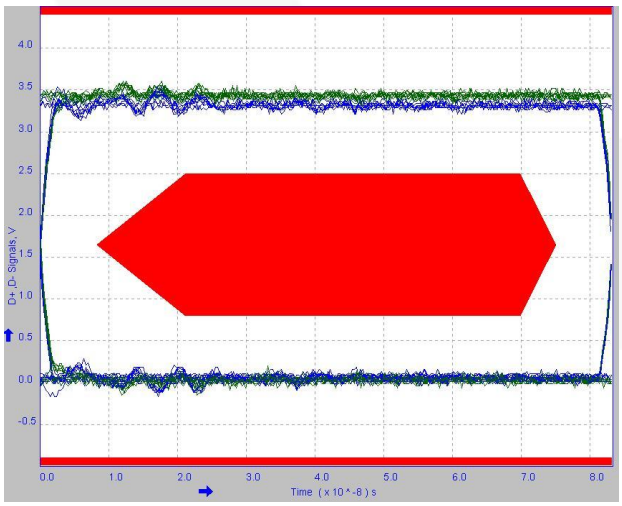


Figure 23. FS Pass-Through Eye Compliance Testing Input Signal

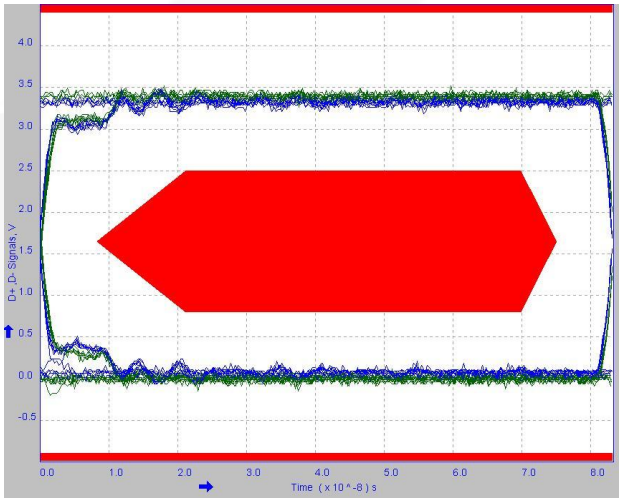


Figure 24. FS USB 2.0 Eye Compliance Test Results at Output (T_A=25°C)

12.14. Programmability Tables

Register descriptions in **BOLD** reflect the default state of the register.

Table 10. Register Addresses

Address	Register Name	Type	Reset Value	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
01H	Device ID	R	N/A	Revision Number					Vendor ID		
02H	Control	R/W	Xxxx_0101					Switch Open	Auto Config	DCD TO Disable	INT Mask
03H	Interrupt 1	R/C	0000_0000	TSD_EN	OVP_EN	TREG_EN	TC_TO	DBP_TO	Bat_Charged	Detach	Attach
04H	Interrupt 2	R/C	000x_x0x0	TSD_DIS	OVP_DIS	TREG_DIS			TRECOVER		TSD_LDO
05H	Interrupt Mask 1	R/W	0000_0000	TSD_EN	OVP_EN	TREG_EN	TC_TO	DBP_TO	Bat_Charged	Detach	Attach
06H	Interrupt Mask 2	R/W	000x_x0x0	TSD_DIS	OVP_DIS	TREG_DIS			TRECOVER		TSD_LDO
07H	ADC	R	Xxx1_1111				ADC Value				
08H	Status 1	R	1xxx_xx0x	ON_KEY_N						V_{BUS_VALID}	
09H	Device Type1	R	0000_0000	Car Kit Type 1 and TA Charger	Jig USB Off	Jig USB On	Jig UART Off	Jig UART On	USB Charger (CDP)	Dedicated Charger (DCP)	Standard USB (SDP)
0AH	Device Type2	R	Xxxx_xxx0								Unknown Accessory
0BH	GPO	R/W	Xxx0_0000				REF_EN	GPO1_OD	GPO2_OD	GPO1	GPO2
0CH	LDO1_Ctrl	R/W	01xx_0100	LDO1_EN	LDO1_ DSCHG			LDO1_Voltage			
0DH	LDO2_Ctrl	R/W	01xx_0100	LDO2_EN	LDO2_ DSCHG			LDO2_Voltage			
0EH	Charger Ctrl1	R/W	X010_1111		V_{BUS} Reg Dis	VICHG_EN	AutoStop	TC_EN	TopOff_EN	Charger_EN	DBP_EN
0FH	Charger Ctrl2	R/W	X001_0011		TC_Time		OVP_Threshold		WB_Threshold		
10H	Charger Ctrl3	R/W	10xx_0101	Auto_FC	FC_ Override			FC_Current			
11H	Charger Ctrl4	R/W	Xxxx_0000					EC_Current			
12H	Charger Ctrl5	R/W	Xxxx_1000					CV_Voltage			
13H	Manual Switch	R/W	0000_00x0	D- Switching			D+ Switching				JIG ON
14H	Reset	R/W	Xxxx_xx00							LC Reset	Reset
15H-26H	Reserved			Reserved							
27H	Interrupt 3	R/C								EOC	VBUS_CHG
28H	Interrupt Mask 3	R/W								EOC	VBUS_CHG

Notes:

19. Do not use registers that are blank.
20. Write 0 to undefined register bits.
21. Values read from undefined register bits are not defined and invalid.

Table 11. Device ID

Address: 01h

Type: Read Only

Bit #	Name	Size (Bits)	Description
7:3	Revision Number	5	Rev 2.0=10100
2:0	Vendor ID	3	000: Fairchild Semiconductor

Table 12. Switch Control

Address: 02h

Reset Value: xxxx_0101

Type: Read/Write

Bit #	Name	Size (Bits)	Description
7:4	DoNotUse	4	N/A
3	Switch Open	1	1: Opens all switches 0: Does not open all switches
2	Auto Config	1	1: Automatic switching (also called auto-configuration) 0: Manual switching
1	DCD TO Disable	1	1: Keeps checking DCD as long as V_{bus_valid} and id_float 0: If DCD check times out (450ms typical), completes standard charger detection
0	INT Mask	1	1: Mask interrupt – does not interrupt baseband processor 0: Unmask interrupt – interrupts baseband processor on change of state in Interrupt register

Table 13. Interrupt 1

Address: 03h

Reset Value: 0000_0000

Type: Read/Clear

Bit #	Name	Size (Bits)	Description
7	TSD_EN	1	1: Thermal shutdown event has occurred and charger is disabled 0: No thermal shutdown event occurred
6	OVP_EN	1	1: OVP event 0: No OVP event
5	TREG_EN	1	1: Thermal regulation causing current limiting to lower die temperature below threshold 0: No thermal regulation is occurring
4	TC_TO	1	1: Total charging timeout occurred 0: Total charging timeout has not occurred
3	DBP_TO	1	1: Dead-battery provision timeout occurred 0: No dead-battery provision timeout occurred
2	Bat_Charged	1	1: Battery fully charged with top-off timer expired if enabled 0: Battery not fully charged or linear charger is not active
1	Detach	1	1: Accessory detached 0: Accessory not detached
0	Attach	1	1: Accessory attached 0: Accessory not attached

Table 14. Interrupt 2

Address: 04h

Reset Value: 000x_x0x0

Type: Read/Clear

Bit #	Name	Size (Bits)	Description
7	TSD_DIS	1	1: Thermal Shutdown (TSD) event has recovered for linear charger 0: TSD event not recovered or never existed for linear charger
6	OVP _DIS	1	1: Over-Voltage Protection (OVP) event has recovered for linear charger 0: OVP event not recovered or never existed for linear charger
5	TREG_DIS	1	1: Thermal Regulation (TREG) event has recovered for linear charger 0: TREG event not recovered or never existed for linear charger
4:3	DoNotUse	2	N/A
2	TRECOVER	1	1: Thermal Shutdown (TSD) event has recovered for LDO1 or LDO2 0: TSD event not recovered or never existed for LDO or LDO2
1	DoNotUse	1	N/A
0	TSD_LDO	1	1: TSD event has occurred for either LDO and both LDOs are disabled 0: No TSD event has occurred for LDO1 or LDO2

Table 15. Interrupt Mask 1

Address: 05h

Reset Value: 0000_0000

Type: Read/Write

Bit #	Name	Size (Bits)	Description
7	TSD_EN	1	1: Interrupt in Interrupt Register is masked and does not interrupt processor 0: Interrupt in Interrupt Register is not masked and, when active, interrupts processor
6	OVP_EN	1	
5	TREG_EN	1	
4	TC_TO	1	
3	DBP_TO	1	
2	Bat_Charged	1	
1	Detach	1	
0	Attach	1	

Table 16. Interrupt Mask 2

Address: 06h

Reset Value: 000x_x0x0

Type: Read/Write

Bit #	Name	Size (Bits)	Description
7	TSD_DIS	1	1: Interrupt in Interrupt Register is masked and does not interrupt processor 0: Interrupt in Interrupt Register is not masked and when active interrupts processor
6	OVP_DIS	1	
5	TREG_DIS	1	
4:3	DoNotUse	2	
2	TRECOVER	1	
1	DoNotUse	1	
0	TSD_LDO	1	

Table 17. ADC

Address: 07h

Reset Value: xxx1_1111

Type: Read Only

Bit #	Name	Size (Bits)	Description
7:5	DoNotUse	3	N/A
4:0	ADC Value	5	ADC value read from ID: 10101: Unknown Accessory 10110: Unknown Accessory 10111: Car Kit Type 1 Charger 11000: Factory Mode Boot OFF-USB 11001: Factory Mode Boot ON-USB 11010: Unknown Accessory 11011: Unknown Accessory 11100: Factory Mode Boot OFF-UART 11101: Factory Mode Boot ON-UART 11110: Unknown Accessory 11111: No Accessory or USB Accessory Detected

Table 18. Status 1

Address: 08h

Reset Value: 1xxx_xx0x

Type: Read

Bit #	Name	Size (Bits)	Description
7	ON_KEY_N	1	1: ON_KEY_N is HIGH 0: ON_KEY_N is LOW
6:2	DoNotUse	5	N/A
1	V_{BUS}_Valid	1	1: Valid V_{BUS_IN} detected for accessory detection 0: No V_{BUS_IN} detected
0	DoNotUse	1	N/A

Table 19. Device Type 1

Address: 09h

Reset Value: 0000_0000

Type: Read

Bit #	Name	Size (Bits)	Description
7	Car kit Type 1 & TA Charger	1	1: Car Kit Type 1 or Travel Adapter (TA) detected 0: Car Kit Type 1 or Travel Adapter (TA) not detected
6	JIG_USB_OFF	1	1: Factory mode cable BOOT OFF – USB detected 0: Factory mode cable BOOT OFF – USB not detected
5	JIG_USB_ON	1	1: Factory mode cable BOOT ON – USB detected 0: Factory mode cable BOOT ON - USB not detected
4	JIG_UART_OFF	1	1: Factory mode cable BOOT OFF – UART detected 0: Factory mode cable BOOT OFF - UART not detected
3	JIG_UART_ON	1	1: Factory mode cable BOOT ON – UART detected 0: Factory mode cable BOOT ON - UART not detected
2	USB Charger (CDP)	1	1: USB Charging Downstream Port (CDP) charger detected 0: USB Charging Downstream Port (CDP) charger not detected
1	Dedicated Charger (DCP)	1	1: USB Dedicated Charging Port (DCP) charger detected 0: USB Dedicated Charging Port (DCP) charger not detected
0	Standard USB (SDP)	1	1: USB Standard Downstream Port (SDP) detected 0: USB Standard Downstream Port (SDP) not detected

Table 20. Device Type 2

Address: 0Ah

Reset Value: xxxx_xxx0

Type: Read

Bit #	Name	Size (Bits)	Description
7:1	DoNotUse	6	N/A
0	Unknown Accessory	1	1: Unknown accessory detected 0: Unknown accessory not detected

Table 21. GPO

Address: 0Bh

Reset Value: xxx0_0000

Type: Read/Write

Bit #	Name	Size (Bits)	Description
7:5	DoNotUse	3	N/A
4	REF_EN	1	1: Enable 0.6V reference voltage on V_{REF} pin 0: Disable 0.6V reference voltage on V_{REF} pin
3	GPO1_OD	1	1: GPO1 is an open-drain output 0: GPO1 is a CMOS push-pull output
2	GPO2_OD	1	1: GPO2 is an open-drain output 0: GPO2 is a CMOS push-pull output
1	GPO1	1	1: GPO1 output is a HIGH (Hi-Z if GPO1_OD is HIGH) 0: GPO1 output is a LOW
0	GPO2	1	1: GPO2 output is a HIGH (Hi-Z if GPO2_OD is HIGH) 0: GPO2 output is a LOW

Table 22. LDO1_Ctrl

Address: 0Ch

Reset Value: 01xx_0100

Type: Read/Write

Bit #	Name	Size (Bits)	Description		
7	LDO1_EN	1	1: Enable LDO1 output with the voltage programmed by LDO1_Voltage 0: Disable LDO1 output		
6	LDO1_DSCHG	1	1: Enable discharge resistor to actively discharge LDO1 output(22) 0: Disable discharge resistor		
5:4	Reserved	2	N/A		
3:0	LDO1_Voltage	4	Voltage Programmed on the LDO1 Output(23)		
			0000: Bypass 0001: 3.6 0010: 3.5 0011: 3.4 0100: 3.3 0101: 3.2	0110: 3.1 0111: 3.0 1000: 2.9 1001: 2.8 1010: 2.7 1011: 2.6	1100: 2.5 1101: 2.4 1110: 2.0 1111: 1.8

Notes:

22. The FSA9591 checks the status of LDO1_EN before enabling the discharge resistors. LDO1_EN is required to be LOW before the discharge resistors are enabled.
23. It is possible to program the LDO output voltage above the V_{BAT} level; in which case, the LDO is not regulated and the performance of the LDO is compromised. This is not recommended.

Table 23. LDO2_Ctrl

Address: 0Dh

Reset Value: 01xx_0100

Type: Read/Write

Bit #	Name	Size (Bits)	Description		
7	LDO2_EN	1	1: Enable LDO2 output with the voltage programmed by LDO2_Voltage 0: Disable LDO2 output		
6	LDO2_DSCHG	1	1: Enable discharge resistor to actively discharge LDO2 output(24) 0: Disable discharge resistor		
5:4	Reserved	2	N/A		
3:0	LDO1_Voltage	4	Voltage Programmed on the LDO1 Output(25)		
			0000: Bypass 0001: 3.6 0010: 3.5 0011: 3.4 0100: 3.3 0101: 3.2	0110: 3.1 0111: 3.0 1000: 2.9 1001: 2.8 1010: 2.7 1011: 2.6	1100: 2.5 1101: 2.4 1110: 2.0 1111: 1.8

Notes:

24. The FSA9591 checks the status of LDO1_EN before enabling the discharge resistors. LDO1_EN is required to be LOW before the discharge resistors are enabled.
25. It is possible to program the LDO output voltage above the V_{BAT} level; in which case, the LDO is not regulated and the performance of the LDO is compromised. This is not recommended.

Table 24. Charger Ctrl1

Address: 0Eh

Reset Value: x010_1111

Type: Read/Write

Bit #	Name	Size (Bits)	Description
7	DoNotUse	1	N/A
6	V_{BUS}_Reg_Dis	1	1: V_{BUS_IN} regulation loop disabled 0: V_{BUS_IN} regulation loop enabled
5	VICHG_EN	1	1: VICHG reference output is enabled 0: VICHG reference output is not enabled
4	AutoStop	1	1: Stop charging after top-off timer expires 0: AutoStop must be enabled by writing this bit HIGH prior to charging occuring.
3	TC_EN	1	**1: Enable timer for total charging elapsed time** (default) 0: Disable timer for total charging elapsed time
2	TopOff_EN(26)	1	**1: Enable battery top-off timer for 30 minutes after end-of-charge termination current is detected** (default) 0: Disable top-off timer
1	Charger_EN	1	**1: Enable charger when V_{BUS_Valid} is detected** (default) 0: Disable charger
0	DBP_EN(27,28)	1	1: Enable Dead-Battery Provision Mode (default until processor has a valid operating voltage) 0: Disable Dead-Battery Provision Mode (not USB compliant)

Notes:

26. The top-off timer is reset if an OVP event occurs. The top-off timer is not reset if I_{BAT} increases above EOC threshold after started.
27. Dead-battery timer starts when a charger is attached and the battery is below the weak-battery threshold. A dead-battery timeout occurs when the timer expires and V_{BAT} is still below the weak-battery threshold.
28. The dead battery timer is not reset if an OVP event occurs.

Table 25. Charger Ctrl2

Address: 0Fh

Reset Value: x000_1011

Type: Read/Write

Bit #	Name	Size (Bits)	Description
7	DoNotUse	1	N/A
6:5	TC_Time[29,30]	2	Total elapsed charging time threshold: **00: 5 hours** (default setting) 01: 6 hours 10: 7 hours 11: No time limit
4:3	OVP_Threshold	2	V_{BUS} Over-Voltage Protection threshold: 00: 6.5 V **01: 7.0 V** (default setting) 10: 7.5 V 11: 8.0 V
2:0	WB_Threshold	3	Weak battery threshold[31] 000: Reserved 001: 2.7 V 010: 2.9 V **011: 3.1 V** (default setting) 100: 3.3 V 101: 3.5 V 110: 3.7 V 111: Reserved

Notes:

29. Changing the TC_TIME while the charger is active does not restart the timer and can cause an immediate timeout, depending on the current state of the timer. For example, if the timer is programmed to 7 hours (0x10) and the timer is at 6 hourrs, programming the timer to 5 hours (0x00) causes a timeout to occur.
30. The TC_TIME timer is not reset if an OVP event is detected or Vbus_in falls below the Vbus_valid threshold.
31. This threshold is checked at the completion of the dead-battery timer. If DBP_EN=1 and V_{BAT} is below the threshold, then a DBP_TO occurs.

Table 26. Charger Ctrl3

Address: 10h

Reset Value: 11xx_0101

Type: Read/Write

Bit #	Name	Size (Bits)	Description
7	Auto_FC	1	1: Automatically detect charger and increase fast charge current to the default FC_Current in Charger Ctrl2[FC_Current] if charger detected 0: Use 90mA fast charge current to continue charging after the pre-qualification stage
6	FC_Override	1	1: Always use programmed FC_Current regardless of Auto_FC programming 0: Follow USB current requirements based on accessory detection and Auto_FC
5:4	DoNotUse	2	N/A
3:0	FC_Current	4	Fast charge current level if Charger_Ctrl3[Auto_FC]=1 and charger is attached or if Charger_Ctrl3 [FC_Override]=1: 0000: 200 mA 0001: 250 mA 0010: 300 mA 0011: 350 mA 0100: 400 mA **0101: 450 mA** (default) 0110: 500 mA 0111: 550 mA 1000: 600 mA 1001: 650 mA 1010: 700 mA 1011: 750 mA 1100: 800 mA 1101: 850 mA 1110: 900 mA 1111: 950 mA

Table 27. Charger Ctrl4

Address: 11h

Reset Value: xxxx_0000

Type: Read/Write

Bit #	Name	Size (Bits)	Description
7:4	DoNotUse	4	N/A
3:0	EC_Current[32]	4	End-of-charge current level[33]. If the current is below this level in the constant voltage stage of charging, the charger progresses to top off if enabled or is disabled. **0000: 20 mA** (default setting) 0001: 30 mA 0010: 40 mA 0011: 50 mA 0100: 60 mA 0101: 70 mA 0110: 80 mA 0111: 90 mA 1000: 100 mA 1001: 110 mA 1010: 120 mA 1011: 130 mA 1100: 140 mA 1101: 150 mA 1110: 160 mA 1111: 170 mA

Notes:

32. Setting EC_Current below 120 mA is not recommended.
33. The end-of-charge current can be set above the fast charge current. This is not recommended.

Table 28. Charger Ctrl5

Address: 12h

Reset Value: xxxx_1000

Type: Read/Write

Bit #	Name	Size(Bits)	Description
7:4	DoNotUse	4	N/A
3:0	CV_Voltage	4	Constant voltage level. Charger maintains constant voltage when V_{BAT} is this level: 0000: 4.00 V 0001: 4.04 V 0010: 4.08 V 0011: 4.10 V 0100: 4.12 V 0101: 4.14 V 0110: 4.16 V 0111: 4.18 V **1000: 4.20 V** (default setting) 1001: 4.22 V 1010: 4.24 V 1011: 4.26 V 1100: 4.28 V 1101: 4.30 V 1110: 4.32 V 1111: 4.35 V

Table 29. Manual S/W[34]

Address: 13h

Reset Value: 000000x0

Type: Read/Write

Bit #	Name	Size(Bits)	Description
7:5	DM_CON Switching	3	**000: Open switch** 001: DM_CON connected to DM_HOST of USB port 011: DM_CON connected to TxD_HOST of UART port All other values: DoNotUse
4:2	DP_CON Switching	3	**000: Open switch** 001: DP_CON connected to DP_HOST of USB port 011: DP_CON connected to RxD_HOST of UART port All other values: DoNotUse
1	DoNotUse	1	N/A
0	JIG_ON[35]	1	1: JIG output=GND 0: JIG output=High Impedance

Notes:

34. When switching between manual switch configurations on a single attach, the accessory must pass through an “000: Open Switch” state between configurations. Manual Modes must have an accessory attached prior to operation. The FSA9591 does not configure per the Manual Modes register if an accessory has not been previously attached.
35. In normal operation, the JIG pin is used in the logic to drive the ON_BT_UP pin. When in Manual Mode, the JIG pin is not used in the logic to drive the ON_BT_UP pin.

Table 30. Reset

Address: 14h

Reset Value: xxxx_xx00

Type: Write/Clear

Bit #	Name	Size (Bits)	Description
7:2	DoNotUse	6	N/A
1	LC_Reset	1	1: Resets the linear charger (upon reset, this bit clears itself) 0: Does not reset
0	Reset	1	1: Resets the detection logic (upon reset, this bit clears itself) 0: Does not reset

Table 31. Interrupt 3

Address: 27h

Reset Value: xxxx_xx00

Type: Read/Clear

Bit #	Name	Size (Bits)	Description
7:2	DoNotUse	6	N/A
1	EOC(1)	1	1: EOC threshold has been reached **0: EOC threshold not reached** (default)
0	VBUS_CHG(2)	1	1: VBUS status changed. Read Status 1 register to determine the current status of VBUS **0: VBUS status has not changed** (default)

Notes:

36. VBUS_CHG interrupt is triggered every time the V_{BUS}_Valid status bit in Status 1 changes state. Typical applications have this interrupt masked prior to attach to prevent both VBUS_CHG and attach interrupt on attach. After an attach and the given accessory is detected, the application can unmask this interrupt to allow detection of powered accessories where V_{BUS} is applied after attach.
37. EOC interrupt is triggered when the EOC threshold is reached. In cases where the top-off timer is disabled, there is both a battery_charged and EOC interrupt that occur. If the top-off timer is enabled, the EOC interrupt is triggered when the top-off timer is enabled and internally masked until the top-off timer expires. This prevents multiple EOC interrupts if I_{BAT} is oscillating during the top-off time.

Table 32. Interrupt Mask 3

Address: 28h

Reset Value: xxxx_xx11

Type: Read/Write

Bit #	Name	Size (Bits)	Description
7:2	DoNotUse	6	N/A
1	EOC	1	1: Interrupt in Interrupt Register is masked and does not interrupt processor
0	VBUS_CHG	1	**0: Interrupt in Interrupt Register is not masked and, when active, interrupts processor** (default)

13. Layout Guidelines

13.1. PCB Layout Guidelines for High-Speed USB Signal Integrity

1. Place FSA9591 as close to the USB controller as possible. Shorter traces mean less loss, less chance of picking up stray noise, and less radiated EMI.
   a) Keep the distance between the USB controller and the device less than one inch (< 25 mm).
   b) For best results, this distance should be <18 mm. This keeps it less than one quarter (¼) of the transmission electrical length.
2. Use an impedance calculator to ensure 90 Ω differential impedance for DP_CON and DM_CON lines.
3. Select the best transmission line for the application.
   a) For example, for a densely populated board, select an edge-coupled differential stripline.
4. Minimize the use of vias and keep HS USB lines on same plane in the stack.
   a) Vias are an interruption in the impedance of the transmission line and should be avoided.
   b) Try to avoid routing schemes that generally force the use of at least two vias: one on each end to get the signal to and from the surface.
5. Cross lines, only if necessary, orthogonally to avoid noise coupling (traces running in parallel couple).
6. If possible, separate HS USB lines with GND to improve isolation.
   a) Routing GND, power, or components close to the transmission lines can create impedance discontinuities.
7. Match transmission line pairs as much as possible to improve skew performance.
8. Avoid sharp bends in PCB traces; a chamfer or rounding is generally preferred.
9. Place decoupling for power pins as close to the device as possible.
   a) Use low-ESR capacitors for decoupling if possible.
   b) Use a tuned PI filter to negate the effects of switching power supplies and other noise sources, if needed.

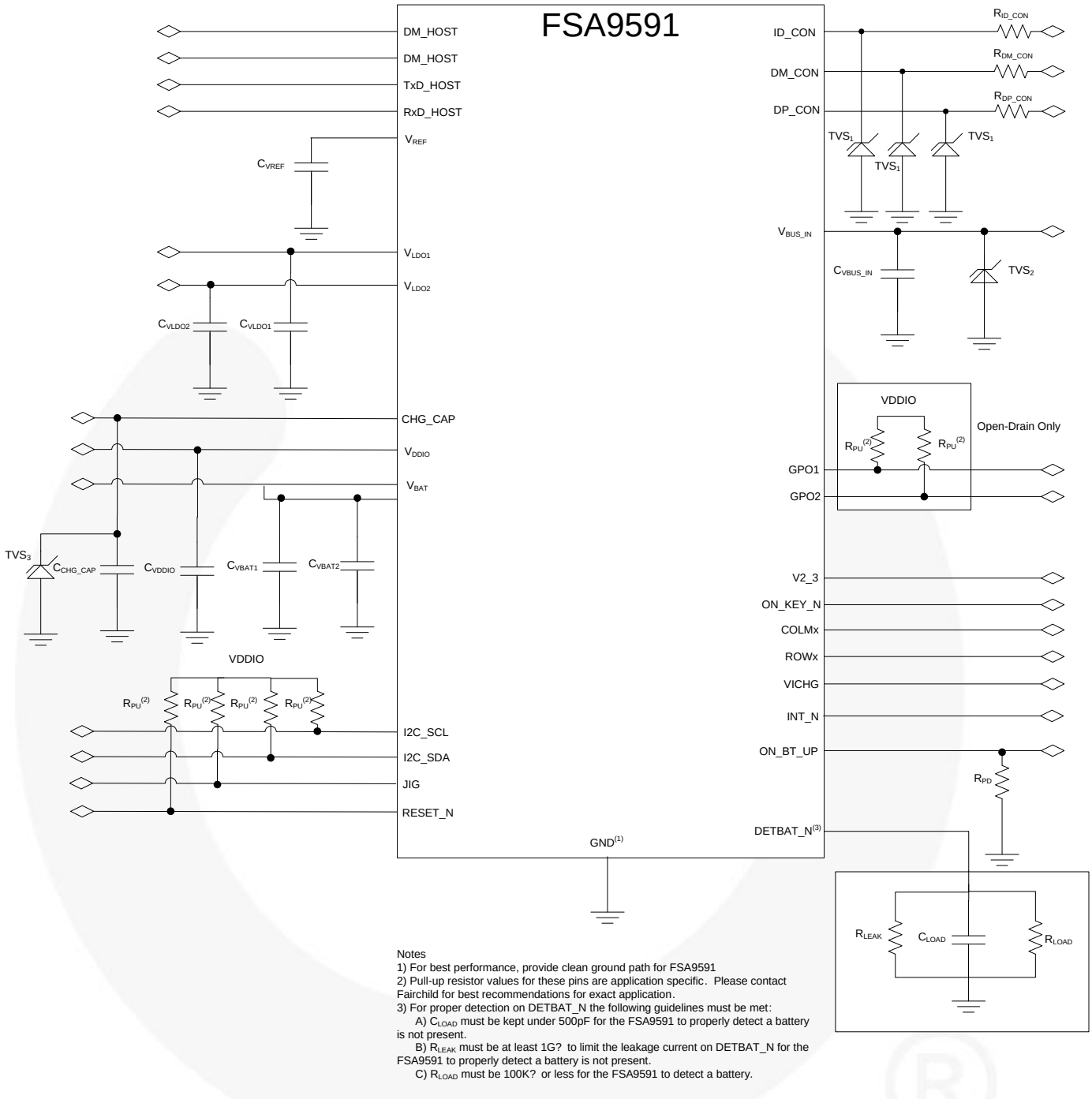
13.2. Layout for GSM / TDMA Buzz Reduction

There are two possible mechanisms for TDMA / GSM noise to negatively impact performance. The first is the result of large current draw by the phone transmitter during active signaling when the transmitter is at full or almost-full power. With the phone transmitter dumping large amounts of current in the phone GND plane; it is possible for there to be temporary voltage excursions in the GND plane if not properly designed. This noise can be coupled back through the GND plane into the FSA9591 device and, although the FSA9591 has very good isolation; if the GND noise amplitude is large enough, it can result in noise coupling to the FSA9591. The second path for GSM noise is through electromagnetic coupling onto the signal lines.

In most cases, the noise introduced as a result is on the V_{BAT} and/or GND supply rails. Following are recommendations for PCB board design that help address these two sources of TDMA / GSM noise.

1. Provide a wide, low-impedance GND return path to both the FSA9591 and to the power amplifier that sources the phone transmit block.
2. Provide separate GND connections to PCB GND plane for each device. Do not share GND return paths.
3. Add as large a decoupling capacitor as possible (≥1µF) between the V_{BAT} pin and GND to shunt any power supply noise away from the FSA9591. Also add decoupling capacitance at the power amplifier *(see reference application in Figure 1 for recommended decoupling capacitor values)*.
4. Add 33pF shunt capacitors on any PCB nodes with the potential to collect radiated energy from the phone transmitter.
5. Add a series R_{BAT} resistor prior to the decoupling capacitor on the V_{BAT} pin to attenuate noise prior to reaching the FSA9591.

14. Reference Schematic



Notes
1) For best performance, provide clean ground path for FSA9591
2) Pull-up resistor values for these pins are application specific. Please contact Fairchild for best recommendations for exact application.
3) For proper detection on DETBAT_N the following guidelines must be met:
A) C_{LOAD} must be kept under 500pF for the FSA9591 to properly detect a battery is not present.
B) R_{LEAK} must be at least 1G? to limit the leakage current on DETBAT_N for the FSA9591 to properly detect a battery is not present.
C) R_{LOAD} must be 100K? or less for the FSA9591 to detect a battery.

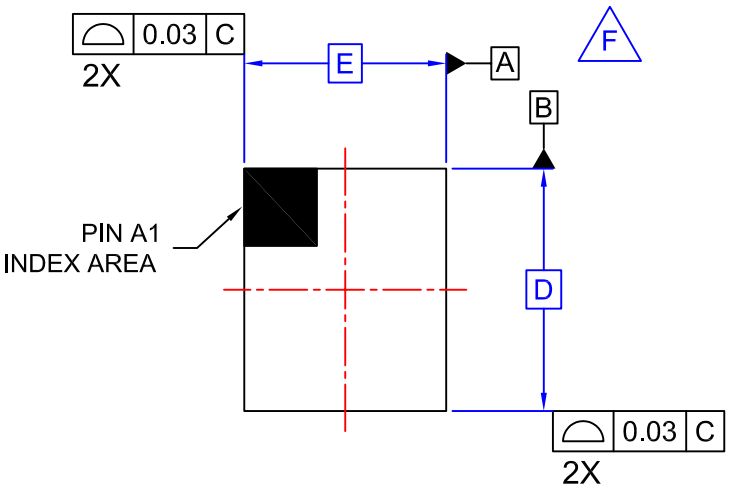
Figure 25. Reference Schematic Diagram

Table 33. Recommended Component Values for Reference Schematic

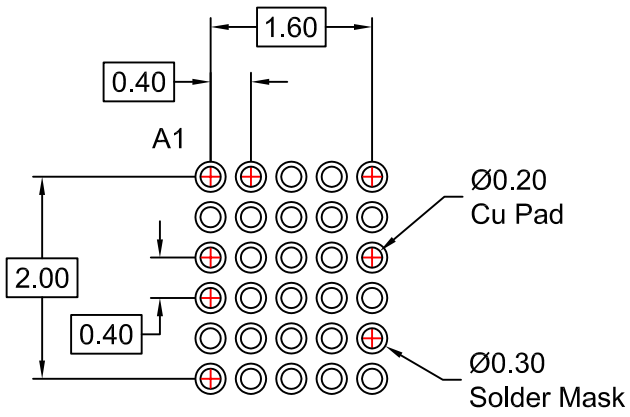
Symbol	Parameter	Recommended Value			Unit	Notes
		Min.	Typ.	Max.		
C_{VREF}	V_{REF} Decoupling	1	10	100	nF	This capacitance can affect the startup timing of V_{REF}
C_{VLDO1}, C_{VLDO2}	V_{VLDOx} Decoupling	1			µF	
C_{CHG_CAP}	CHG_CAP Decoupling	0.1			µF	
C_{VDDIO}	V_{DDIO} Decoupling	0.1	1.0		µF	
C_{VBAT1}	V_{BAT} Decoupling	0.1			µF	
C_{VBAT2}		2.2	4.7	10.0	µF	
R_{PU}	Pull-up Values		4.7		kΩ	These values are application specific.
R_{ID_CON},R_{DM_CON},R_{DP_CON}	ID_CON, DP_CON and DM_CON Series Resistance		2.2		Ω	Series resistance to improve surge performance of high-speed USB path.
C_{TVS1}	High-Speed TVS Diodes		1		pF	Recommended high-speed TVS diodes to improve ESD performance.
V_{TVS2}	High-Speed TVS Diode			32	V	V_{BR} for TVS on the V_{BUS_IN} line.
R_{TVS2}	High-Speed TVS Diode			1.4	Ω	R_{ON} for TVS on the V_{BUS_IN} line.
V_{TVS3}	TVS Diode			6	V	V_{BR} for TVS on the CHG_CAP line.
R_{TVS3}	TVS Diode			50	mΩ	R_{ON} for TVS on the CHG_CAP line.
C_{VBUS_IN}	V_{BUS_IN} Decoupling	1.0	4.7	10.0	µF	This is the recommended capacitance in the USB standard (for the downstream port V_{BUS} capacitance specification).
R_{LEAK}	DETBAT_N Maximum Leakage Specification			1	GΩ	This is the maximum leakage on DETBAT_N pin to ensure proper detection of no battery.
C_{LOAD}	DETBAT_N Maximum Capacitance Specification			500	pF	This is the maximum capacitance for proper detection of the battery.
R_{LOAD}	DETBAT_N Detection Threshold			100	kΩ	This is the maximum resistance for detection of battery present on DETBAT_N.
R_{PD}	ON_BT_UP Pull-Down Resistance		100		kΩ	These values are application specific based on disable timing required for ON_BT_UP.

Product-Specific Dimensions

Product	D	E	X	Y
FSA9591UCX	2.38	1.98	0.19	0.19



TOP VIEW



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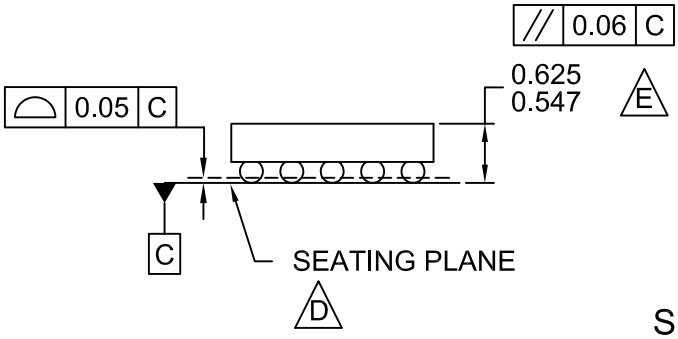
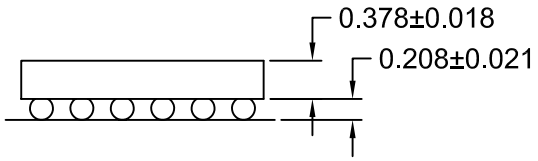
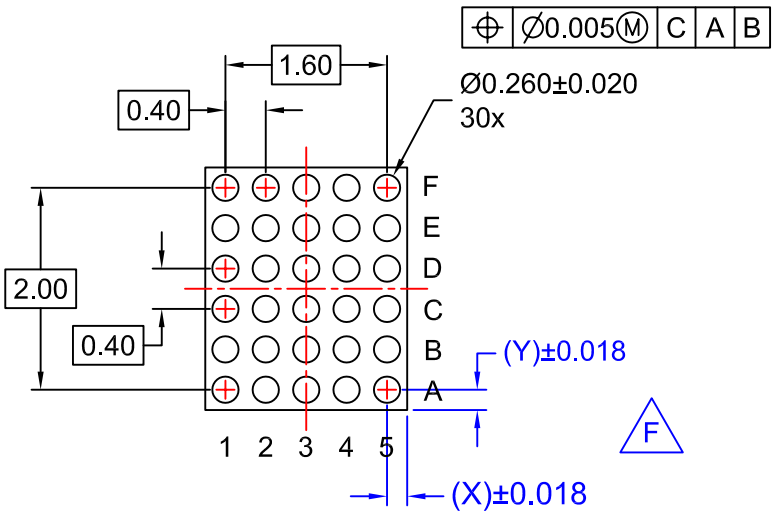
(NSMD PAD TYPE)





SIDE VIEWS



BOTTOM VIEW

NOTES:

A. NO JEDEC REGISTRATION APPLIES.
B. DIMENSIONS ARE IN MILLIMETERS.
C. DIMENSIONS AND TOLERANCE PER ASMEY14.5M, 1994.
D. DATUM C IS DEFINED BY THE SPHERICAL CROWNS OF THE BALLS.
E. PACKAGE NOMINAL HEIGHT IS 586 MICRONS ±39 MICRONS (547-625 MICRONS).
F. FOR DIMENSIONS D, E, X, AND Y SEE PRODUCT DATASHEET.
G. DRAWING FILNAME: MKT-UC030ABrev1

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