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FAIRCHILD SEMICONDUCTOR®

January 2014

FSAM50SM60A
Motion SPM® 2 Series

Features

- UL Certified No. E209204 (UL1557)
- 600 V - 50 A 3-Phase IGBT Inverter with Integral Gate Drivers and Protection
- Low-Loss, Short-Circuit Rated IGBTs
- Very Low Thermal Resistance Using Al_2O_3 DBC Substrate
- Separate Open-Emitter Pins from Low Side IGBTs for Three-Phase Current Sensing
- Single-Grounded Power Supply
- Optimized for 5 kHz Switching Frequency
- Built-in NTC Thermistor for Temperature Monitoring
- Inverter Power Rating of 4.0 kW / 100~253 VAC
- Adjustable Current Protection Level via Selection of Sense-IGBT Emitter's External Rs
- Isolation Rating: 2500 V_{rms} / min.

Applications

- Motion Control - Home Appliance / Industrial Motor

Resource

- AN-9043 - Motion SPM® 2 Series User's Guide

General Description

FSAM50SM60A is a Motion SPM® 2 module providing a fully-featured, high-performance inverter stage for AC Induction, BLDC, and PMSM motors. These modules integrate optimized gate drive of the built-in IGBTs to minimize EMI and losses, while also providing multiple on-module protection features including under-voltage lockouts, over-current shutdown, thermal monitoring, and fault reporting. The built-in, high-speed HVIC requires only a single supply voltage and translates the incoming logic-level gate inputs to the high-voltage, high-current drive signals required to properly drive the module's internal IGBTs. Separate negative IGBT terminals are available for each phase to support the widest variety of control algorithms.

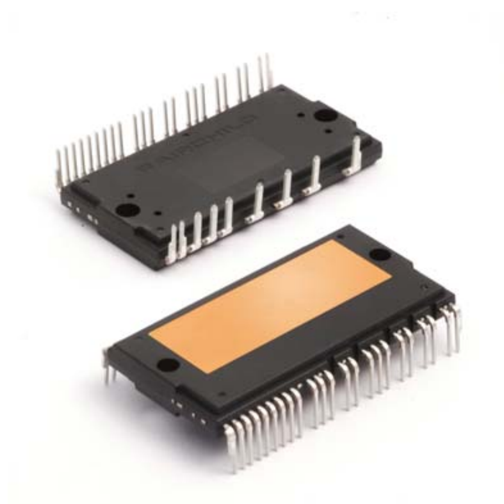


Figure 1. Package Overview

Package Marking and Ordering Information

Device	Device Marking	Package	Packing Type	Quantity
FSAM50SM60A	FSAM50SM60A	S32CA-032	Rail	8

Integrated Power Functions

- 600V - 50 A IGBT inverter for three-phase DC / AC power conversion (please refer to Figure 3)

Integrated Drive, Protection and System Control Functions

- For inverter high-side IGBTs: gate drive circuit, high-voltage isolated high-speed level shifting
  control circuit Under-Voltage Lock-Out (UVLO) Protection
  Note) Available bootstrap circuit example is given in Figures 13 and 14.
- For inverter low-side IGBTs: gate drive circuit, Short-Circuit Protection (SCP)
  control supply circuit Under-Voltage Lock-Out (UVLO) Protection
- Temperature Monitoring: system temperature monitoring using built-in thermistor
  Note) Available temperature monitoring circuit is given in Figure 14.
- Fault signaling: corresponding to a SC fault (low-side IGBTs) and UV fault (low-side control supply)
- Input interface: active-LOW Interface, works with 3.3 / 5 V logic, Schmitt-trigger input

Pin Configuration

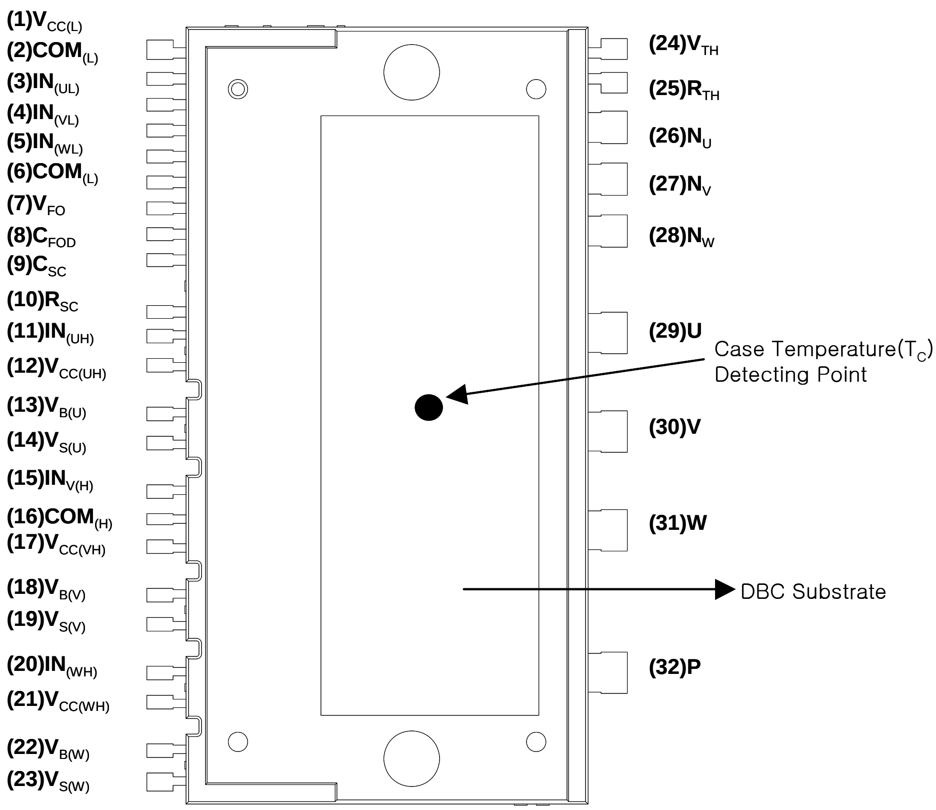


Figure 2. Top View

Pin Descriptions

Pin Number	Pin Name	Pin Description
1	$V_{CC(L)}$	Low-Side Common Bias Voltage for IC and IGBTs Driving
2	$COM_{(L)}$	Low-Side Common Supply Ground
3	$IN_{(UL)}$	Signal Input Terminal for Low-Side U-Phase
4	$IN_{(VL)}$	Signal Input Terminal for Low-Side V-Phase
5	$IN_{(WL)}$	Signal Input Terminal for Low-Side W-Phase
6	$COM_{(L)}$	Low-Side Common Supply Ground
7	V_{FO}	Fault Output
8	C_{FOD}	Capacitor for Fault Output Duration Selection
9	C_{SC}	Capacitor (Low-Pass Filter) for Short-Circuit Current Detection Input
10	R_{SC}	Resistor for Short-Circuit Current Detection
11	$IN_{(UH)}$	Signal Input for High-Side U-Phase
12	$V_{CC(UH)}$	High-Side Bias Voltage for U-Phase IC
13	$V_{B(U)}$	High-Side Bias Voltage for U-Phase IGBT Driving
14	$V_{S(U)}$	High-SideBias Voltage Ground for U-Phase IGBT Driving
15	$IN_{(VH)}$	Signal Input for High-Side V-Phase
16	$COM_{(H)}$	High-Side Common Supply Ground
17	$V_{CC(VH)}$	High-Side Bias Voltage for V-Phase IC
18	$V_{B(V)}$	High-Side Bias Voltage for V-Phase IGBT Driving
19	$V_{S(V)}$	High-Side Bias Voltage Ground for V-Phase IGBT Driving
20	$IN_{(WH)}$	Signal Input for High-side W-Phase
21	$V_{CC(WH)}$	High-Side Bias Voltage for W-Phase IC
22	$V_{B(W)}$	High-Side Bias Voltage for W-Phase IGBT Driving
23	$V_{S(W)}$	High-Side Bias Voltage Ground for W-Phase IGBT Driving
24	V_{TH}	Thermistor Bias Voltage
25	R_{TH}	Series Resistor for the Use of Thermistor (Temperature Detection)
26	N_U	Negative DC-Link Input Terminal for U-Phase
27	N_V	Negative DC-Link Input Terminal for V-Phase
28	N_W	Negative DC-Link Input Terminal for W-Phase
29	U	Output for U-Phase
30	V	Output for V-Phase
31	W	Output for W-Phase
32	P	Positive DC-Link Input

Internal Equivalent Circuit and Input/Output Pins

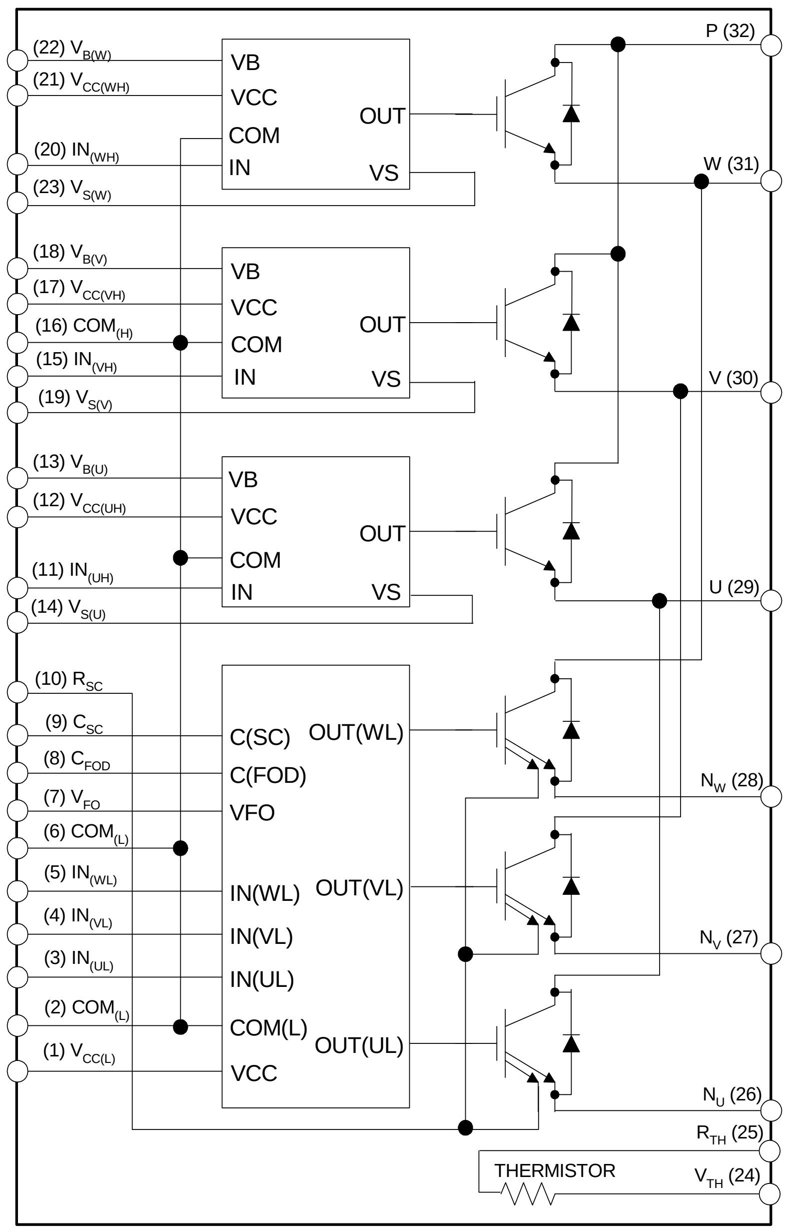


Figure 3. Internal Block Diagram

1st Notes:

1. Inverter low-side is composed of three sense-IGBTs including freewheeling diodes for each IGBT and one control IC which has gate driving, current-sensing and protection functions.
2. Inverter power side is composed of four inverter DC-link input pins and three inverter output pins.
3. Inverter high-side is composed of three normal-IGBTs including freewheeling diodes and three drive ICs for each IGBT.

Absolute Maximum Ratings (T_J = 25°C, unless otherwise specified.)

Inverter Part

Item	Symbol	Condition	Rating	Unit
Supply Voltage	V_{DC}	Applied to DC-Link	450	V
Supply Voltage (Surge)	$V_{PN(Surge)}$	Applied between P and N	500	V
Collector - Emitter Voltage	V_{CES}		600	V
Each IGBT Collector Current	$\pm I_C$	T_C = 25°C	50	A
Each IGBT Collector Current	$\pm I_C$	T_C = 100°C	25	A
Each IGBT Collector Current (Peak)	$\pm I_{CP}$	T_C = 25°C , Under 1ms Pulse Width	100	A
Collector Dissipation	P_C	T_C = 25°C per Chip	100	W
Operating Junction Temperature	T_J	(2nd Note 1)	-20 ~ 125	°C

2nd Notes:
1. It would be recommended that the average junction temperature should be limited to $T_J \le$ 125°C (at $T_C \le$ 100°C) in order to guarantee safe operation.

Control Part

Item	Symbol	Condition	Rating	Unit
Control Supply Voltage	V_{CC}	Applied between $V_{CC(UH)}$, $V_{CC(VH)}$, $V_{CC(WH)}$ - $COM_{(H)}$, $V_{CC(L)}$ - $COM_{(L)}$	20	V
High-Side Control Bias Voltage	V_{BS}	Applied between $V_{B(U)}$ - $V_{S(U)}$, $V_{B(V)}$ - $V_{S(V)}$, $V_{B(W)}$ - $V_{S(W)}$	20	V
Input Signal Voltage	V_{IN}	Applied between $IN_{(UH)}$, $IN_{(VH)}$, $IN_{(WH)}$ - $COM_{(H)}$ $IN_{(UL)}$, $IN_{(VL)}$, $IN_{(WL)}$ - $COM_{(L)}$	-0.3 ~ V_{CC}+0.3	V
Fault Output Supply Voltage	V_{FO}	Applied between V_{FO} - $COM_{(L)}$	-0.3 ~ V_{CC}+0.3	V
Fault Output Current	I_{FO}	Sink Current at V_{FO} Pin	5	mA
Current-Sensing Input Voltage	V_{SC}	Applied between C_{SC} - $COM_{(L)}$	-0.3 ~ V_{CC}+0.3	V

Total System

Item	Symbol	Condition	Rating	Unit
Self-Protection Supply Voltage Limit (Short-Circuit Protection Capability)	$V_{PN(PROT)}$	Applied to DC-Link, V_{CC} = V_{BS} = 13.5 ~ 16.5 V T_J = 125°C, Non-Repetitive, < 5 μs	400	V
Module Case Operation Temperature	T_C	See Figure 2	-20 ~ 100	°C
Storage Temperature	T_{STG}		-20 ~ 125	°C
Isolation Voltage	V_{ISO}	60Hz, Sinusoidal, AC 1 Minute, Connect Pins to Heat Sink Plate	2500	V_{rms}

Thermal Resistance

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Junction to Case Thermal Resistance	$R_{th(j-c)Q}$	Inverter IGBT Part (per 1/6 module)	-	-	1.00	°C/W
	$R_{th(j-c)F}$	Inverter FWDi Part (per 1/6 module)	-	-	1.50	°C/W
Contact Thermal Resistance	$R_{th(c-f)}$	DBC Substrate (per 1 Module) Thermal Grease Applied (2nd Note 3)	-	-	0.06	°C/W

2nd Notes:
2. For the measurement point of case temperature(T_C), please refer to Figure 2.
3. The thickness of thermal grease should not be more than 100 μm.

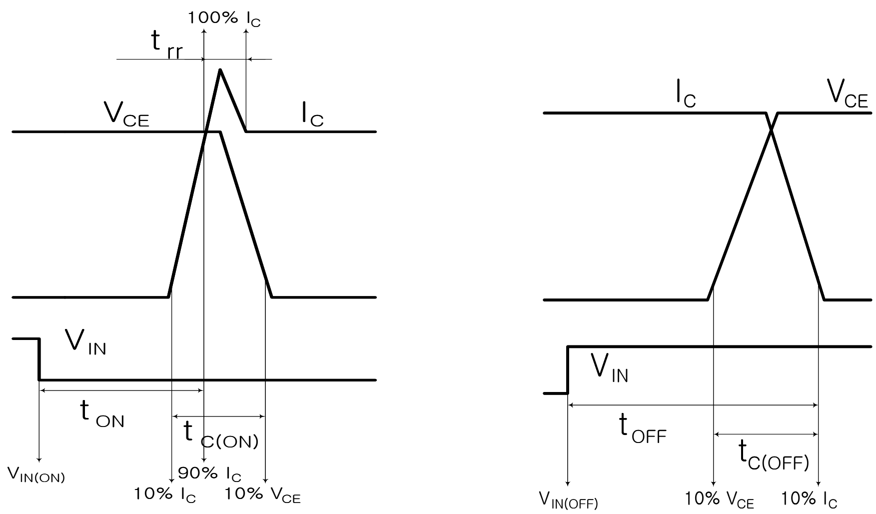
Electrical Characteristics

Inverter Part (T_J = 25°C, unless otherwise specified.)

Item	Symbol	Condition		Min.	Typ.	Max.	Unit
Collector - emitter Saturation Voltage	$V_{CE(SAT)}$	$V_{CC} = V_{BS}$ = 15 V, V_{IN} = 0 V	I_C = 50 A, T_J = 25°C	-	-	2.4	V
FWDi Forward Voltage	V_{FM}	V_{IN} = 5 V	I_C = 50 A, T_J = 25°C	-	-	2.1	V
Switching Times	t_{ON}	V_{PN} = 300 V, $V_{CC} = V_{BS}$ = 15 V, I_C = 50 A, T_J = 25°C, V_{IN} = 5 V ↔ 0 V, Inductive Load (High- And Low-Side) (2nd Note 4)		-	0.69	-	μs
	$t_{C(ON)}$			-	0.32	-	μs
	t_{OFF}			-	1.32	-	μs
	$t_{C(OFF)}$			-	0.46	-	μs
	t_{rr}			-	0.10	-	μs
Collector-Emitter Leakage Current	I_{CES}	$V_{CE} = V_{CES}$, T_J = 25°C		-	-	250	μA

2nd Notes:

4. t_{ON} and t_{OFF} include the propagation delay time of the internal drive IC. $t_{C(ON)}$ and $t_{C(OFF)}$ are the switching time of IGBT itself under the given gate driving condition internally. For the detailed information, please see Figure 4.



(a) Turn-on (b) Turn-off

Figure 4. Switching Time Definition

Electrical Characteristics (T$_J$ = 25°C, unless otherwise specified.)

Control Part

Item	Symbol	Condition		Min.	Typ.	Max.	Unit
Quiescent V_{CC} Supply Current	I_{QCCL}	V_{CC} = 15 V, $IN_{(UL, VL, WL)}$ = 5V	$V_{CC(L)}$ - $COM_{(L)}$	-	-	26	mA
	I_{QCCH}	V_{CC} = 15 V, $IN_{(UH, VH, WH)}$ = 5V	$V_{CC(UH)}$, $V_{CC(VH)}$, $V_{CC(WH)}$ - $COM_{(H)}$	-	-	130	μA
Quiescent V_{BS} Supply Current	I_{QBS}	V_{BS} = 15 V, $IN_{(UH, VH, WH)}$ = 5V	$V_{B(U)}$ - $V_{S(U)}$, $V_{B(V)}$ -$V_{S(V)}$, $V_{B(W)}$ - $V_{S(W)}$	-	-	420	μA
Fault Output Voltage	V_{FOH}	V_{SC} = 0 V, V_{FO} Circuit: 4.7 kΩ to 5 V Pull-up		4.5	-	-	V
	V_{FOL}	V_{SC} = 1 V, V_{FO} Circuit: 4.7 kΩ to 5 V Pull-up		-	-	1.1	V
Short-Circuit Trip Level	$V_{SC(ref)}$	V_{CC} = 15 V (2nd Note 5)		0.45	0.51	0.56	V
Sensing Voltage of IGBT Current	V_{SEN}	R_{SC} = 40 Ω, R_{SU} = R_{SV} = R_{SW} = 0 Ω and I_C = 75 A (See a Figure 6)		0.45	0.51	0.56	V
Supply Circuit Under-Voltage Protection	UV_{CCD}	Detection Level		11.5	12.0	12.5	V
	UV_{CCR}	Reset Level		12.0	12.5	13.0	V
	UV_{BSD}	Detection Level		7.3	9.0	10.8	V
	UV_{BSR}	Reset Level		8.6	10.3	12.0	V
Fault Output Pulse Width	t_{FOD}	C_{FOD} = 33 nF (2nd Note 6)		1.4	1.8	2.0	ms
ON Threshold Voltage	$V_{IN(ON)}$	High-Side	Applied between $IN_{(UH)}$, $IN_{(VH)}$, $IN_{(WH)}$ - $COM_{(H)}$	-	-	0.8	V
OFF Threshold Voltage	$V_{IN(OFF)}$			3.0	-	-	V
ON Threshold Voltage	$V_{IN(ON)}$	Low-Side	Applied between $IN_{(UL)}$, $IN_{(VL)}$, $IN_{(WL)}$ - $COM_{(L)}$	-	-	0.8	V
OFF Threshold Voltage	$V_{IN(OFF)}$			3.0	-	-	V
Resistance of Thermistor	R_{TH}	@ T_{TH} = 25°C (2nd Note 7, Figure 5)		-	50	-	kΩ
		@ T_{TH} = 100°C (2nd Note 7, Figure 5)		-	3.0	-	kΩ

2nd Notes:
5. Short-circuit protection is functioning only at the low-sides. It would be recommended that the value of the external sensing resistor (R_{SC}) should be selected around 40 Ω in order to make the SC trip-level of about 75A at the shunt resistors (R_{SU}, R_{SV}, R_{SW}) of 0 Ω. For the detailed information about the relationship between the external sensing resistor (R_{SC}) and the shunt resistors (R_{SU}, R_{SV}, R_{SW}), please see Figure 6.
6. The fault-out pulse width t_{FOD} depends on the capacitance value of C_{FOD} according to the following approximate equation: $C_{FOD} = 18.3 \times 10^{-6} \times t_{FOD}$ [F]
7. T_{TH} is the temperature of thermistor itself. To know case temperature (T_C), please make the experiment considering your application.

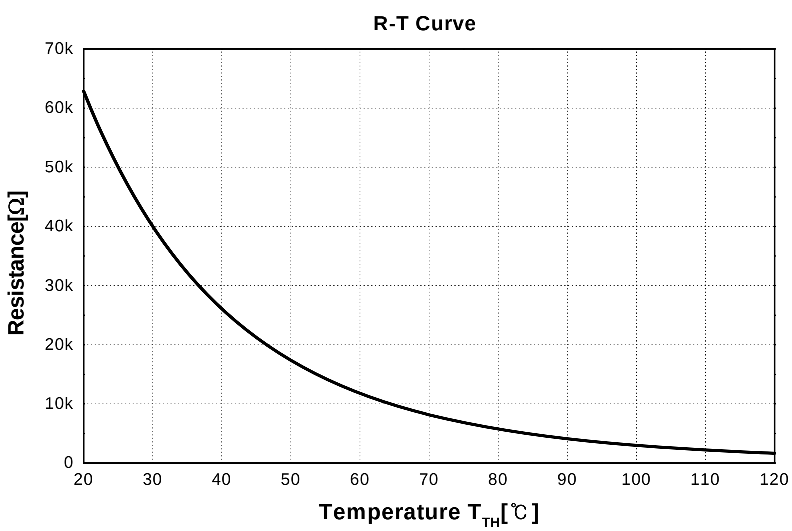


Figure 5. R-T Curve of The Built-in Thermistor

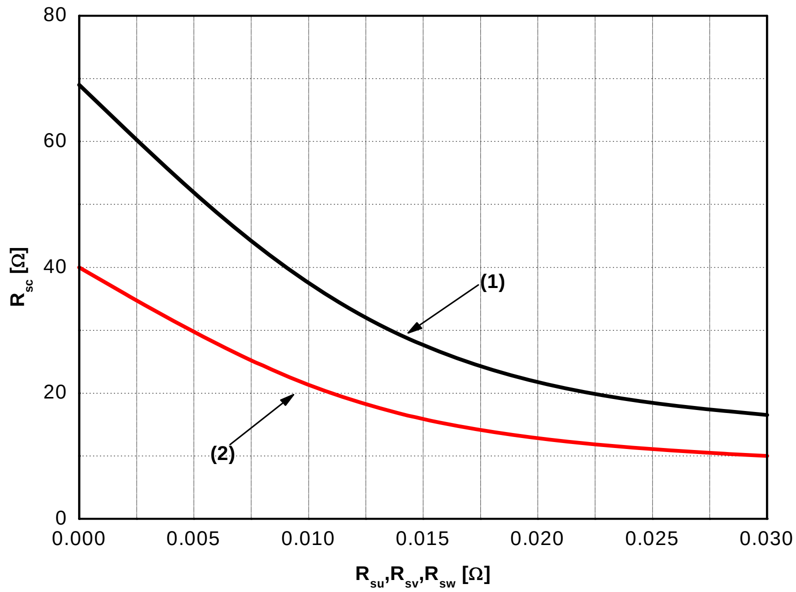


Figure 6. R_{SC} Variation by Change of Shunt Resistors (R_{SU}, R_{SV}, R_{SW}) for Short-Circuit Protection
(1) @ Current Trip Level ≒ 50 A
(2) @ Current Trip Level ≒ 75 A

Recommended Operating Conditions

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Supply Voltage	V_{PN}	Applied between P - N_U, N_V, N_W	-	300	400	V
Control Supply Voltage	V_{CC}	Applied between $V_{CC(UH)}$, $V_{CC(VH)}$, $V_{CC(WH)}$ - $COM_{(H)}$, $V_{CC(L)}$ - $COM_{(L)}$	13.5	15.0	16.5	V
High-side Bias Voltage	V_{BS}	Applied between $V_{B(U)}$ - $V_{S(U)}$, $V_{B(V)}$ - $V_{S(V)}$, $V_{B(W)}$ - $V_{S(W)}$	13.0	15.0	18.5	V
Blanking Time for Preventing Arm-short	t_{dead}	For Each Input Signal	3.5	-	-	μs
PWM Input Signal	f_{PWM}	$T_C \le 100°C$, $T_J \le 125°C$	-	5	-	kHz
Minimum Input Pulse Width	$PW_{IN(OFF)}$	$200 \le V_{PN} \le 400$ V, $13.5 \le V_{CC} \le 16.5$ V, $13.0 \le V_{BS} \le 18.5$ V, $0 \le I_C \le 100$ A, $-20 \le T_J \le 125°C$ V_{IN} = 5 V ↔ 0 V, Inductive Load (2nd Note 8)	3	-	-	μs
Input ON Threshold Voltage	$V_{IN(ON)}$	Applied between $IN_{(UH)}$, $IN_{(VH)}$, $IN_{(WH)}$ - $COM_{(H)}$, $IN_{(UL)}$, $IN_{(VL)}$, $IN_{(WL)}$ - $COM_{(L)}$		0 ~ 0.65		V
Input OFF Threshold Voltage	$V_{IN(OFF)}$	Applied between $IN_{(UH)}$, $IN_{(VH)}$, $IN_{(WH)}$ - $COM_{(H)}$, $IN_{(UL)}$, $IN_{(VL)}$, $IN_{(WL)}$ - $COM_{(L)}$		4 ~ 5.5		V

2nd Notes:
8. Motion SPM® 2 product might not make response if the $PW_{IN(OFF)}$ is less than the recommended minimum value.

Mechanical Characteristics and Ratings

Item	Condition		Min.	Typ.	Max.	Units
Mounting Torque	Mounting Screw: M4 (2nd Note 9 and 10)	Recommended 10 kg•cm	8	10	12	kg•cm
		Recommended 0.98 N•m	0.78	0.98	1.17	N•m
DBC Flatness		See Figure 7	0	-	+120	μm
Weight			-	32	-	g

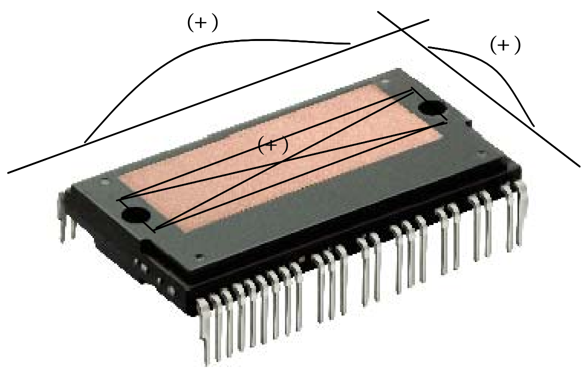


Figure 7. Flatness Measurement Position of The DBC Substrate

2nd Notes:

9. Do not make over torque or mounting screws. Much mounting torque may cause DBC substrate cracks and bolts and Al heat-sink destruction.
10. Avoid one side tightening stress. Figure 8 shows the recommended torque order for mounting screws. Uneven mounting can cause the Motion SPM® 2 package DBC substrate to be damaged.

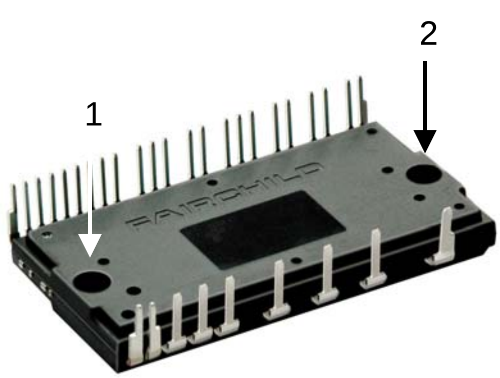
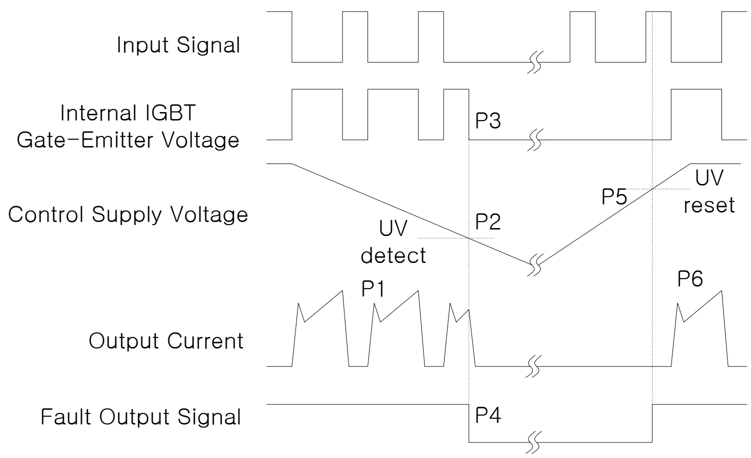


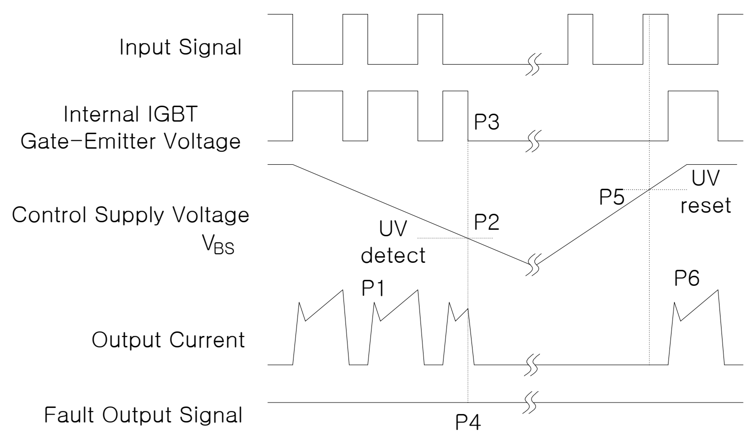
Figure 8. Mounting Screws Torque Order (1 → 2)

Time Charts of Protective Function



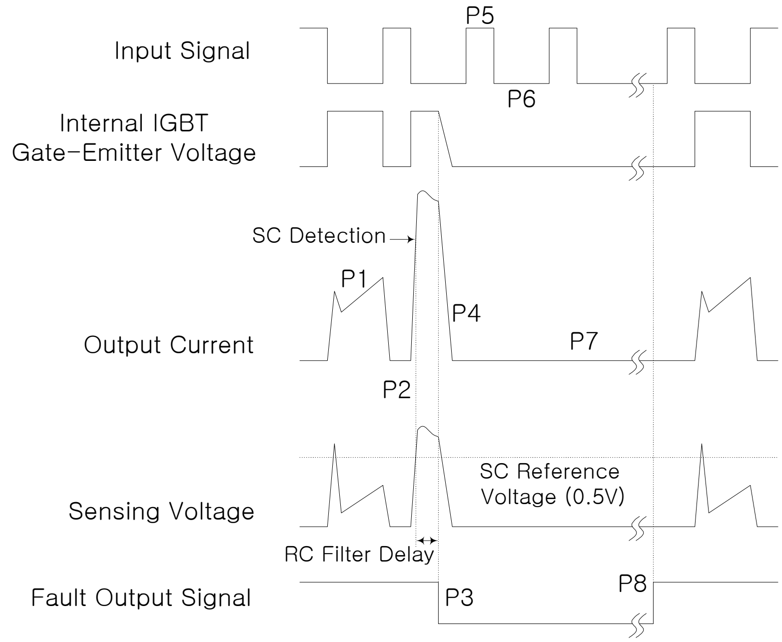
P1 : Normal operation: IGBT ON and conducting current .
P2 : Under-voltage detection.
P3 : IGBT gate interrupt.
P4 : Fault signal generation.
P5 : Under-voltage reset.
P6 : Normal operation: IGBT ON and conducting current.

Figure 9. Under-Voltage Protection (Low-Side)



P1 : Normal operation: IGBT ON and conducting current.
P2 : Under-voltage detection.
P3 : IGBT gate interrupt.
P4 : No fault signal.
P5 : Under-voltage reset.
P6 : Normal operation: IGBT ON and conducting current.

Figure 10. Under-Voltage Protection (High-Side)



P1 : Normal operation: IGBT ON and conducting current.
P2 : Short-circuit current detection.
P3 : IGBT gate interrupt / fault signal generation.
P4 : IGBT is slowly turned off.
P5 : IGBT OFF signal.
P6 : IGBT ON signal: but IGBT cannot be turned on during the fault-output activation.
P7 : IGBT OFF state.
P8 : Fault-output reset and normal operation start.

Figure 11. Short-Circuit Protection (Low-Side Operation Only)

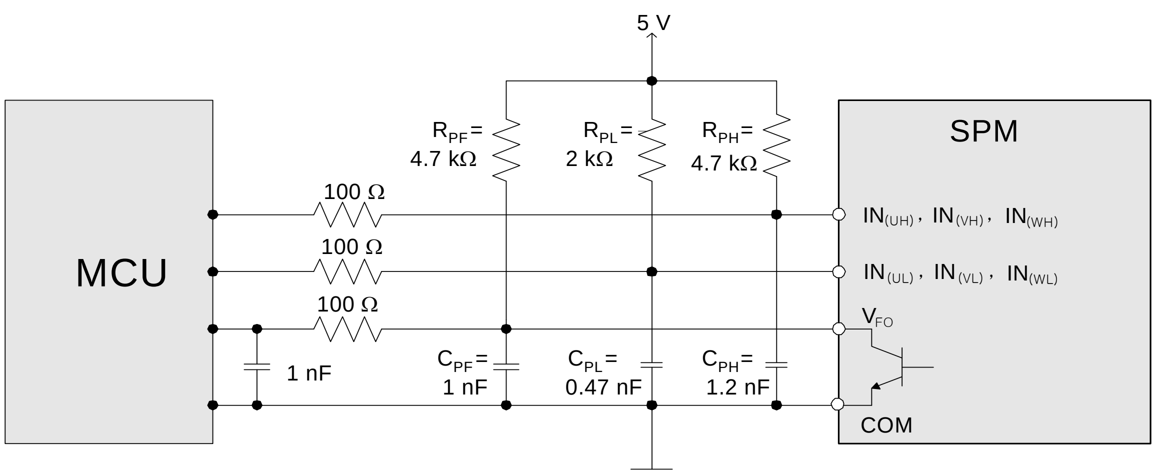


Figure 12. Recommended MCU I/O Interface Circuit

3rd Notes:

1. It would be recommended that by-pass capacitors for the gating input signals, $IN_{(UL)}$, $IN_{(VL)}$, $IN_{(WL)}$, $IN_{(UH)}$, $IN_{(VH)}$ and $IN_{(WH)}$ should be placed on the Motion SPM® 2 product pins and on the both sides of MCU and Motion SPM 2 Product for the fault output signal, V_{FO}, as close as possible.
2. The logic input works with standard CMOS or LSTTL outputs.
3. $R_{PL}C_{PL}/R_{PH}C_{PH}/R_{PF}C_{PF}$ coupling at each Motion SPM 2 product input is recommended in order to prevent input/output signals' oscillation and it should be as close as possible to each of Motion SPM 2 Product pins.

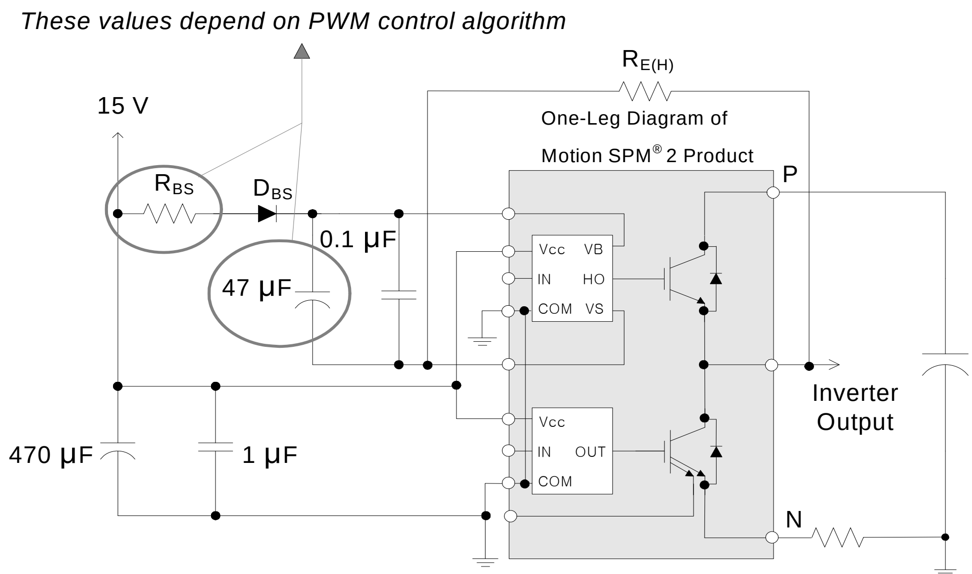


Figure 13. Recommended Bootstrap Operation Circuit and Parameters

3rd Notes:

4. It would be recommended that the bootstrap diode, D_{BS}, has soft and fast recovery characteristics.

5. The bootstrap resistor(R_{BS}) should be three times greater than $R_{E(H)}$. The recommended value of $R_{E(H)}$ is 5.6Ω, but it can be increased up to 20Ω for a slower dv/dt of high-side.

6. The ceramic capacitor placed between V_{CC} - COM should be over 1 μF and mounted as close to the pins of the Motion SPM® 2 product as possible.

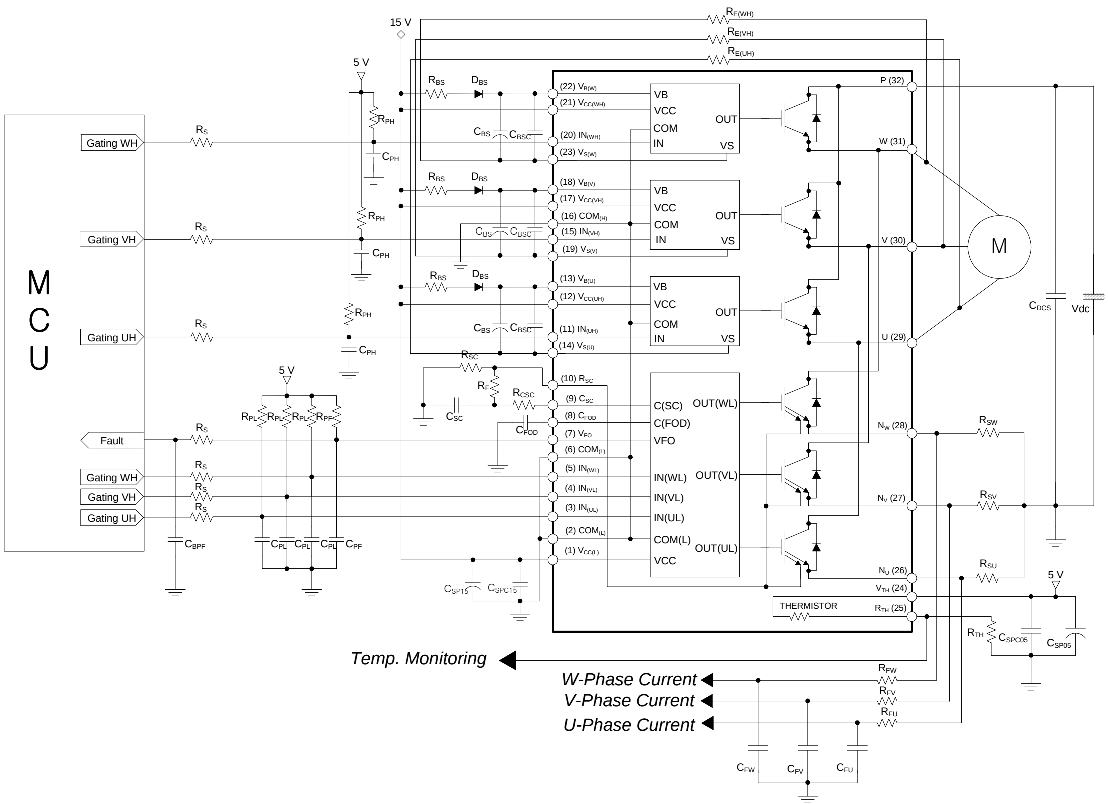
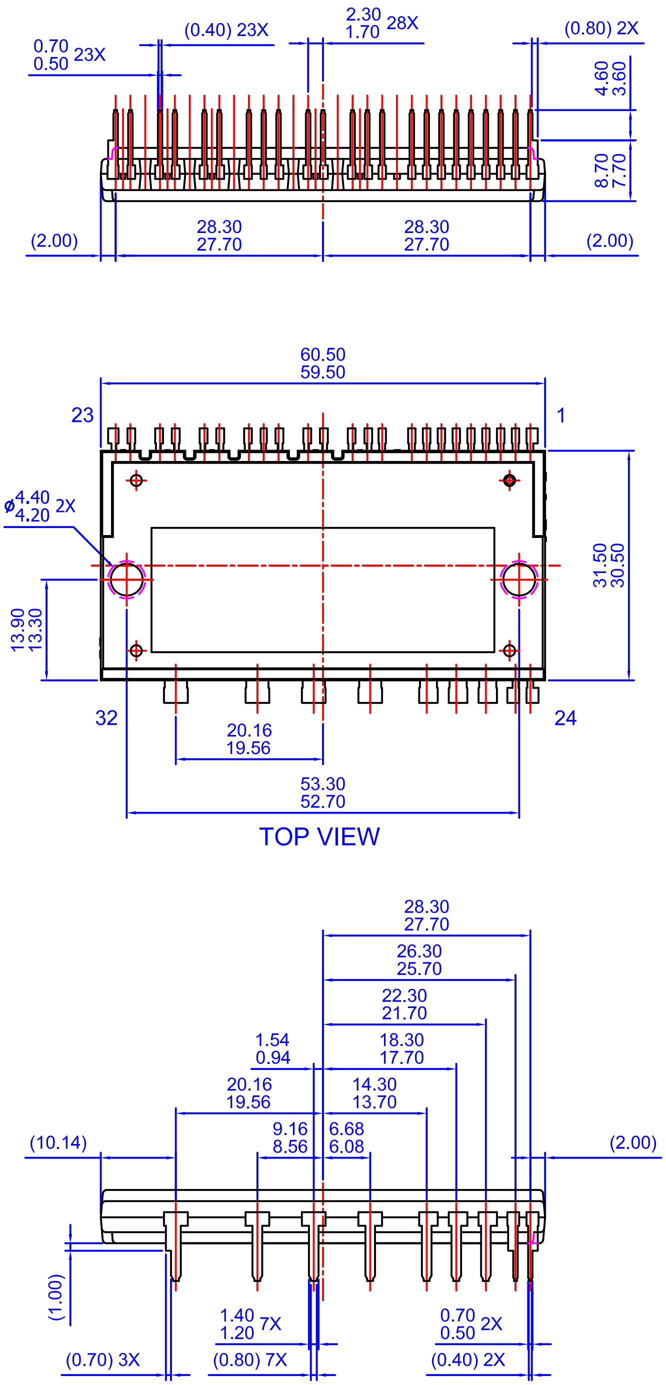
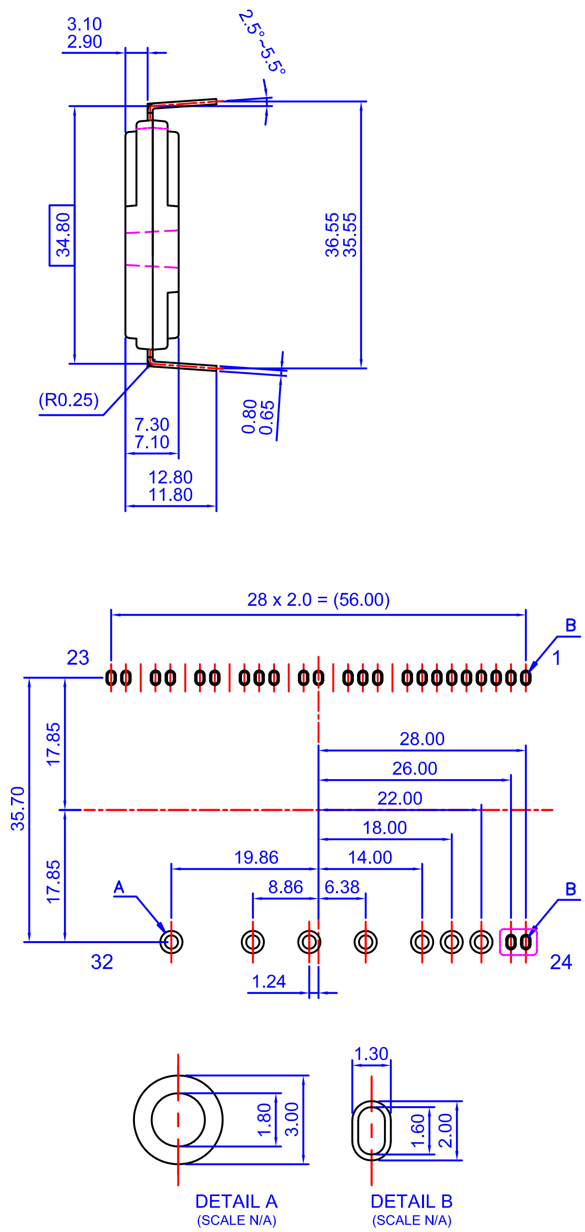


Figure 14. Application Circuit

4th Notes:

1. $R_{PL}C_{PL}$/$R_{PH}C_{PH}$ /$R_{PF}C_{PF}$ coupling at each Motion SPM® 2 product input is recommended in order to prevent input signals' oscillation and it should be as close as possible to each Motion SPM 2 product input pin.
2. By virtue of integrating an application specific type HVIC inside the Motion SPM 2 product, direct coupling to MCU terminals without any optocoupler or transformer isolation is possible.
3. V_{FO} output is open-collector type. This signal line should be pulled up to the positive side of the 5 V power supply with approximately 4.7 kΩ resistance. Please refer to Figure 12.
4. C_{SP15} of around seven times larger than bootstrap capacitor C_{BS} is recommended.
5. V_{FO} output pulse width should be determined by connecting an external capacitor(C_{FOD}) between C_{FOD}(pin 8) and $COM_{(L)}$(pin 2). (Example : if C_{FOD} = 33 nF, then t_{FO} = 1.8 ms (typ.)) Please refer to the 2nd note 6 for calculation method.
6. Each input signal line should be pulled up to the 5 V power supply with approximately 4.7 kΩ (at high side input) or 2 kΩ (at low side input) resistance (other RC coupling circuits at each input may be needed depending on the PWM control scheme used and on the wiring impedance of the system's printed circuit board). Approximately a 0.22 ~ 2 nF by-pass capacitor should be used across each power supply connection terminals.
7. To prevent errors of the protection function, the wiring around R_{SC}, R_F and C_{SC} should be as short as possible.
8. In the short-circuit protection circuit, please select the R_FC_{SC} time constant in the range 3 ~ 4 μs.
9. Each capacitor should be mounted as close to the pins of the Motion SPM 2 product as possible.
10. To prevent surge destruction, the wiring between the smoothing capacitor and the P & N pins should be as short as possible. The use of a high frequency non-inductive capacitor of around 0.1 ~ 0.22 μF between the P&N pins is recommended.
11. Relays are used at almost every systems of electrical equipments of home appliances. In these cases, there should be sufficient distance between the MCU and the relays. It is recommended that the distance be 5 cm at least.





LAND PATTERN RECOMMENDATIONS

NOTES: UNLESS OTHERWISE SPECIFIED

A) THIS PACKAGE DOES NOT COMPLY TO ANY CURRENT PACKAGING STANDARD

B) ALL DIMENSIONS ARE IN MILLIMETERS

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