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January 2014

FSB50325T

Motion SPM® 5 Series

Features

- UL Certified No. E209204 (UL1557)
- 250 V R_{DS(on)} = 1.8 Ω(Max) FRFET MOSFET 3-Phase Inverter with Gate Drivers
- Separate Open-Source Pins from Low-Side MOSFETs for Three-Phase Current-Sensing
- Active-HIGH Interface, Works with 3.3 / 5 V Logic, Schmitt-trigger Input
- · Optimized for Low Electromagnetic Interference
- HVIC for Gate Driving and Under-Voltage Protection
- Isolation Rating: 1500 V_{rms} / min.
- · RoHS Compliant

Applications

 3-Phase Inverter Driver for Small Power AC Motor Drives

Related Source

- AN-9082 Motion SPM5 Series Thermal Performance by Contact Pressure
- AN-9080 User's Guide for Motion SPM 5 Series
 Ver. 1

General Description

The FSB50325T is an advanced Motion SPM® 5 module providing a fully-featured, high-performance inverter output stage for AC Induction, BLDC and PMSM motors. These modules integrate optimized gate drive of the built-in MOSFETs (FRFET® technology) to minimize EMI and losses. The built-in, high-speed HVIC requires only a single supply voltage and translates the incoming logic-level gate inputs to the high-voltage, high-current drive signals required to properly drive the module's internal MOSFETs. Separate open-source MOSFET terminals are available for each phase to support the widest variety of control algorithms.



Package Marking & Ordering Information

Device	Device Marking	Package	Packing Type	Quantity
FSB50325T	FSB50325T	SPM5F-023	Rail	15

Absolute Maximum Ratings

Inverter Part (each MOSFET unless otherwise specified.)

Symbol	Parameter	Conditions	Rating	Unit
V _{DSS}	Drain-Source Voltage of Each MOSFET		250	V
*I _{D 25}	Each MOSFET Drain Current, Continuous	T _C = 25°C	1.5	Α
*I _{D 80}	Each MOSFET Drain Current, Continuous	T _C = 80°C	1.0	Α
*I _{DP}	Each MOSFET Drain Current, Peak	T _C = 25°C, PW < 100 μs	3.0	Α
*P _D	Maximum Power Dissipation	T _C = 25°C, For Each MOSFET	10	W

Control Part (each HVIC unless otherwise specified.)

Symbol	Parameter	Conditions	Rating	Unit
V _{CC}	Control Supply Voltage	Applied Between V _{CC} and COM	20	V
V _{BS}	High-side Bias Voltage	Applied Between V _B and V _S	20	V
V _{IN}	Input Signal Voltage	Applied Between IN and COM	-0.3 ~ V _{CC} + 0.3	V

Thermal Resistance

Symbol	Parameter	Conditions	Rating	Unit
$R_{ hetaJC}$	Junction to Case Thermal Resistance	Each MOSFET under Inverter Operating Condition (1st Note 1)	10.2	°C/W

Total System

Symbol	Parameter	Conditions	Rating	Unit
T _J	Operating Junction Temperature		-20 ~ 150	°C
T _{STG}	Storage Temperature		-50 ~ 150	°C
V _{ISO}	Isolation Voltage	60 Hz, Sinusoidal, 1 Minute, Connect Pins to Heat Sink Plate	1500	V _{rms}

1st Notes

^{1.} For the measurement point of case temperature $T_{\mathbb{C}},$ please refer to Figure 4.

^{2.} Marking " * " is calculation value or design factor.

Pin descriptions

Pin Number	Pin Name	Pin Description
1	СОМ	IC Common Supply Ground
2	V _{B(U)}	Bias Voltage for U Phase High Side MOSFET® Driving
3	V _{CC(U)}	Bias Voltage for U Phase IC and Low Side MOSFET Driving
4	IN _(UH)	Signal Input for U Phase High-Side
5	IN _(UL)	Signal Input for U Phase Low-Side
6	N.C	No Connectiion
7	V _{B(V)}	Bias Voltage for V Phase High Side MOSFET Driving
8	V _{CC(V)}	Bias Voltage for V Phase IC and Low Side MOSFET Driving
9	IN _(VH)	Signal Input for V Phase High-Side
10	IN _(VL)	Signal Input for V Phase Low-Side
11	N.C	No Connectiion
12	V _{B(W)}	Bias Voltage for W Phase High Side MOSFET Driving
13	V _{CC(W)}	Bias Voltage for W Phase IC and Low Side MOSFET Driving
14	IN _(WH)	Signal Input for W Phase High-Side
15	IN _(WL)	Signal Input for W Phase Low-Side
16	N.C	No Connectiion
17	Р	Positive DC-Link Input
18	U, V _{S(U)}	Output for U Phase & Bias Voltage Ground for High Side MOSFET Driving
19	N _U	Negative DC-Link Input for U Phase
20	N _V	Negative DC-Link Input for V Phase
21	V, V _{S(V)}	Output for V Phase & Bias Voltage Ground for High Side MOSFET Driving
22	N _W	Negative DC-Link Input for W Phase
23	W, V _{S(W)}	Output for W Phase & Bias Voltage Ground for High Side MOSFET Driving

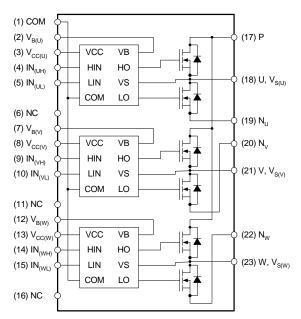


Figure 1. Pin Configuration and Internal Block Diagram (Bottom View)

1st Notes:

^{3.} Source terminal of each low-side MOSFET is not connected to supply ground or bias voltage ground inside Motion SPM® 5 product. External connections should be made as indicated in Figure 3.

Electrical Characteristics ($T_J = 25^{\circ}C$, $V_{CC} = V_{BS} = 15 \text{ V}$ unless otherwise specified.)

Inverter Part (each MOSFET unless otherwise specified.)

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
BV _{DSS}	Drain - Source Breakdown Voltage	$V_{IN} = 0 \text{ V}, I_D = 250 \mu\text{A} \text{ (2nd Note 1)}$	250	-	-	V
I _{DSS}	Zero Gate Voltage Drain Current	V _{IN} = 0 V, V _{DS} = 250V	-	-	250	μΑ
R _{DS(on)}	Static Drain - Source Turn-On Resistance	V _{CC} = V _{BS} = 15 V, V _{IN} = 5 V, I _D = 1.0 A	-	1.4	1.8	Ω
V _{SD}	Drain - Source Diode Forward Voltage	$V_{CC} = V_{BS} = 15V$, $V_{IN} = 0$ V, $I_{D} = -1.0$ A	-	-	1.2	V
t _{ON}			-	1076	-	ns
t _{OFF}		$V_{PN} = 150 \text{ V}, V_{CC} = V_{BS} = 15 \text{ V}, I_D = 1.0 \text{ A}$	-	660	-	ns
t _{rr}	Switching Times	$V_{IN} = 0 \text{ V} \leftrightarrow 5 \text{ V}$, Inductive Load L = 3 mH High- and Low-Side MOSFET Switching	-	108	-	ns
E _{ON}		(2nd Note 2)	-	47	-	μJ
E _{OFF}				3.1	-	μJ
RBSOA	Reverse Bias Safe Operating Area	$\begin{split} &V_{PN} = 200 \text{ V, } V_{CC} = V_{BS} = 15 \text{ V, } I_D = I_{DP}, V_{DS} = BV_{DSS}, \\ &T_J = 150 ^{\circ}\text{C} \\ &\text{High- and Low-Side MOSFET Switching (2nd Note 3)} \end{split}$		Full Square		

Control Part (each HVIC unless otherwise specified.)

Symbol	Parameter		Conditions	Min	Тур	Max	Unit
I _{QCC}	Quiescent V _{CC} Current	V _{CC} = 15 V, V _{IN} = 0 V	Applied Between V _{CC} and COM	-	-	160	μА
I _{QBS}	Quiescent V _{BS} Current	V _{BS} = 15 V, V _{IN} = 0 V	$ \begin{array}{c} \text{Applied Between V}_{B(U)} \text{ - U,} \\ \text{V}_{B(V)} \text{ - V, V}_{B(W)} \text{ - W} \end{array} $	-	-	100	μА
UV _{CCD}	Low-Side Under-Voltage	V _{CC} Under-Voltage	Protection Detection Level	7.4	8.0	9.4	V
UV _{CCR}	Protection (Figure 8)	V _{CC} Under-Voltage Protection Reset Level		8.0	8.9	9.8	V
UV _{BSD}	High-Side Under-Voltage	V _{BS} Under-Voltage	Protection Detection Level	7.4	8.0	9.4	V
UV _{BSR}	Protection (Figure 9)	V _{BS} Under-Voltage	Protection Reset Level	8.0	8.9	9.8	V
V _{IH}	ON Threshold Voltage	Logic HIGH Level	Applied between IN and COM	2.9	-	-	V
V _{IL}	OFF Threshold Voltage	Logic LOW Level	Applied between IN and COM		-	0.8	V
I _{IH}	Innut Diag Current	V _{IN} = 5 V	Applied between IN and COM	-	10	20	μА
I _{IL}	Input Bias Current	V _{IN} = 0 V	Applied between IN and COM	-	-	2	μΑ

2nd Notes:

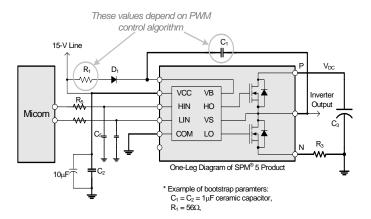
^{1.} BV_{DSS} is the absolute maximum voltage rating between drain and source terminal of each MOSFET inside Motion SPM[®] 5 product. V_{PN} should be sufficiently less than this value considering the effect of the stray inductance so that V_{PN} should not exceed BV_{DSS} in any case.

^{2.} t_{ON} and t_{OFF} include the propagation delay of the internal drive IC. Listed values are measured at the laboratory test condition, and they can be different according to the field applications due to the effect of different printed circuit boards and wirings. Please see Figure 4 for the switching time definition with the switching test circuit of Figure 5.

^{3.} The peak current and voltage of each MOSFET during the switching operation should be included in the Safe Operating Area (SOA). Please see Figure 5 for the RBSOA test circuit that is same as the switching test circuit.

Recommended Operating Condition

Symbol	Parameter	Conditions	Min.	Тур.	Max.	Unit
V _{PN}	Supply Voltage	Applied Between P and N	-	150	200	V
V _{CC}	Control Supply Voltage	Applied Between V _{CC} and COM	13.5	15.0	16.5	V
V _{BS}	High-Side Bias Voltage	Applied Between V _B and V _S	13.5	15.0	16.5	V
V _{IN(ON)}	Input ON Threshold Voltage	Applied Between IN and COM	3.0	-	V _{CC}	V
V _{IN(OFF)}	Input OFF Threshold Voltage	Applied Between III and COM	0	-	0.6	V
t _{dead}	Blanking Time for Preventing Arm-Short	$V_{CC} = V_{BS} = 13.5 \sim 16.5 \text{ V}, T_{J} \le 150^{\circ}\text{C}$	1.0	-	-	μS
f _{PWM}	PWM Switching Frequency	$T_{J} \le 150^{\circ}C$	-	15	-	kHz
T _C	Case Temperature	T _J ≤ 150°C	-20	-	125	°C



HIN	LIN	Output	Note
0	0	Z	Both FRFET Off
0	1	0	Low side FRFET On
1	0	VDC	High side FRFET On
1	1	Forbidden	Shoot through
Open	Open	Z	Same as (0,0)

Figure 2. Recommended MCU Interface and Bootstrap Circuit with Parameters

3rd Notes:

- 1. It is recommended the bootstrap diode D_1 to have soft and fast recovery characteristics with 600 V Rating.
- 2. Parameters for bootstrap circuit elements are dependent on PWM algorithm. For 15 kHz of switching frequency, typical example of parameters is shown above.
- 3. RC-coupling (R₅ and C₅) and C₄ at each input of Motion SPM 5 product and MCU (Indicated as Dotted Lines) may be used to prevent improper signal due to surge-noise.
- 4. Bold lines should be short and thick in PCB pattern to have small stray inductance of circuit, which results in the reduction of surge-voltage. Bypass capacitors such as C₁, C₂ and C₃ should have good high-frequency characteristics to absorb high-frequency ripple-current.

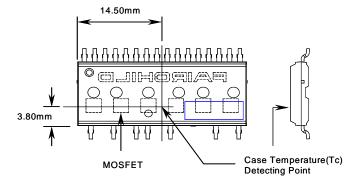


Figure 3. Case Temperature Measurement

3rd Notes

5. Attach the thermocouple on top of the heat-sink of SPM 5 package (between SPM 5 package and heatsink if applied) to get the correct temperature measurement.

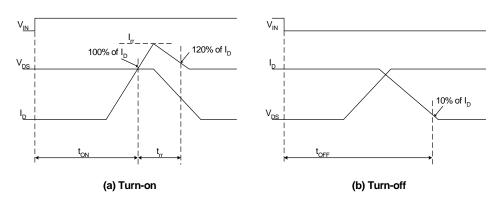


Figure 4. Switching Time Definitions

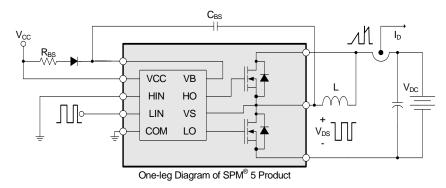


Figure 5. Switching and RBSOA (Single-pulse) Test Circuit (Low-side)

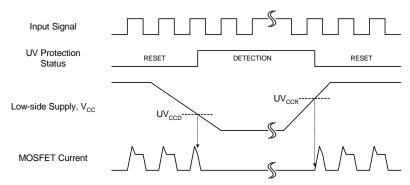


Figure 6. Under-Voltage Protection (Low-Side)

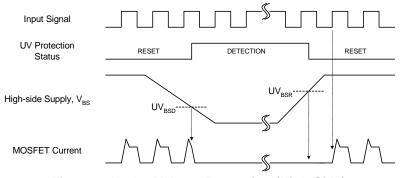


Figure 7. Under-Voltage Protection (High-Side)

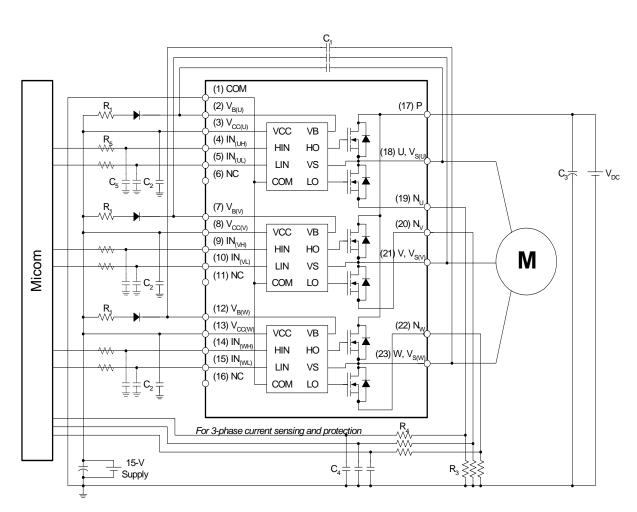
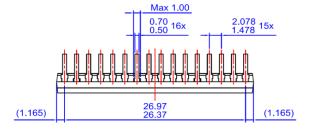


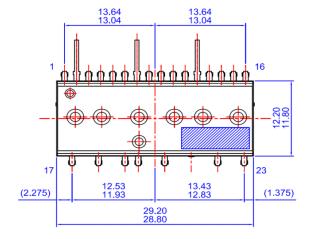
Figure 8. Example of Application Circuit

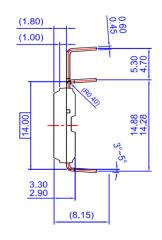
4th Notes:

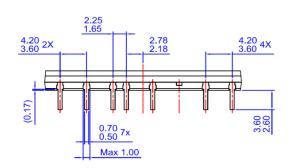
- 1. About pin position, refer to Figure 1.
- $2. \ RC\text{-coupling } (R_5 \text{ and } C_5, R_4 \text{ and } C_6) \text{ and } C_4 \text{ at each input of Motion SPM}^{\$} 5 \text{ product and MCU are useful to prevent improper input signal caused by surge-noise.}$
- 3. The voltage-drop across R₃ affects the low-side switching performance and the bootstrap characteristics since it is placed between COM and the source terminal of the low-side MOSFET. For this reason, the voltage-drop across R₃ should be less than 1 V in the steady-state.
- $4. \ Ground-wires \ and \ output \ terminals, should \ be \ thick \ and \ short \ in \ order \ to \ avoid \ surge-voltage \ and \ malfunction \ of \ HVIC.$
- 5. All the filter capacitors should be connected close to Motion SPM 5 product, and they should have good characteristics for rejecting high-frequency ripple current.

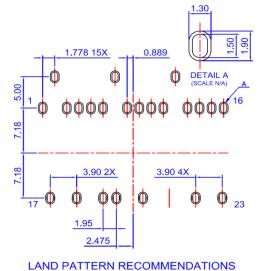
Detailed Package Outline Drawings











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